A CMOS Differential Buffer Amplifier with Accurate Gain and Clipping Control

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***Abstract*—A CMOS fully differential buffer amplifier with accurate gain and clipping control is presented. The gain is made variable by controlling the amount of the feedback around the power amplifier by means of an additional gain control loop. A new clipping technique is used to control the clipping level of the amplifier. The amplifier is realized in a 1.2 μm CMOS process with a single 5 V power supply. Measurements confirm the presented techniques.**

I. Introduction

FULLY differential circuit topologies have been widely adopted for high-performance analog circuits design. A differential buffer amplifier is used to interface fully differential circuits with the external world. Many different type CMOS buffer amplifiers have been proposed in the literature and continuous efforts have been being made to improve their performance. This paper will not discuss the design of buffer amplifiers as such but will focus on the gain and clipping control techniques for such amplifiers. The gain of most published buffer amplifiers is normally constant and in most cases equals to unity. However, for some applications such as modern digital telephones, the power amplifier driving a loudspeaker or an earpiece should have a tunable transfer characteristic to fulfill different requirements for different countries. Furthermore, accurate clipping control is required for good power efficiency and auditorial protection. In [1], a digital technique is presented for realizing the required gain control and clipping where the saturation level of the amplifier is considered as the clipping level. Since the saturation level depends on process, power supply, temperature, etc., accurate clipping control is not possible. In this paper, an analog approach to the control of the gain and the clipping level is described. The amplifier gain is tuned by controlling the amount of the feedback around the power amplifier with an additional gain control loop. It will be shown that by proper design of the on-chip feedback resistances the gain is linearly proportional to an external resistor ratio. The output clipping level is obtained by using a local feedback technique to control the feedback impedance around the buffer amplifier. A prototype buffer amplifier has been realized in a 1.2 μm CMOS technology. The gain and clipping control techniques presented are verified by the experimental results.

II. Amplifier Topology and Gain Control

Two amplifier topologies can be used to design a CMOS buffer amplifier as shown in Fig. 1 [2], [8]. The amplifier in Fig. 1(a) is the fully differential version of the well known inverting-type amplifier. Since the input is at the virtual ground, the design is challenged only by the output stage. The topology in Fig. 1(b) is derived from the noninverting amplifier. For this type of amplifiers, both the input and output stages need to be optimized to obtain a rail-rail input/output swing capability. The gain of the amplifier in Fig. 1(a) is given by R_{F2}/R_{F1} and that of Fig. 1(b) is $(1+R_{F2}/R_{F1})$. In both cases, the gain can be easily varied using digitally controlled on-chip switches to change the resistors R_{F1} and R_{F2}. However, for modern digital telephone applications, an external gain control is required to fulfill the different requirements for different countries. The external gain control can be realized digitally by sending gain setting bits to the chip through a serial interface. However, this will complicate the use of the chip. Therefore, a simpler external gain control is desirable.

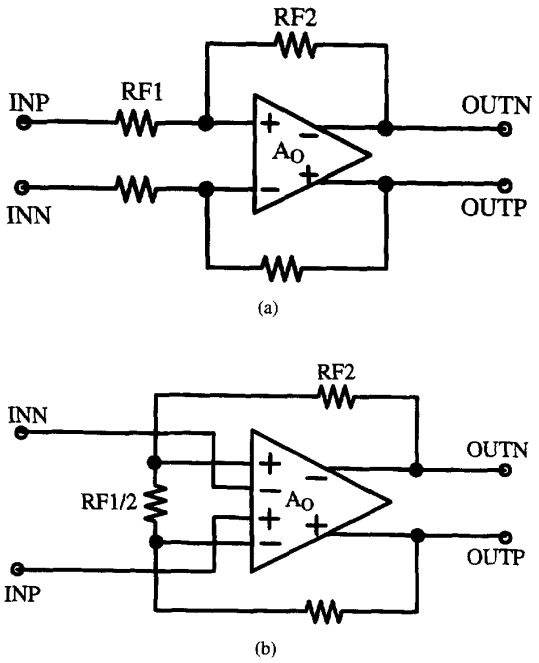

Fig. 1. Fully differential buffer amplifier topologies. (a) Inverting type. (b) Noninverting type.

The simplest approach could be to use some external resistors to set the gain. In this case, all resistors must be put externally to obtain a good matching. This would require four extra bonding pads for the case of the inverting amplifier in Fig. 1(a) and two extra bonding pads for the noninverting case. For a large system, these additional bonding pads can

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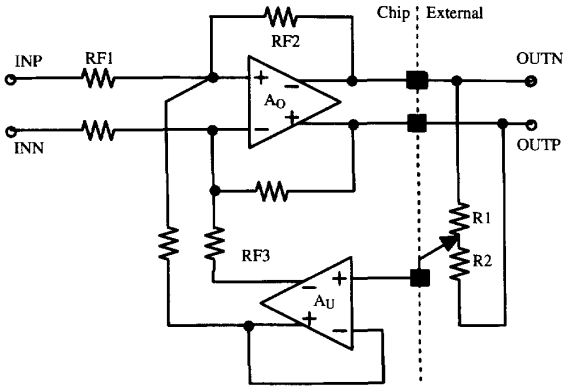

Fig. 2. Fully differential buffer with external gain control loop.

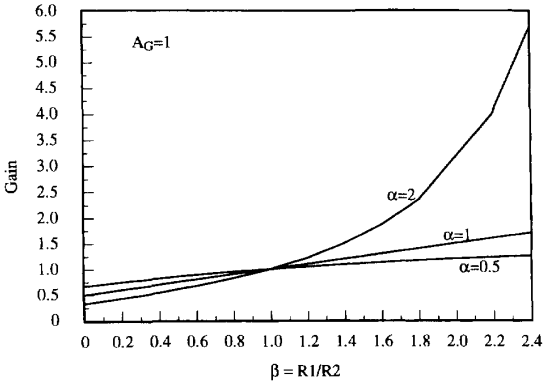

Fig. 3. Gain versus the external resistor ratio R_1/R_2 for $R_{F2}/R_{F1} = 1$.

be unacceptable as it could require a large IC package and therefore increase the cost. The technique presented is depicted in Fig. 2 where an additional feedback loop is added to the basic buffer amplifier. The inverting topology is chosen due to its simplicity. The additional feedback loop which is composed of an external potentiometer and a single-ended to differential unity gain buffer A_U controls the total amount of the feedback around the buffer amplifier. In this way the amplifier gain can be tuned by the external resistor ratio. Only one extra bonding pad is required to take the feedback signal from the external potentiometer.

The gain control mechanism can be physically explained as follows: for the case of an external resistor ratio $R_1/R_2 = \beta < 1$, the additional loop will enhance the total feedback and therefore the total gain will be lower than the inverting amplifier gain R_{F2}/R_{F1}. In this case, the increase of β will reduce the negative feedback effect resulting in an increase in the gain. For the case of $\beta = 1$, the additional feedback signal is exactly zero (i.e., common mode output signal) so that the gain is given by the classical expression R_{F2}/R_{F1}. For the case of $\beta > 1$, the gain control loop changes from negative to positive feedback which will compensate partially the conventional negative feedback effect and therefore the gain will be higher than R_{F2}/R_{F1}. Also in this case, the gain will increase with the increase of the resistor ratio β.

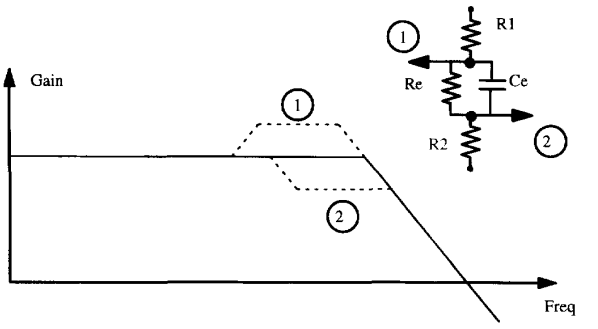

Fig. 4. Tunable transfer characteristic with external *RC* networks.

The exact amplifier gain is calculated as given by

$$G = \frac{1}{(R_{F1}/R_{F2} + R_{F1}/R_{F3}) + (R_{F1}/R_{F2} - R_{F1}/R_{F3})R_1/R_2} \times \left(1 + \frac{R_1}{R_2}\right). \quad (1)$$

The gain depends thus only on the ratio's of the on-chip resistance (R_{F1}, R_{F2}, and R_{F3}) and the ratio of the external potentiometer (R_1/R_2). Therefore, an accurate gain control is obtained. By introducing new parameters $A_G = R_{F2}/R_{F1}, \alpha = R_{F2}/R_{F3}$ and $\beta = R_1/R_2$, (1) can be rewritten in the following form

$$G = \frac{A_G(1+\beta)}{(1+\alpha)\left[1 + \left(\frac{1-\alpha}{1+\alpha}\right)\beta\right]}. \quad (2)$$

As expression (2) shows, different gain tuning ranges can be realized with β depending on the internal on-chip resistor ratio α. Fig. 3 shows how the gain is tuned with the external resistor ratio β for three different values of α. As explained above, for all three cases, the gain increases with the increase of β. Moreover, all three curves intercept at one point where $G = 1$ and $\beta = 1$, corresponding with the case of zero additional feedback. For the case of $\alpha = 0.5$, the tuning range is very limited and the gain G reaches its maximal value of $2A_G$ for β reaches the infinite (i.e., $R_2 = 0$). An interesting case is for $\alpha = 1$ where the gain is proportional to the potentiometer ratio β as given by $G = 0.5A_G(1+\beta)$. In this case, a linear external gain tuning is obtained. For the case of $\alpha = 2$, a large tuning range is possible with a small range of β. However, the tuning is a nonlinear function of the resistor ratio β. It is interesting to note that in this case the gain will be infinite for $\beta = 3$. This corresponds with the amplifier instability caused by the gain control loop as will be shown later.

By replacing the external potentiometer with some *RC* networks, the transfer characteristic can also be tuned as shown in Fig. 4. For the case where the feedback signal is taken from the node 1 the gain enhancement at the high frequencies is obtained. For the other case where node 2 is fedback the high frequency gain will drop. In this way different transfer characteristics can be realized to fullfil different countries' requirements.

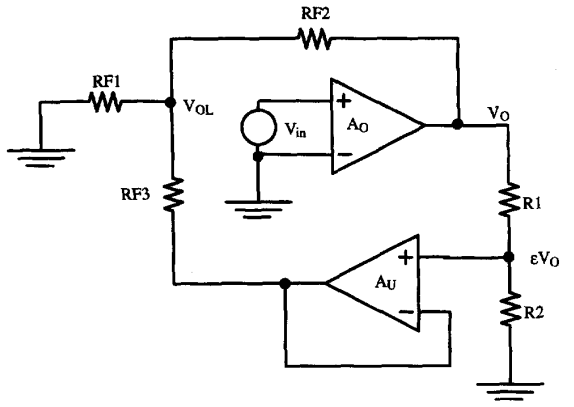

Fig. 5. Single-ended topology for stability analysis.

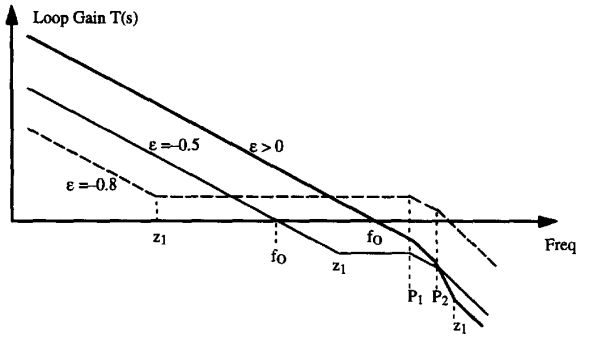

Fig. 6. Effect of the gain control loop on stability.

III. Stability Analysis

As the gain control loop feedback can be negative and positive, care must be taken to ensure the stability under all conditions. To simplify the analysis, a single-ended version of the amplifier is used as shown in Fig. 5. Taking into account the additional gain control loop the feedback loop gain is calculated as given by

$$T(s) = \frac{\mathrm{GBW}(G_{F2} + \varepsilon G_{F3} + s\tau_2 G_{F2})}{s(1+s\tau_1)(1+s\tau_2)(G_{F1}+G_{F2}+G_{F3})} \quad (3)$$

where GBW and $1/\tau_1$ are the gain-band-width and the second pole of the core amplifier A_O, respectively, $1/\tau_2$ is the -3 dB (i.e., GBW of the amplifier A_U) frequency of the unity gain buffer, $G_{Fi} = 1/R_{Fi}$ and ε is defined as the fraction of the output signal V_o taken by the external potentiometer. Thus, ε fullfils the condition $-1 < \varepsilon < +1$. The above loop gain has three poles and one zero as given by

$$\begin{aligned} p_0 &= 0 \\ p_1 &= 1/2\pi\tau_1 \\ p_2 &= 1/2\pi\tau_2 \\ z_1 &= \frac{(G_{F2}+\varepsilon G_{F3})}{G_{F2} 2\pi\tau_2}. \end{aligned} \quad (4)$$

As expected, for the case of $\varepsilon = 0$ (i.e., the external feedback signal vanishes), the zero z_1 cancels exactly the pole p_2 so that the stability is solely determined by the normal feedback.

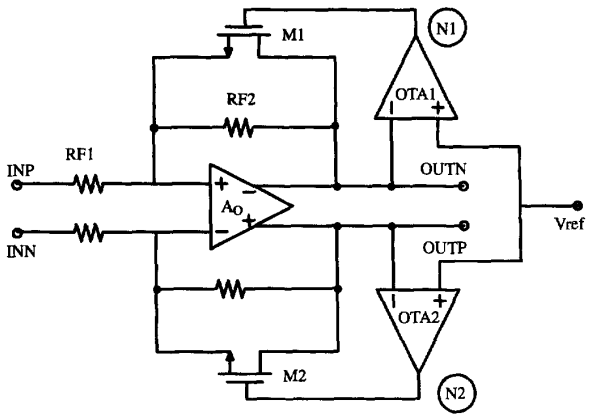

Fig. 7. Clipping control using a local feedback.

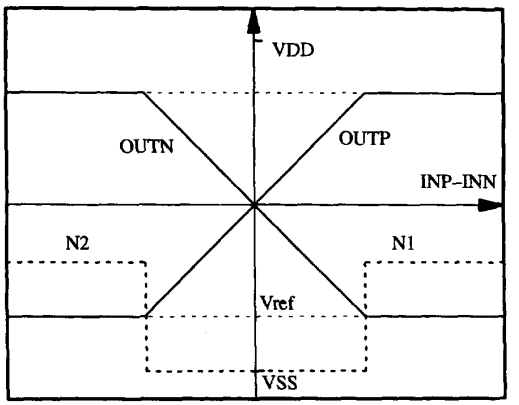

Fig. 8. DC transfer characteristic of the amplifier with clipping control.

The effect of ε on the stability is shown in Fig. 6. As long as $\varepsilon > 0$, the zero z_1 is always higher than the pole p_2. For good stability, one can either make the parasitic pole p_1 of the core amplifier higher than p_2 and z_1 or uses a small G_{F3} so that the pole p_2 is always close to the zero z_1. For the case of $\varepsilon < 0$, the gain control loop becomes positive feedback and the zero z_1 is lower than the pole p_2. Fig. 6 shows two cases for $\varepsilon < 0$. As can be seen that for $\varepsilon = -0.5$, the zero is beyond the unity-gain frequency f_O so that stability is ensured. However, for $\varepsilon = -0.8$, the phase margin will be very small due to high frequency parasitic poles in the vicinity of unity loop gain frequency f_O. In general the stability is guaranteed if the following two conditions are met:

$$\begin{aligned} 1/\tau_2 = \mathrm{GBW}(A_U) &> \mathrm{GBW}\frac{G_{F2}}{G_{F1}+G_{F2}+G_{F3}} \\ \varepsilon &> -R_{F3}/R_{F2}. \end{aligned} \quad (5)$$

The first condition is derived from the requirement that the zero must be higher than the unity-gain frequency f_O of the loop gain. This condition can be always fulfilled by designing $\mathrm{GBW}(A_U) > \mathrm{GBW}(A_O)$. The second condition ensures that the zero lies always in the left half plane. From (3) and (4) it is seen that if z_1 is in the right half plane, the total loop gain $T(s)$ will change to positive feedback with a gain larger than

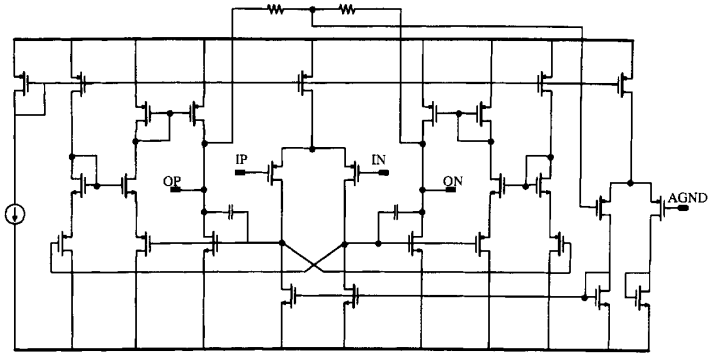

Fig. 9. Schematic of the core amplifier A_O.

unity and thus oscillation will occur. Since ε lies between $-1 < \varepsilon < +1$, the second stability condition can be guaranteed by choosing $R_{F3}/R_{F2} \geq 1$. It is interesting to note that $R_{F3}/R_{F2} = 1$ corresponds with the linear gain tuning case (i.e., $\alpha = 1$) described in the gain expression (2). Therefore, the choice of $R_{F3}/R_{F2} = 1$ results not only in a linear gain tuning but ensures also the stability.

IV. Accurate Clipping Control

Accurate clipping control can be realized by using diodes or $V_{\rm BE}$ multipliers [4], [5]. Both techniques could require CMOS compatible lateral pnp transistors which is not always well controlled in a CMOS process. Furthermore, diode clipping control technique relies on the $V_{\rm BE}$ value of the bipolar transistor which is also process and temperature dependent. Fig. 7 shows a better approach employing a local negative feedback to control the feedback resistance around the core amplifier A_O. The control loop is formed by two OTA's (OTA1, OTA2) together with two nMOS transistors (M1, M2) functioning as voltage controlled resistors.

In the normal case where the output swings are within the $\pm V_{\rm ref}$ range, both OTA's outputs N1 and N2 are at negative power supply VSS turning two feedback nMOS transistors completely off and therefore the clipping control loop has no any effect. This corresponds with the normal operation condition of the buffer amplifier. If one of the output voltage (e.g., OUTN) is lower than $V_{\rm ref}$ (e.g., 1 V), the corresponding OTA (e.g., OTA1) will function in its high gain region turning the MOS transistor on (e.g., M1). Therefore, the feedback loop formed by e.g. OTA1 and M1 starts active. Any increase in the input drive current (i.e., $i_{\rm in} = V_{\rm in}/R_{F2}$) will be absorbed by the MOS M1 so that the output OUTN will clip at the $V_{\rm ref}$ level. Due to the common-mode feedback loop in the fully differential amplifier A_O, the other output (e.g., OUTP) will clip at $-V_{\rm ref}$ level. Therefore, only one clipping level is required to control both positive and negative output which makes clipping control circuit simpler and less area consuming.

The above clipping mechanism is illustrated in Fig. 8. From Fig. 8 it is seen that during the clipping period, the OTA1's (OTA2) output will be about a V_T higher than the negative output swing which means that the OTA1 (OTA2) works in its high gain region and the negative feedback loop is closed through the nMOS M1 (M2). The stability analysis of this control loop is rather complicated due to the interaction of the common-mode feedback loop. Simulations show that the stability is guaranteed if the OTA's are frequency compensated for unity loop stability. This can be intuitively explained as follows: during the clipping period, the nMOS transistor M1 (M2) functions as a source follower with its source at OUTN (OUTP) and therefore the control loop can be considered as an unity feedback loop. It is important to note that during the clipping period the total feedback resistance around the core amplifier A_O is reduced due to parallel of R_{F2} and MOSFET M1 (M2) on resistance $R_{\rm ON}$. In this case, the main gain control loop stability condition (5) must be fulfilled as well. As mentioned before, the first condition will always be fulfilled by making $\mathrm{GBW}(A_U) > \mathrm{GBW}(A_O)$. The second condition is automatically met as the ratio R_{F3}/R_{F2} in the normal case is smaller than the ratio $R_{F3}/(R_{F2}//R_{\rm ON})$ during clipping.

V. Realization and Experimental Results

A complete power amplifier including feedback gain control and clipping control is realized. The schematic of the main power amplifier A_O is shown in Fig. 9 which is a two stage Miller type amplifier with the class-AB output stage as proposed in [2] and [3]. The output stage is biased at 0.5 mA and is designed to be able to drive 20 mA to the external load. A continuous-time common-mode feedback is used for common-mode output control. The amplifier A_U in the gain control loop is a simple class-A amplifier with rail-to-rail input and output swing [6], [7]. Rail-to-rail input is required as in the case of $\beta = 0$, the amplifier input will experience the full output swing of the main amplifier A_O. A simple class-A output stage is chosen as no heavy loads are to be driven. The internal resistor ratio $\alpha = R_{F2}/R_{F3}$ is chosen to be one for linear gain tuning and stability.

The amplifier is fabricated in a 1.2 μm CMOS process. A chip photo is shown in Fig. 10 and its active area measures 870×660 μm^2. Main experimental results are summarized in Table I. The amplifier is powered with a single 5 V supply and consumes 2 mA dc current. The amplifier gain is measured as

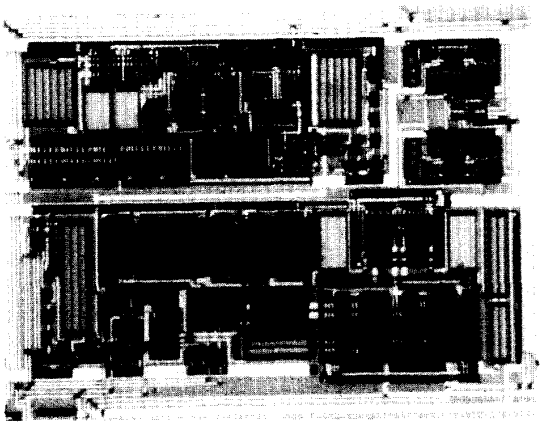

Fig. 10. Chip photograph of the buffer amplifier.

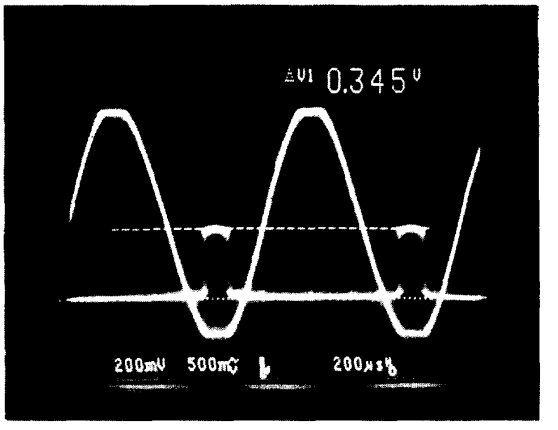

Fig. 11. Measured amplifier output signal with clipping control.

TABLE I
EXPERIMENTAL RESULTS

Parameter	Measured value
Power Supply	5 V
Gain [dB]	−6 to >20 dB
Power dissipation	2 mA
Output quiescent current	0.5 mA
Output driving	20 mA
Noise	26 nV//Hz @10kHz
Clipping control level	6 Vpp (differential)
THD (before clipping)	> 70 dB

a function of potentiometer ratio β. The results agree very well with the theoretical values in the gain range from −6 dB to 20 dB. For high gain the measured value is smaller than the theoretical one due to on-chip resistor mismatching. The result of clipping control is shown in Fig. 11. The amplifier starts to clip at 6 V_{pp} differential output swing which is the same as the designed value. In the same figure, the control voltage at node N1 for transistor M1 measured with a pico-probe is also shown. As can be seen, clipping starts when the control voltage N1 changes from VSS to a high level turning the feedback M1 on. Just before the clipping, the buffer amplifier is able to drive 20 mA to an external load with a measured THD of less than 70 dB.

VI. CONCLUSION

The design techniques are presented to control the gain and the clipping of CMOS buffer amplifiers used for driving a loudspeaker and earpieces. The gain control is realized by an extra feedback loop in parallel with the conventional feedback. By proper design of the on-chip feedback resistors the gain can be tuned linearly with an external potentiometer ratio. Design criteria are provided to guarantee the amplifier stability. An accurate clipping control is obtained by the use of a local feedback. A CMOS amplifier is fabricated in a 1.2 μm CMOS process. Measurements show that the gain is indeed linearly proportional to the external resistor ratio and the amplifier's output clips exactly at the predefined clipping level.

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