A CMOS Rectifier-Integrator for Amplitude Detection in Hard Disk Servo Loops

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***Abstract*—In this paper a CMOS alternative amplitude detection system is presented. It is designed as an alternative for the, bipolar, amplitude detection in hard disk servo systems. The amplitude is detected by converting the input voltage to a current, rectifying the current, and integrating it on a capacitor. For this a new OTA topology and a rectifier cell are designed. This circuitry is expanded with a very linear current mirror and an automatic offset compensation system to cope with technology spread. The measured accuracy of the amplitude detector is 0.2% (9 b). This makes the circuit suitable for implementation in state-of- the art hard disk systems with very high track densities and very short access times. Because the circuit is realized in standard CMOS its a further step toward CMOS only hard disk electronics. Because the circuit operates from a single 3 V power supply and has limited power consumption it can be used in battery powered systems.**

I. Introduction

THE SERVO LOOP of a hard disk is the control loop that is responsible for the accurate positioning of the read/write heads over the tracks. Two classes of servo systems exist: dedicated servo and embedded servo systems. A hard disk system with dedicated servo uses a separate platter containing waveforms used to position the heads over the tracks. At high track densities, deviations between the head positions due to temperature variations, limit the accuracy of a dedicated servo system. It is also not possible to accommodate the servo platter in small-profile hard disks. Therefore in state-of-the-art hard disks embedded servo systems are used [1].

In an embedded servo system, servo waveforms are incorporated in the sector headers. A simplified principle diagram of an embedded servo system is shown in Fig. 1. The servo signals are first amplified and then fed to an amplitude detector. The amplitude of these signals is a measure for the alignment of the read/write head over the tracks. Therefore it is fed to an A/D converter and further used to steer the head position motor.

The servo waveforms are sinusoidal bursts. For state-of-the-art hard disk systems the frequency of the burst is 10 to 12 MHz. The frequency of the servo burst is always taken smaller than the bitrate to avoid pulse distortion, and thus head mispositioning, due to intersymbol interference [1].

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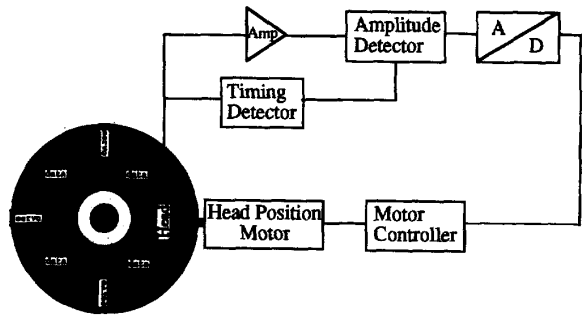

Fig. 1. Principle diagram of a hard disk servo system.

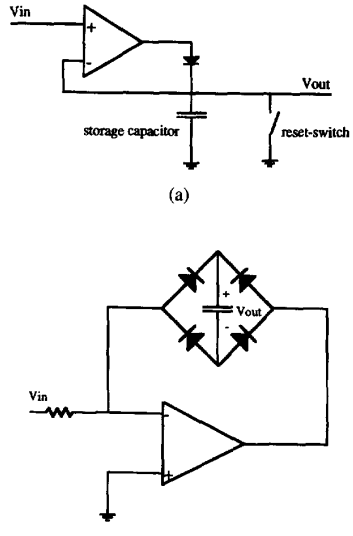

Fig. 2. (a) Principle diagram of a peak detector. (b) Principle diagram of a voltage rectifier.

The amplitude detector in servo systems is classically a peak detector, [2], [4]. A typical peak detector is shown in Fig. 2(a). In this type of circuit an opamp is used to store the maximal value of the input signal on a capacitor.

The problem with peak detection is double. First an opamp with very high slew rate (SR) is required. The required SR is given by

$$SR = \frac{I}{C} = V2\pi f. \tag{1}$$

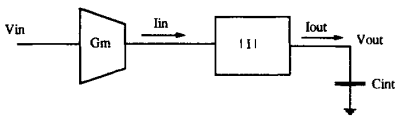

Fig. 3. Alternative principle for amplitude detection: voltage to current conversion, rectification, and integration.

C is the peak storing capacitor.
I is the maximal output current of the opamp.
V is the amplitude of the input voltage.
f is the burst frequency.

Typical values for the input voltage V is 1 V. The corresponding slew rate for an input frequency of 10 MHz is 63 V/μs. For a typical storage capacitor of 100 pF this leads to a current of 6.3 mA to be delivered by the opamp. The power consumption by the opamp will thus be unacceptable.

The second problem with peak detection is the sensitivity of its output signal to signal impairments. Every signal impairment increasing one of the peaks in a servo burst will directly be translated to an error on the output signal.

In this paper a circuit based on an alternative amplitude detector for sinusoidal bursts is presented. It is based on rectification followed by integration. The output voltage of a rectifier followed by an integrator is given by

$$V_{out} = V_{in} \int_0^{nT} \left| \sin\left(\frac{2\pi}{T} t\right) \right| dt. \tag{2}$$

n is the number of periods integrated.
T is the period of the burst.

From this formula it can be concluded that the output voltage V_{out} of the integrator is a measure for the amplitude V_{in} of the burst. In (2) the supposition is implicitly made that an integer number of periods is integrated. This is not necessary but it leads to simple formulas when the integral is evaluated. The same supposition will be made in the rest of the paper unless otherwise stated.

Amplitude detection based on rectification followed by integration is not as sensitive to signal impairments as peak detection because the signal impairments are averaged by the integration. Otherwise said, the amplitude of all periods in the burst is taken into account. The amplitude detector is no longer looking for the perturbation sensitive maximum.

A classical voltage-rectifier followed by an integrating capacitor is shown in Fig. 2(b). The input voltage of the circuit is converted to a current by the opamp. That current is rectified by a diode-bridge and integrated on a capacitor. This circuit will suffer from the same disease as the peak detector of Fig. 2(a) because it will also require an opamp with a very high gain-bandwidth product (GBW) to realize sufficient accuracy. This is solved by performing the voltage to current conversion separately from the rectification, see Fig. 3. This principle diagram does not call for opamps with high GBW. This is due to the fact that the OTA is performing the voltage to current conversion in open loop. Therefore its power consumption will be significantly less then the power consumption of the opamp in the peak detector.

The challenge in the design of the rectifier integrator is to realize sufficient linearity although its an open loop system. An exact definition of the linearity and the accuracy of the system will be given in the next paragraph. Their importance are explained by the fact that they influence the accuracy of the head positioning and the access time of the hard disk. When the amplitude detection is highly nonlinear the access time will increase because the predictive algorithms used when moving from one track to another will not work well. Extra iterations will be needed to predict the correct position of the target track if the amplitude detection is nonlinear.

As track densities will only increase in the future, accurate head positioning, and thus accurate amplitude detection, will become more important. The call for decreasing access time leads to the same conclusion. The amplitude detector presented here gives an answer to the following trends currently seen in hard disk applications: ever increasing track density and decreasing access time. It is also a step from bipolar to CMOS circuitry, reducing the production cost.

Section II of this paper continues with the definition of the required accuracy of the amplitude detector. In Section III a topology is sought for the rectifier. Section IV discusses the detailed design of that topology. In Section V the OTA responsible for the voltage to current conversion is designed. Section VI compares the simulation results to measurements on the realized chip. The last paragraph is the conclusion of this paper.

II. The Accuracy of the Amplitude Detector

The most important specification of the amplitude detector is its accuracy. It is defined as follows. First the output voltage V_{out} is determined for a set of input voltages V_{in}. This results in a set of points (V_{out}, V_{in}). Next a straight line is fitted to the points in the set for which V_{in} lies in the "accuracy input range." The "accuracy input range" is the input range over which the accuracy is specified. The linearity for a given input amplitude can then be defined

$$L_{in}(V_{in}) = \frac{V_{out}(V_{in}) - V_{out,\,fitted}(V_{in})}{V_{out,\,\max}}. \tag{3}$$

The accuracy of the amplitude detection over the specified input range is then given by

$$\text{Accuracy} = \max\left[L_{in}(V_{in})\right] - \min\left[L_{in}(V_{in})\right]. \tag{4}$$

The maximum and the minimum linearity are taken in the input range over which the accuracy is specified.

For a typical hard disk system, the accuracy must be 8 b (0.4%) for input voltages ranging from 0.25 Vpp–2 Vpp. This specification is derived from the total error budget of the servo loop and the errors generated by the other components in the loop.

The full set of target specifications for the amplitude detector as described in this and the previous paragraph is summarized in Table I. The power supply specifications in this table were not discussed yet. The circuit must be able to operate on a 3 V power supply so that it can be used in battery powered systems. For the same reasons the power consumption must be restrained.

TABLE I
TARGET AND MEASURED SPECIFICATIONS FOR THE AMPLITUDE DETECTION SYSTEM

	Target Specification	Measured Value
frequency of the input signal	≥ 12 MHz	12 MHz
Input range = $\frac{V_{in\_max}}{V_{in\_min}}$	$8 = \frac{2\ V_{pp}}{0.25\ V_{pp}}$	$8 = \frac{2\ V_{pp}}{0.25\ V_{pp}}$
Accuracy over the input range	8 bit (0.4%)	9 bit (0.2%)
Integration time	4 periods	4 periods
Technology	CMOS (1μ)	CMOS (1μ)
Power supply voltage	3 - 5 V	3 V
Power consumption	< 15 mW @ 3V	10 mW
Active chip area		0.42 μm^2

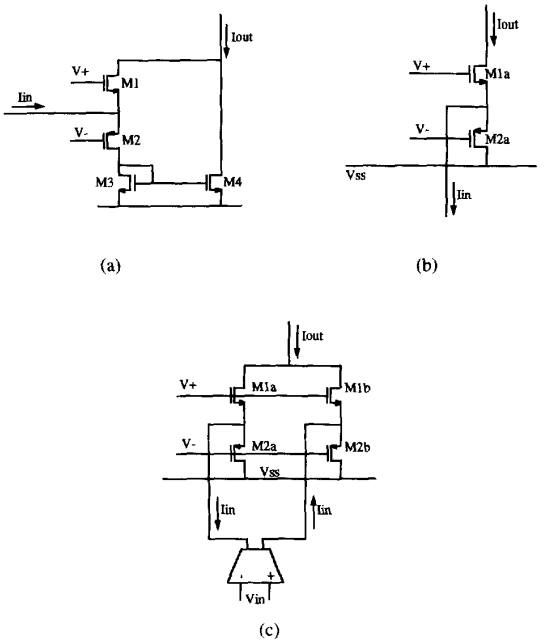

Fig. 4. (a) Schematic diagram of a classical CMOS current full wave rectifier. (b) Schematic diagram of a CMOS current half wave rectifier. (c) Combination of two CMOS current half wave rectifiers forming a CMOS current full wave rectifier.

III. SELECTION OF A CURRENT-RECTIFIER TOPOLOGY

A typical CMOS rectifier is given in Fig. 4(a). In this cell the transistors operate as switches. Currents driven into the cell (positive currents) flow into the source of M2. They are mirrored to the output by M3–M4. M1 is off. Currents drawn from the cell (negative currents) flow through the source of M1. In that case M2 is off.

The presence of a current mirror in the circuit of Fig. 4(a) degrades the accuracy of the rectifier. First, mismatch between the threshold voltages of M3 and M4 affects the linearity of the current mirror and thus of the rectification. Moreover, the finite bandwidth of the current mirror reduces the bandwidth of the rectifier. In this paragraph it is shown that rearranging the topology makes it possible to leave the current mirror out.

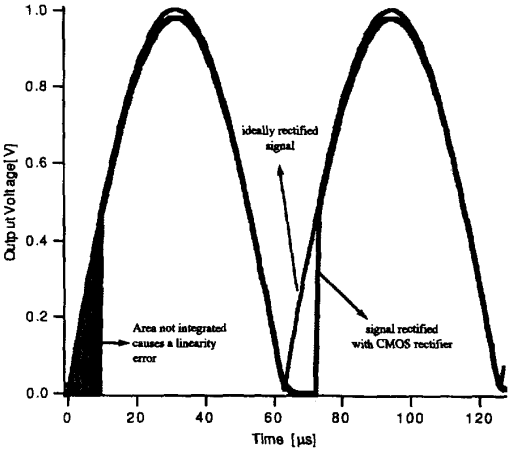

Fig. 5. Output signal of the CMOS full wave current rectifier compared to an ideally rectified input signal.

Fig. 4(b) shows a CMOS half wave rectifier. Positive input currents of this rectifier are conveyed to the ground. Negative input currents are drawn from the output. It is possible to construct a full wave rectifier with two half wave rectifiers, see Fig. 4(c). Here, two half wave rectifiers are driven by the opposite output phases of an OTA with a differential output. Their outputs are summed. When one output of the OTA drives positive current into one half wave rectifier, the other output will draw negative current from the other half wave rectifier. There will always be one half wave rectifier drawing current from the output. Therefore, the OTA and the two half wave rectifiers make up a full wave rectifier. The advantage of this strategy is that there is no inherent source of nonlinearity anymore in the rectifier. The use of an OTA was already proposed in Fig. 3. The important change here is that a differential OTA is used.

The output current of the circuit of Fig. 4(c), together with an ideally rectified current is plotted in Fig. 5. The figure shows a delay in the output signal after the zero crossing of the input signal. The delay causes an error on the integrated output signal as shown in Fig. 5. This error affects the linearity of the rectifier because it is not linearly proportional to the input signal's amplitude.

The delay is due to the fact that the transistors M1a,b and M2a,b in Fig. 4(c) have to switch from the off state to conduction or vice versa. When this happens the gate source voltage of these transistors swings between zero and VT. The total voltage swing at each input is thus 2 VT. This causes a delay approximately given by

$$\Delta t = \frac{C_{in}}{I_{in}} \Delta V = \frac{C_{in}}{I_{in}} 2VT. \tag{5}$$

C_{in} is the input capacitance of the rectifier.

I_{in} is the input current of the rectifier.

ΔV is the voltage swing at the input of the rectifier.

Δt could be decreased by driving the gates of M1a,b and M2a,b with opamps. The input of each opamp should compare the input voltage of the rectifier to a reference voltage. This feedback configuration results in an increase of the input

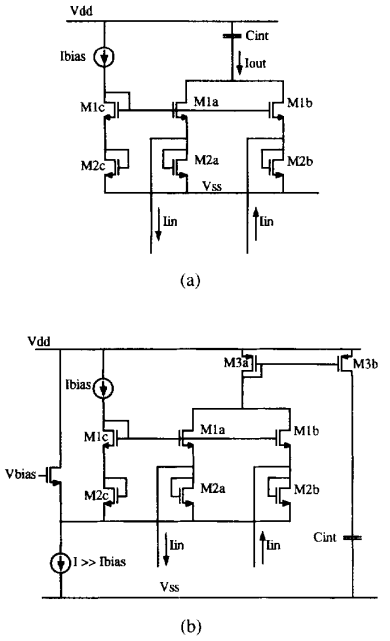

Fig. 6. (a) nMOS only full wave current rectifier followed by an integration capacitor. (b) nMOS only full wave current rectifier with lifted input bias voltage. At the output a current mirror is added.

current around the zero crossing of the input signal. According to (5) this will decrease the time delay. The introduction of an opamp is however no real solution to the problem. It only shifts the design problem from slew rate (SR) of the OTA rectifier combination to slew rate of the opamp.

Formula (5) contains two other parameters that can be influenced to decrease the time delay: the voltage swing and the input capacitance. The input capacitance of the rectifier is approximately given by

$$C_{in} = C_{gs,\,\mathrm{M1}} + C_{sb,\,\mathrm{M1}} + C_{gs,\,\mathrm{M2}} + C_{sb,\,\mathrm{M2}}. \tag{6}$$

The CMOS technology used is of the n-well type. So the junction capacitance per unit area is approximately 2 times larger for pMOST than for nMOST. The mobility in the n-well is approximately 3 times lower than in the substrate. Therefore a pMOST must be 3 times wider than a nMOST to realize the same β for transistors with the same length. This yields

$$\begin{aligned} C_{gs,\,\mathrm{M2}} &= 3C_{gs,\,\mathrm{M1}}, \\ C_{sb,\,\mathrm{M2}} &= 6C_{sb,\,\mathrm{M1}}. \end{aligned} \tag{7}$$

From (7) it follows that at least 3/4 of the input capacitance is due to the pMOST. Therefore the input capacitance will be 2–3.5 times smaller when the pMOST are replaced by nMOST. This is shown in Fig. 6(a). Replacing the pMOST by a nMOST is possible because that transistor only serves to dump positive input currents to the ground.

The voltage swing at the input of the rectifiers can be decreased by the introduction of a bias current in the rectifier, see Fig. 6(a). In that case the input transistors do not completely switch off during the zero crossing of the input current. One of the transistors of a half wave rectifier will only switch off when the other one, conducting the current during that half period, is completely on. How long this takes depends again on the SR ratio I_{in}/C_{in}.

The bias current adds extra current to the output current of the rectifier. This creates an error on the integrated output voltage because extra current will be integrated as long as the non conducting transistor in each half wave rectifier is not completely off. It is very difficult to calculate, or even to simulate, the error caused by bias current integration accurately because it depends on the behavior of the transistors in weak inversion, moderate inversion and the saturation region. It is particularly very hard to model the transitions between the different regions of operation. However, the error caused by bias current integration is given by

$$V_{error} = \frac{I_{BIAS} t_{off}}{C_{int}} \tag{8}$$

where C_{int} is the integrating capacitor

In (8) t_{off} is the time needed to switch off the transistors that should not conduct during a given half period. This is also the time it takes for the conducting transistor to switch completely on, because it is the growing of the V_{GS} of the conducting transistor that switches the other one off. This V_{GS} does not depend linearly on the input current, nor does t_{off} depend linearly on V_{GS}. Therefore there is no linear proportionality between t_{off} and the input current. This allows to conclude that the error caused by bias current integration does not depend linearly on the bias current. Therefore it will affect the linearity of the rectifier. According to (8), the only way to decrease the error caused by partial integration of the bias current is to make that bias current as small as possible.

The bias current can be decreased until the transistors operate in the weak inversion region. The voltage at the inputs of the rectifier is then slightly below the threshold voltage of the input transistors. This voltage difference is called V_{WI}. The maximum voltage swing at the input in that case is given by

$$\Delta V = 2(V_{GS,\,\mathrm{M1}} - VT + V_{WI}). \tag{9}$$

$V_{GS,\,M1}$ is the gate source voltage of M1 for maximum input current. In the next paragraph it will be shown that this leads to a ΔV of ± 0.4 V. ΔV was ± 1 V without biasing.

The conclusion of this paragraph is that the replacement of the pMOST at the input of the rectifier by nMOST and the introduction of a bias current reduces the delay around the zero crossing of the input current with at least a factor 4. At least a factor of 2 is coming from the reduction of the input capacitance. The remaining factor 2 comes from reduction of the input voltage swing.

IV. Design of the Rectifier-Integrator

Transistors M1a,b and M2a,b in Fig. 6(a) are sized so that the $V_{GS} - VT$ is equal to 0.3 V for maximum input current (100 μA) This gives a transistor width $W = 30\ \mu$. The length of M1a,b and M2a,b is taken minimal (1 μ) to reduce the input capacitance. The choice of a maximum input current of 100 μA is explained below.

TABLE II
INFLUENCE OF VT MISMATCH IN THE CURRENT MIRROR ON THE ACCURACY OF THE RECTIFIER-INTEGRATOR

$\Delta V_T = V_{T,MP3b} - V_{T,MP3a}$ (mV)	Accuracy (bits)
5	7.9
-5	9.7
10	7.1
-10	8.2
20	6.4
-20	6.5

The bias current through M1a,b and M2a,b is chosen to be 0.2 μA. The onset of weak inversion for a 30/1 nMOST is approximately 5 μA. Operation of the transistor in weak inversion is thus guaranteed. V_{WI} in (9) is approximately 0.1 V. The maximum voltage swing at the input is $\pm$0.4 V.

Further reduction of the bias current to reduce the error caused by partial bias current integration, drives the transistor deeper into the weak inversion region. In that case V_{WI}, and thus Δt, increases also, see (8) and (5). The negative effect of an increase in Δt on the accuracy of the rectifier will be larger than the effect of partially integrated bias current. This is due the fact that the bias current is already very small.

The bias voltage at the input of the rectifier is 0.1 V (V_{WI}) below the threshold voltage of the input transistors. In the given technology this is 0.6 V. The input voltage of the rectifier is also the output voltage of the OTA. It the next paragraph it will turn out that 0.6 V is a too low bias voltage to guarantee operation of the output transistors of the OTA in the saturation region. Therefore the bias input voltage of the rectifier is lifted up as shown Fig. 6(b).

There is still another problem with the circuit of Fig. 6(a). The integrating capacitor must be external to the chip and referred to ground. This is a "customer requirement" that could not be changed during the design. Normally an external capacitor of 100 pF is used when the input frequency is 10 MHz and the number of integrated periods is four. The maximal output voltage is 1 V.

To integrate the current on the external capacitor a current mirror is used, see Fig. 6(b). The integrated output voltage is given by

$$V_{out} = \frac{1}{C}\int_0^{nT}\left|I_{rect}\sin\left(\frac{2\pi}{T}t\right)\right|dt = \frac{2}{\pi C}nTI_{rect} \tag{10}$$

where T is the period of the input signal, N is the number of integrated periods, and I_{rect} is the amplitude of the rectified current.

When the maximal output voltage must be 1 V, n is 4 and T = 1/10 MHz, the rectified current must be equal to 400 μA. The rectifier could be designed for a maximal input current of 400 μA but this will lead to a large voltage swing or a large capacitance at the input. A larger input current for the rectifier requires a larger transconductance, and thus a larger power consumption, for the OTA. Therefore the input current is chosen to be 100 μA and a current mirror with a current gain of 4 is used. The bias current is not chosen smaller than 100 μA because then the ratio between the maximum input current and the bias current becomes too small. This would increase the relative error caused by partial bias current integration as discussed above.

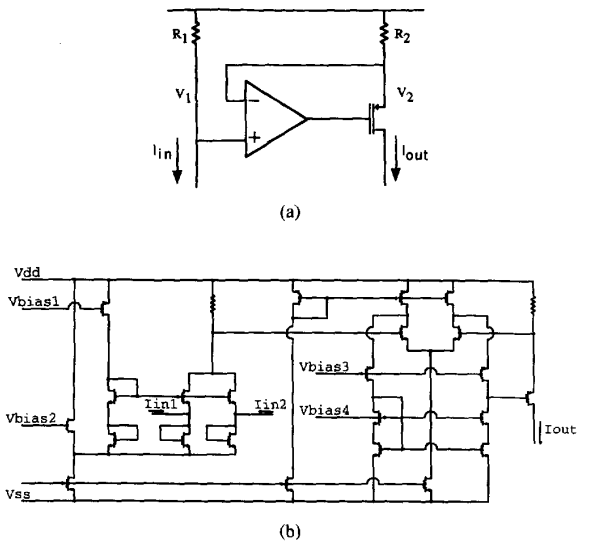

Fig. 7. (a) Principle diagram of a very linear current mirror. (b) Complete circuit diagram: the rectifier followed by a very linear current mirror.

When a simple current mirror is used in the integrator, see Fig. 6(b), the linearity of the system is completely degraded by VT mismatch between the mirror transistors. This is illustrated with the simulation results in Table II. The accuracy of the rectifier-integrator without VT mismatch is 10 b. It degrades to 7.1 b for only 10 mV of VT mismatch.

An alternative type of current mirror is implemented on the chip. Its principle is given in Fig. 7(a). The voltage across both resistors in Fig. 7(a) is kept equal by the opamp. Therefore the current gain is determined by the ratio of these resistors as shown in (11).

$$\begin{aligned} V_1 &= V_2 \\ R_1 I_{in} &= R_2 I_{out} \\ \frac{I_{out}}{I_{in}} &= \frac{R_1}{R_2}. \end{aligned} \tag{11}$$

The effect of offset in the opamp on the output current of the mirror is calculated as follows:

$$\begin{aligned} V_1 &= V_2 + V_{OFFSET} \\ R_1 I_{in} &= R_2 I_{out} + V_{OFFSET} \\ I_{out} &= \frac{R_1}{R_2} I_{in} + \frac{V_{OFFSET}}{R_2}. \end{aligned} \tag{12}$$

The last term for I_{out} in (12) is the error on the output current due to the offset voltage of the opamp. This error does not depend on the input current so it will not affect the linearity of the current mirror.

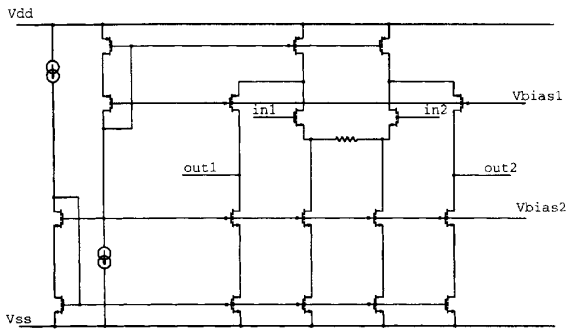

Fig. 8. Schematic diagram of a folded cascode OTA.

The full circuit diagram of the rectifier-integrator is given in Fig. 7(b). The opamp in the current mirror is implemented with folded cascodes to combine a large dc gain, sufficient GBW and a low power supply voltage.

V. Design of the OTA Driving the Rectifier-Integrator

A. A Folded Cascode OTA

As high input frequencies and a low supply voltage are to be combined, the design of the OTA is started with a folded cascode OTA, see Fig. 8. The current mirrors in the OTA are expanded with two extra transistors. The first one is a cascode to increase the mirror's output impedance. At the input a transistor with the same sizes as the cascode and the same voltage at its gate is added. This increases the accuracy of the current mirror as the drain source voltage of the mirror transistors will always be equal. To increase the linearity of the OTA the sources of its differential pair are degenerated.

To achieve the desired accuracy, the circuit is designed for third order distortion (HD3) less then 0.3%. Higher order distortion is neglected. HD3 of 0.3% gives 0.1% nonlinearity on the integrated current. The reason for this attenuation of the nonlinearity in the OTA is explained in the next deduction.

The output signal in the presence of harmonic distortion of order h and relative amplitude d is given by

$$V_{out} = \int_0^{T/2} \left| \sin\left(\frac{2\pi}{T}t\right) + d\,\sin\left(h\frac{2\pi}{T}t\right)\right| dt. \quad (13)$$

Assuming that the distortion d is much smaller than one, the integral can be calculated as

$$V_{out} = \frac{T}{\pi}\left\{1 + \frac{d}{2h}\left[1 - \cos(\pi h)\right]\right\}. \quad (14)$$

When h is even the effect of harmonic distortion cancels out completely. When h is odd, the effect of the distortion is attenuated with a factor h. When harmonic distortion with order higher than three is neglected, 0.3% HD3 distortion is sufficient to get an overall accuracy of 0.1%.

The third order harmonic distortion of the OTA is given by

$$\mathrm{HD3} = \frac{(V_{GS} - VT)V_p^2}{4(IR_s)^3} \quad (15)$$

where

V_p is the peak amplitude of the differential input signal;
I is the bias current of a single transistor in the differential pair;
$V_{GS} - VT$ is the overdrive of the differential pair;
R_s is the degeneration resistor of the differential pair.

The transconductance is determined by the ratio of the maximum input voltage and the maximum output current of the OTA: 200 μS. Therefore R_s equals 5 kΩ. Using (15) the transistors of the differential pair in the OTA can be calculated. The sizing of the other transistors is then straightforward.

The problem with the OTA of Fig. 8 is its output impedance. The output conductance and the output capacitance are too high. The output conductance causes an error because it gives rise to a nonlinear loss of current at the output of the OTA. The voltage at the output of the OTA, and thus the current through the output conductance of the OTA, depends nonlinearly on the output current of the OTA. The current through the output conductance of the OTA is not integrated at the output of the rectifier. Therefore a high-output conductance for the OTA affects the linearity of the system. The effect of a high capacitance at the output of the OTA was discussed in paragraph 3.

B. Cascode Boosting

Both, the output conductance and the output capacitance, can be decreased by means of cascode boosting. The principle of cascode boosting is given in Fig. 9(a) [3]. The resulting output conductance is given by

$$g_{out} = \frac{go}{(1+A)\left(1 + \dfrac{gm_{cascode}}{go_{cascode}}\right)} \quad (16)$$

where A is the open loop gain of the boost amplifier and go is the conductance "shielded" by the boosted cascode.

The output capacitance, when A is sufficiently large, can be approximated by

$$C_{out} = C_{db,\,cascode} + C_{gd,\,cascode}\left(1 + \frac{go_{cascode}}{gm_{cascode}}\right) \quad (17)$$

The output impedance of the OTA is dominated by the output impedance of the pMOS transistors at its output. This is due to the fact that the given technology is of the n-well type. The output capacitance of the OTA without cascode boosting, is 310 fF, 205 fF coming from the pMOST. The output conductance is 1 μS, 0.8 μS coming from the pMOST. Therefore only the pMOS cascodes at the output of the OTA will be boosted.

The output capacitance C_{out} of the boosted cascode is dominated by the drain-bulk capacitance of the boosted cascode transistor. Therefore the size of this transistor is reduced compared to the unboosted cascode, keeping its W/L ratio constant. In that case the transconductance of the cascode stays

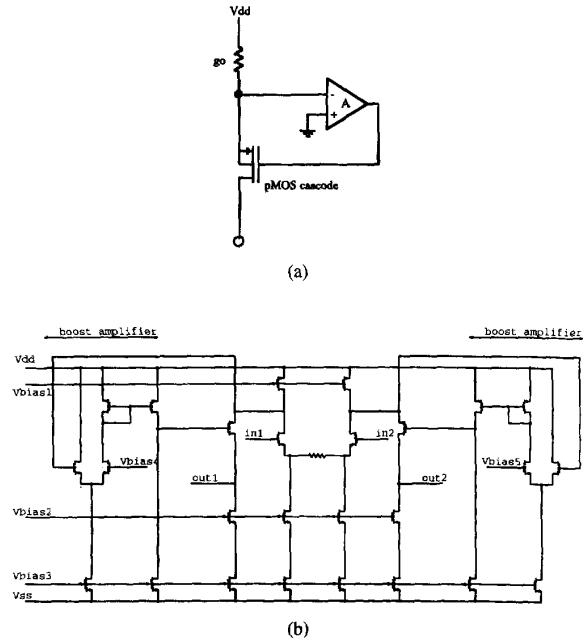

Fig. 9. Schematic diagram of a folded cascode OTA with boosted pMOS cascodes.

constant but its output conductance increases. A decrease of $go_{cascode}$ has two side effects. First, the g_{out} of the boosted cascode will increase, see (16). This is no harm because, as long as the gain A of the boost amplifier is high, the output conductance of the OTA will be determined by the output conductance of the nMOS cascode at the output of the OTA. The output conductance of that nMOST is 0.2 μS. Second there will be a minor increase in the output capacitance of the cascode because the second term in (17) will be slightly larger. This can be neglected because the first term in (17) is much larger than the second one and because $go_{cascode}/gm_{cascode}$ will be smaller than one even when the size of the cascode is reduced.

The schematic diagram of the OTA with boosted cascodes is given in Fig. 9(b). The boosting amplifiers are implemented with a differential pair. The stability of the boost loop was calculated. It shows that the loop is stable with only the parasitic capacitance at the gate of the boosted cascode as compensation capacitance. Other topologies for the boosting amplifier are possible. However, most of them are very hard to bias when the power supply voltage is only 3 V.

C. Offset Calibration

In spite of all design steps described above, there is still one major source of inaccuracy left in the system: offset in the output current of the OTA. In that case the output currents of the OTA can be described as

$$\begin{aligned} i_1(t) &= I_{OFFSET,1} + I\sin(\omega t) \\ i_2(t) &= I_{OFFSET,2} + I\sin(\omega t). \end{aligned} \tag{18}$$

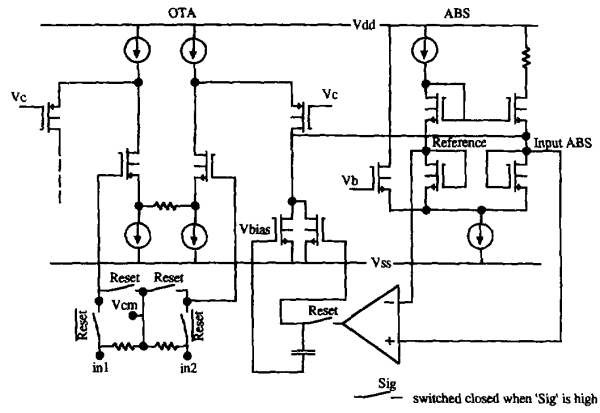

Fig. 10. Principle diagram of the automatic offset calibration system.

The rectifier-integrator takes the positive part of each of these currents and integrates it. Assuming a perfect linearity for the OTA and the rectifier, the integrated output voltage is given by

$$V_{out} = \frac{nTI}{C_{int}\pi} \cdot \left\{ \begin{array}{l} \sqrt{1-\left(\frac{I_{OFFSET,1}}{I}\right)^2} + \frac{I_{OFFSET,1}}{I} \\ \quad \cdot \left[a\sin\left(\frac{I_{OFFSET,1}}{I}\right) + \frac{\pi}{2}\right] \\ + \\ \sqrt{1-\left(\frac{I_{OFFSET,2}}{I}\right)^2} + \frac{I_{OFFSET,2}}{I} \\ \quad \cdot \left[a\sin\left(\frac{I_{OFFSET,2}}{I}\right) + \frac{\pi}{2}\right] \end{array} \right\}. \tag{19}$$

When (19) is evaluated with $I_{offset,1} = I_{offset,2} = 1$ μA it shows that the error on the output voltage is almost constant for a large input current. In that case, the linearity of the system is not influenced. For a small input current the error increases and the linearity decreases. This allows to conclude that the offset currents of the OTA will decrease the range over which a certain accuracy is realized. Starting from (19) it was calculated that for offset currents 1 μA, an accuracy of 0.1% is realized for input currents above 5 μA. When the offset current is 2 μA the input current must be above 17.5 μA to realize 0.1% accuracy. Offset currents of 5 μA or even higher are reasonable when the chip is actually implemented. Therefore an offset compensation system is required.

The offset current is trimmed by adjusting the output voltages of the OTA with two feedback loops. One of these loops is shown in Fig. 10. (For now ignore the switches in Fig. 10, assume that the Reset signal is high.) When the offset current of the OTA is zero, the input voltage of the rectifier branch, which is also an output voltage of the OTA, will be equal to the reference voltage. The feedback loop guarantees this condition: the bias current of the OTA is adjusted to minimize the difference between the output voltage of the OTA and the reference voltage. Therefore the feedback loop minimizes the offset in the output current of the OTA.

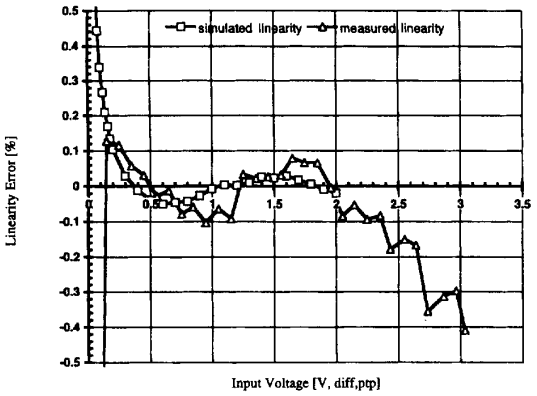

Fig. 11. Comparison of simulated and measured results for the amplitude detector's linearity.

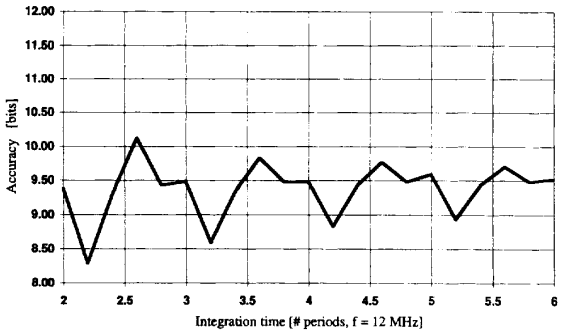

Fig. 12. Accuracy of the amplitude detector for different numbers of integrated periods.

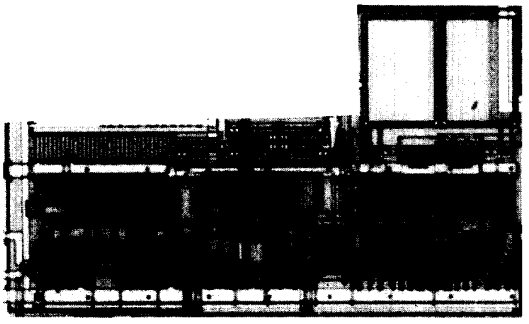

Fig. 13. Microphotograph of the servo amplitude detector chip.

The switches in Fig. 10 solve the following problem. The dc voltage at the input of the rectifier does not only depend on the bias current but also on the signal current. This is due to the non linear relationship between the signal current and the voltage swing it causes at the input of the rectifier. Therefore, if the offset compensating feedback loops operate continuously, the offset will adjust to an input signal dependent value. This might even increase the offset.

To avoid this effect the loops are operated in a switched mode: the offset is trimmed only during the reset time of the integrator. During that reset-time the input signal of the OTA is switched off and the feedback loops are allowed to perform their offset compensating action. Just before the integrator has to become active again, the input signal is switched on again. At that time the operation of the feedback loops is stopped and the bias currents of the OTA are frozen to their regulated value.

The stability of the offset compensating feedback loops is no problem because it is stabilized by the large capacitor (20 pF) required to store the regulated values when the operation of the feedback loops is disabled. The input stage of the opamps in the feedback loops was kept very small to reduce the capacitance it adds to the input of the rectifier.

VI. Results

The simulated linearity of the system is given in Fig. 11. The simulated accuracy is 0.2% when the input voltage ranges from 1/9 of full range to full range. The input frequency is 12 MHz. This meets the specifications of Table I.

The circuit was also simulated taking a variety of technological deviations into account: offset voltages in the opamps in the offset compensating feedback loops, offset in the opamp of the special current mirror, mismatches between the transistors in the rectifier, etc. These deviations give rise to a certain degradation of the accuracy but the accuracy specification is never endangered.

At last the accuracy of the system was simulated when the number of integrated periods changes. The results are plotted in Fig. 12. The accuracy is worse when the number of integrated periods is not a multiple of 0.5. This is due to the fact that the attenuation of the errors caused by harmonics is less in that case. However when the number of integrated periods is larger than four the accuracy specification is never threatened.

The system was implemented in standard 1 μ CMOS. For the resistors normal poly-interconnect was used. This allows to realize the chip without need for special analog modules in the technology. A microphotograph of the chip is given in Fig. 13.

The measured linearity is also plotted in Fig. 11. The measured accuracy is 0.2% for input voltages ranging from 1/8 of the full range to full range. The input frequency is 12 MHz. The measured accuracy falls well within the target specifications. A comparison of the measurements to target specifications is given in Table I.

VII. Conclusion

An amplitude detector for the servo loops in a hard disk is presented. It is based on rectification followed by integration of the input signal. In contrast with classical peak detectors, the new amplitude detector is much less sensitive to signal impairments. By performing the rectification with a current rectifier driven by an OTA, the system can be implemented as an open loop system. This avoids the need of opamps with very high slew rate. Therefore the power consumption can be kept small.

The circuit consists of two half wave rectifiers driven by a fully differential OTA. To increase the output impedance of the OTA, a folded cascode OTA with boosted cascodes

is implemented. The rectifier is followed by a current mirror integrating the rectified current on a capacitor. To cope with technology spreading a very linear current mirror is used. For the same reason the system is expanded with an automatic offset compensation system.

The amplitude detector is realized in a standard 1 μ CMOS process. It operates from a single 3 V power supply. Its measured linearity is 0.2% (9 b) for input voltages ranging from $0.25V_{pp,differential}$ to $2V_{pp,differential}$.

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