1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS

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***Abstract*— 1-V power supply high-speed low-power digital circuit technology with 0.5-μm multithreshold-voltage CMOS (MTCMOS) is proposed. This technology features both low-threshold voltage and high-threshold voltage MOSFET's in a single LSI. The low-threshold voltage MOSFET's enhance speed performance at a low supply voltage of 1 V or less, while the high-threshold voltage MOSFET's suppress the stand-by leakage current during the sleep period. This technology has brought about logic gate characteristics of a 1.7-ns propagation delay time and 0.3-μW/MHz/gate power dissipation with a standard load. In addition, an MTCMOS standard cell library has been developed so that conventional CAD tools can be used to lay out low-voltage LSI's. To demonstrate MTCMOS's effectiveness, a PLL LSI based on standard cells was designed as a carrying vehicle. 18-MHz operation at 1 V was achieved using a 0.5-μm CMOS process.**

I. Introduction

A low-power design is essential to achieve miniaturization and long battery life in battery-operated portable equipment. Recently, there has been rapid progress in personal communications service (PCS) based on battery drives, including digital cellular phones, personal digital assistants, notebook, and palm-top computers. Future PCS will be more dedicated to multimedia systems, and thus the LSI's, the key component of the equipment, are desired not only for low-power consumption but also for higher signal or data processing capability [1], [2]. In order to promote this development, the demand for LSI designs achieving both low-power and high-speed performance should become stronger.

Lowering the supply voltage is the most effective way to achieve low-power performance because power dissipation in digital CMOS circuits is approximately proportional to the square of the supply voltage. From the point of view of applications to battery-powered mobile equipment, the supply voltage should be set at 1 V [1]. 1-V operation enables direct battery drive by a single Ni-Cd or Ni-H battery cell even taking the cell's discharge characteristic into account. This provides the smallest size and lightest weight equipment and eliminates the need for a power wasting dc-to-dc voltage converter.

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However, it is generally rather difficult to reduce the supply voltage to 1 V. The drastic degradation in speed is the largest problem. Although several studies of high-speed 1-V operating DRAM's have been reported [3], [4], they seem difficult to apply to general logic circuits because they assume stand-by node voltages throughout the entire circuit are predictable in memory LSI's, and utilization of the conventional layout CAD tool is thought to be difficult. Therefore, the development of novel circuit technology that achieves high-speed operation at a low voltage of 1 V with only a single battery drive and can be easily applied to random logic circuits is the key to developing the LSI designs for mobile equipment in the multimedia era.

This paper proposes just such a new 1-V high-speed circuit technology that is applicable to all digital CMOS circuits [5]. We call it multithreshold-voltage CMOS (MTCMOS). Its unique feature is that it uses both high- and low-threshold voltage MOSFET's in a single chip. In the next section, key issues in low-voltage operation are discussed. The MTCMOS technology and its main characteristics are described in Section III. In Section IV, layout schemes based on a standard cell and chip configurations are discussed. Finally, the performance of a PLL LSI designed and fabricated using a 0.5-μm CMOS process as a carrying vehicle for MTCMOS technology is shown in Section V.

II. Design Issues for Low Voltage CMOS Circuits

A. Low-Voltage Operation

Power dissipation in digital CMOS circuits is approximately expressed as

$$P \simeq C_L V_{dd}^2 f_{OP} \tag{1}$$

where C_L is the load capacitance, V_{dd} is the supply voltage, and f_{OP} is the operating frequency. According to this formula, lowering V_{dd} is the most effective way to reduce power dissipation because it is proportional to the square of V_{dd}. Fig. 1 shows the relation between power consumption and supply voltage. It is apparent that lowering V_{dd} contributes significantly to power reduction. Reducing supply voltage from the 3.3 V, widely used at present, to 1 V realizes about 1/10 the power dissipation. Certainly, scaling down C_L or f_{OP} in (1) also contributes to low-power operation. Decreasing capac-

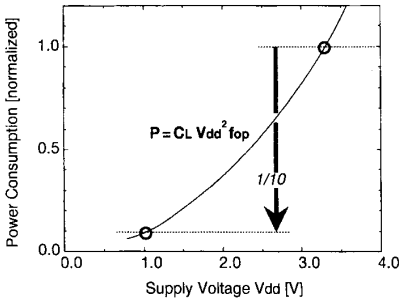


Fig. 1. Relation between power consumption and supply voltage.

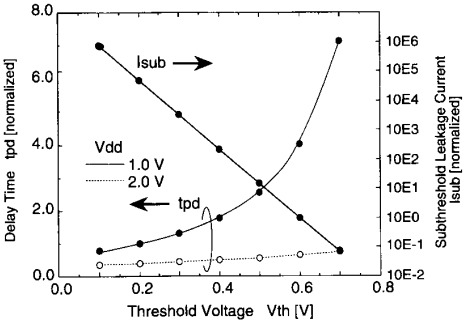


Fig. 2. Gate delay time and subthreshold leakage current dependence on threshold voltage.

itance C_L, however, would be difficult without scaling down the device and wiring, and higher throughput performance usually requires an increase in frequency f_{OP}. Although there have been attempts to lower f_{OP} by introducing parallel processing, this approach generally increases hardware overhead and requires extensive reworking at an architecture or algorithm design level [2].

B. Key Issue for Low-Voltage Operation

Although lowering V_{dd} to 1 V is effective in lowering power dissipation, as previously described, it is generally difficult because the speed performance is dramatically reduced at lower voltages. In CMOS digital circuits, the gate delay time (tpd) is approximately given by

$$tpd \propto \frac{C_L V_{dd}}{I_{DS}} \simeq \frac{C_L V_{dd}}{A(V_{dd} - V_{th})^2} \tag{2}$$

where C_L is the load capacitance, I_{DS} is the drain current in the saturation region, V_{dd} is the supply voltage, V_{th} is the MOSFET's threshold voltage, and A is a constant. In the above expression, lowering the supply voltage decreases I_{DS} proportional to the square of the voltage difference $V_{dd} - V_{th}$, which results in a drastic increase in gate delay time as V_{dd} approaches V_{th}.

Until now, supply voltage has generally been lowered by scaling down the device feature size to ensure the reliability of thin gate oxides [6], [7]. Speed performance is maintained even at low voltage due to the improvement in transconductance g_m brought about by shrinking feature size to a half or deep submicron size. Considering the increasing demand for extremely low-power operation, however, much lower voltage should be applied to devices in the same generation. In this case, a decrease in delay time at lower voltage must be achieved without relying on device feature size scaling.

One way to overcome the speed degradation problem is to reduce the V_{th} of a MOSFET, as seen clearly in (2). Fig. 2 shows the circuit characteristics dependence on V_{th}. As V_{dd} gets lower from 2 to 1 V, gate delay time tpd becomes more sensitive to V_{th}. Therefore, reducing V_{th} is effective to achieve high-speed operation at a V_{dd} of 1 V. As V_{th} is reduced, however, another significant problem emerges—a rapid increase in stand-by current due to changes in the subthreshold leakage current. Subthreshold leakage current of a MOSFET I_{sub} at $V_{GS} = 0$ is expressed as

$$I_{sub} \propto \exp\left(\frac{-V_{th}}{S/\ln 10}\right) \tag{3}$$

where V_{th} is the threshold voltage of a MOSFET, and S is subthreshold swing. Leakage current characteristics at a V_{dd} of 1 V are also shown in Fig. 2. These values are calculated assuming S is 85 mV/decade. As V_{th} is reduced by 0.1 V, I_{sub} becomes about ten times larger. This becomes the source of the large stand-by current. With respect to portable equipment, in particular, the stand-by period is generally much longer than the operating period. Therefore, an increased stand-by current wastes battery power seriously. That is why it has been difficult to satisfy the requirements for both high-speed and low stand-by power at a low supply voltage of 1 V.

III. MTCMOS Circuit Technology

A. Basic Circuit Scheme

The new MTCMOS circuit technology is proposed to satisfy both requirements of lowering the threshold voltage of a MOSFET and reducing stand-by current, both of which are necessary to obtain high-speed low-power performance at a V_{dd} of 1 V.

This technology has two main features. One is that N-channel and P-channel MOSFET's with two different threshold voltages are employed in a single chip. The other one is two operational modes, "active" and "sleep," for efficient power management.

Fig. 3 shows the basic MTCMOS circuit scheme with the NAND gates. The logic gate is composed of MOSFET's with a low threshold voltage of about 0.2–0.3 V. Its power terminals are not connected directly to the power supply lines VDD and GND, but rather to the "virtual" power supply lines VDDV and GNDV. The real and virtual power lines are linked by MOSFET's Q1 and Q2. These have a high threshold voltage of about 0.5–0.6 V and serve as sleep control transistors. Signals SL and $\overline{SL}$, which are connected to the gates of Q1 and Q2, respectively, are used for active/sleep mode control. Circuit operation in each mode at a supply voltage of 1 V is described below.

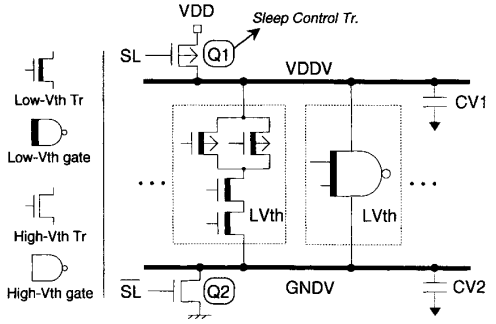
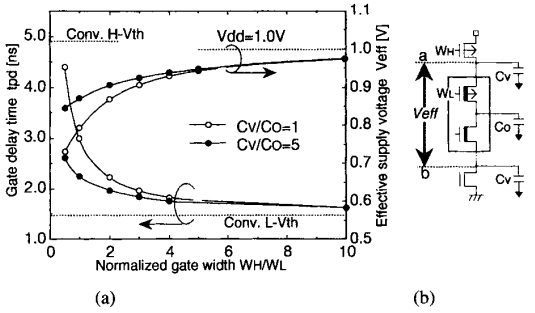


Fig. 3. MTCMOS circuit scheme.



(a) (b)

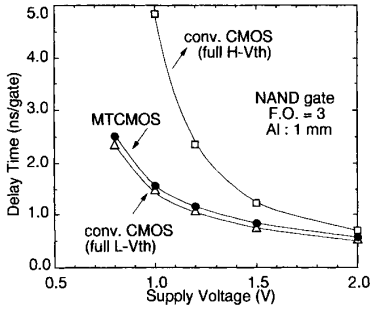
Fig. 4. Gate delay time and effective supply voltage dependence on the normalized gate width of the sleep control transistor. (a) Simulation results. (b) Simulation circuit model.

In the active mode, when SL is set low, Q1 and Q2 are turned on and their on-resistance is so small that VDDV and GNDV function as real power lines. Therefore, the NAND gate operates normally and at a high speed because the V_{th} of 0.3 V is low enough relative to the supply voltage of 1 V.

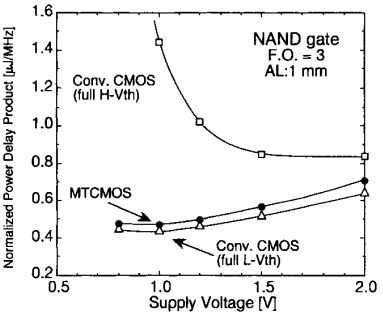
In the sleep mode, when SL is set high, Q1 and Q2 are turned off so that the virtual lines VDDV and GNDV are assumed to be floating. The relatively large leakage current, determined by the subthreshold characteristics of low-V_{th} MOSFET's, is almost completely suppressed by Q1 and Q2 since they have a high V_{th} and thus a much lower leakage current. Therefore, power consumption during the stand-by period can be dramatically reduced by the sleep control.

It should be pointed out that two other factors affect the speed performance of an MTCMOS circuit. One is the size of the sleep control transistors Q1 and Q2, and the other is the capacitances C_{V1} and C_{V2} of the virtual power lines. Q1 and Q2 supply current to the virtual lines. The larger their gate widths are designed, the smaller the on-resistance becomes. C_{V1} and C_{V2} also act as temporary supply sources to internal logic gates. Thus, the voltage rise in GNDV and drop in VDDV caused by the switching of the internal logic gate are suppressed by setting them large enough to maintain high-speed performance.

To confirm the effects, simulations were carried out. Fig. 4 shows the gate delay time *tpd* and effective supply voltage V_{eff} dependence on the normalized gate width of sleep control transistors W_H/W_L along with the simple single MTCMOS circuit model used for simulations, where V_{eff} is defined as the minimum value of spontaneous voltage difference between VDDV and GNDV (between node a and b in this simulation). It is clear that larger C_V, virtual line capacitance, and W_H, sleep control transistor width, maintain the effective supply voltage V_{eff} for the internal logic gates and enhance the speed performance. For instance, a W_H/W_L of 5 and C_V/C_O of 5 keep the decrease in V_{eff} within 10% of V_{dd} and the degradation in gate delay time within 15% compared to a pure low-V_{th} CMOS. The area penalty for the wider gate transistors is relatively small because they are shared by all the logic gates on a chip. As for C_V, the above condition is generally met in an actual LSI because C_V includes the source capacitances of all the logic gates connected to virtual power lines and wiring capacitances. Therefore, nothing extra need be added.



(a)



(b)

Fig. 5. MTCMOS performances. (a) Gate delay time. (b) Normalized power delay product dependence on supply voltage.

B. Electrical Performance

The measured MTCMOS logic gate delay time is shown in Fig. 5(a) as a function of supply voltage. Data for the conventional full high-V_{th} and full low-V_{th} CMOS logic gates are also plotted for comparison. It is obvious that the voltage dependence of an MTCMOS gate delay is much smaller than that of a conventional CMOS gate with high-V_{th} and that the MTCMOS gate operates almost as fast as the full low-V_{th} gate. At a 1-V power supply, the MTCMOS gate delay time is reduced by 70% as compared with the conventional CMOS gate with high-V_{th}. The dependence of normalized power-delay product (NPDP) on supply voltage is shown in Fig. 5(b),

TABLE I
CHARACTERISTICS OF MTCMOS CIRCUIT TECHNOLOGY

Power supply voltage	1.0 V
Propagation delay time	1.7 ns/gate
Power dissipation	0.3 μW/MHz/gate
	(2-input NAND with F.O.=3, line = 1 mm)

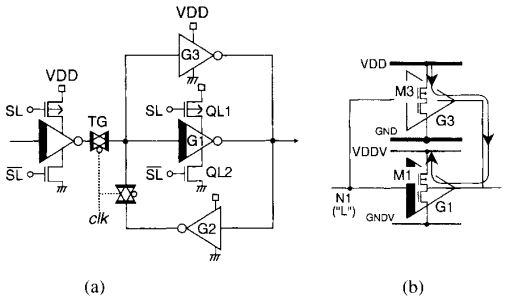


Fig. 6. MTCMOS latch circuit. (a) The proposed circuit. (b) The problem of the leakage current path.

where power consumption is normalized by frequency. At low voltages, especially below 1.5 V, the NPDP of the MTCMOS is much less than that of the conventional high-V_{th} gates, reflecting the improved speed performance at lower voltage. The smallest NPDP is achieved around 1 V in the MTCMOS gates. This shows that power reduction effect proportional to the square of supply voltage overcomes speed degradation in low-voltage operation. In addition, it was confirmed that the stand-by current was reduced three or four orders of magnitude due to the sleep control.

From these results, it is clear that MTCMOS circuit technology achieves both high-speed and low-power operations at a low supply voltage of 1 V or less. The measured characteristics related to this circuit technology are summarized in Table I. At 1 V, NAND gate delay time is typically 1.7 ns per gate, and power consumption is 0.3 μW/MHz per gate with a standard output load of three fanouts and 1 mm of wiring. MTCMOS gate operates about three times faster than conventional 0.5-μm CMOS gate. Power dissipation of 0.3 μW/MHz is 1/10 of the power needed for 3-V operation.

C. Design of Flip-Flop Circuit

Special attention must be paid to the MTCMOS design of latch or flip-flop circuits that have memory functions. This is because memorized data in latch or flip-flop circuits must be retained even in the sleep mode when virtual power lines are floating to cut leakage current completely. The proposed MTCMOS latch circuit is shown in Fig. 6(a), which is used for flip-flop circuits. The features are described below.

1) A conventional inverter G2 and a newly added one G3 are composed of high-V_{th} MOSFET's. They are connected directly to the true power supply lines VDD and GND. The latch path consists of G2 and G3, which are always provided with power. Therefore, data can be retained even in the sleep mode, when the clock signal CLK is fixed by using the sleep control signal SL. G3 is designed to be smaller to suppress both the increases in the gate delay time and the area.

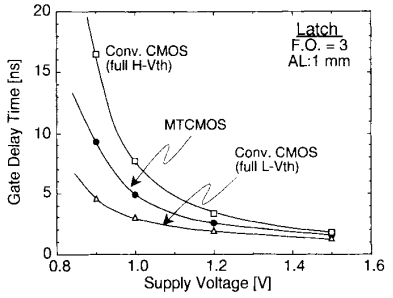


Fig. 7. Latch circuit delay time dependence on supply voltage.

2) As for the forward path, the inverter G1 and the CMOS-type transmission gate TG are composed of low-V_{th} MOSFET's. This makes high-speed operation possible at 1-V power supply. This circuit also includes local sleep control transistors QL1 and QL2 with high-V_{th}. The reason for including them can be understood with Fig. 6(b), where a node N1 is assumed to maintain a "low" state in the sleep mode. If G1 were connected directly to the virtual power line VDDV, as shown in this figure, VDD and VDDV would be short through M1 and M3, so that stand-by current would be increased in the sleep mode. Therefore, QL1 and QL2 are indispensable for completely cutting the leakage current path. Fig. 7 shows the simulation results for the delay time of the MTCMOS latch circuit. They confirm that the delay time is reduced by 50% at 1 V compared with that of the conventional circuit with high-V_{th}. Furthermore, the stand-by current in the sleep mode was also confirmed to be almost as low as that of the high-V_{th} circuit.

IV. CHIP LAYOUT SCHEME

In order to make this low-voltage technology practical, conventional CAD tools must be applicable to lay out an MTCMOS LSI easily without any special consideration of the particular circuit scheme. To meet this requirement, the MTCMOS standard cell library was developed.

Fig. 8 shows the MTCMOS layout scheme based on a standard cell. The main feature is that the extra components of the MTCMOS circuit are buried in the cells. More specifically, the virtual power supply lines (VDDV and GNDV) and the sleep control signal line (SL) are buried in each cell, while the sleep control transistors Q1 and Q2 with high-V_{th} are buried in the power supply cell that provides the area needed to connect the true and virtual power supply lines to each other in the x and y directions. Power supply cells are placed on both sides of the logic cell based core. The true power supply lines VDD and GND, which are also placed in each cell, fix the voltage of either the substrate or the well and supply current to flip-flop circuits. This layout scheme allows the extra MTCMOS components to be connected automatically throughout the chip by abutting cells with a minimum increase in chip area.

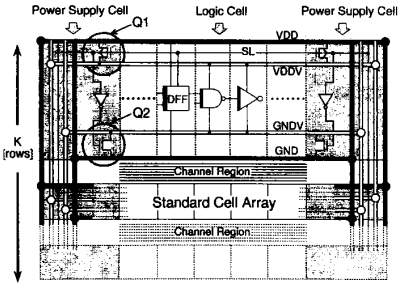


Fig. 8. Chip layout scheme based on a standard cell.

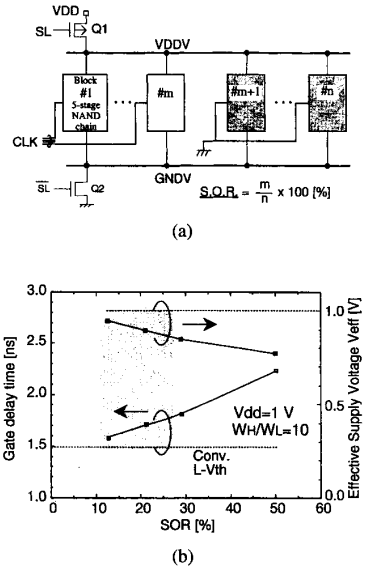


Fig. 9. Gate delay time and effective supply voltage dependence on Switch-On-Rate (SOR). (a) Simulation circuit model. (b) Gate delay time and effective supply voltage versus SOR.

Because Q1 and Q2 can be placed just under the power supply lines in the power supply cell, their insertion would incur no area penalty. Furthermore, the virtual power lines VDDV and GNDV in each row are connected together so that one cell can be supplied current through all the sleep control transistors within the chip, which contributes to suppress speed degradation.

In this experiment, W_H, the poly-gate width of sleep control transistors Q1 and Q2 in a power supply cell, was design to be ten times larger than that in the logic cells (W_L). Q1 and Q2 are shared by all the logic gates connected to the virtual power lines in this scheme. Therefore, the simultaneous switch-on rate (SOR), which indicates how many logic gates are switched on at almost the same time, seems to affect speed performance, especially in MTCMOS circuits. The amount of current supplied through Q1 and Q2 depends on the switching probability of the internal logic gates. Thus, a high SOR enhances the voltage drops at Q1 and Q2, which consequently reduces the effective supply voltage between VDDV and GNDV. Fig. 9 shows the simulation results for the SOR along

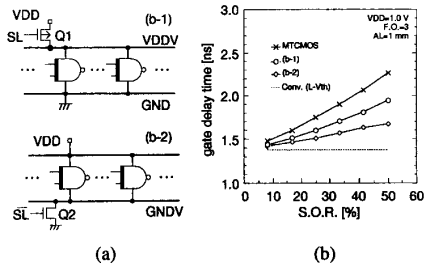


Fig. 10. Influences of virtual power supply lines. (a) Simulation circuit model. (b) Gate delay time versus SOR.

TABLE II
DEVICE TECHNOLOGY

	High-Vth Tr	Low-Vth Tr
Gate length	0.55 μm	0.65 μm
Gate oxide thichness	110 Å	110 Å
N-channel : Vth	0.55 V	0.25 V
P-channel : Vth	-0.65 V	-0.35 V

with the circuit model. Here, the SOR is defined as m/n, where m and n indicate the number of operating logic blocks and the total number of blocks, respectively, assuming a 2-mm block width. As the SOR increases, the voltage on VDDV drops because Q1 has to supply more current to VDDV at one time. For similar reasons, the voltage also rises on GNDV. These voltage changes cause the effective supply voltage V_{eff} between VDDV and GNDV to decrease, extending gate delay time. Generally, however, the SOR is expected to be at most 20 or 30%. In this region, the reduction of V_{eff} is less than 15% of the supply voltage, and the speed performance of 1.7 ns/gate is still quite high.

One way to further decrease the dependence of speed performance on the SOR is to use a sleep control transistor with a wider gate. This is, however, a trade-off between speed and stand-by current because total stand-by current in a chip is approximately given by $2KW_HI_H$. Here, K is the number of rows in the block shown in Fig. 8, while W_H is the gate width of the sleep control transistor, and I_H is its leakage current when the gate's width and length are equal. Another effective way to decrease this dependence is to remove one set of the two sleep control transistors and virtual power lines. The expected improvements in speed are shown in Fig. 10 along with simulation circuits. By removing of GNDV (b-1) and VDDV (b-2), gate delay time can be reduced by 15–25% compared with the basic scheme. The removal of VDDV is clearly more effective in increasing speed. The reason for this is that the threshold voltage of the P-channel MOSFET (Q1) was designed to be higher than that of the N-channel one (Q2) in this study (see Table II).

V. TEST CHIP RESULTS

A. Process and Device Technology

To confirm the effectiveness of MTCMOS circuit technology, a PLL LSI using new MTCMOS standard cells was

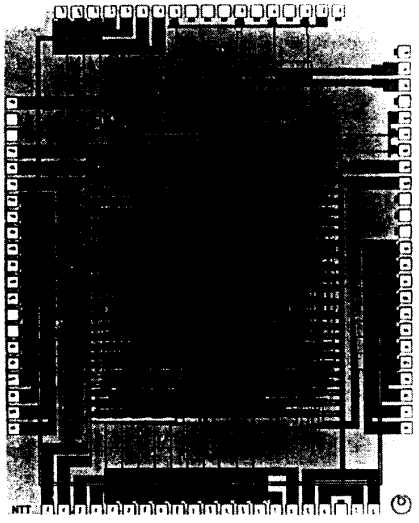


Fig. 11. Microphotograph of the PLL chip.

TABLE III
AREA PENALTY FACTOR

Combinational Circuit	1.1
Sequential Circuit	2.0
PLL LSI Digital Core	1.3

designed and fabricated. Conventional 0.5-μm CMOS process technology for 3.3-V operation with single-polysilicon and double-metal layers was used. MOSFET's with different V_{th}'s in the same well were formed by optimizing the impurity concentration in the well and controlling the channel doses with two additional masks, which minimizes the increase in the number of process steps. The key device parameters and characteristics are summarized in Table II. The gate length of the low-V_{th} MOSFET is 0.65 μm, which is 0.1 μm longer than that of the high-V_{th} ones. This is preferable to suppress variations in the threshold voltage due to short-channel effects. The gate oxide thickness is 110 Å for both types of MOSFET's. The low-V_{th}'s are 0.25 V for N-channel and -0.35 V for P-channel MOSFET's.

A microphotograph of the PLL chip is shown in Fig. 11. This chip consists of about 5 K gates, including the automatic frequency control circuit and the intermittent operation controller [8]. The whole chip is 4×5 mm^2, and the digital core is about 2×2 mm^2. Table III lists the area penalty factors in this study. An MTCMOS combinational circuit cell has an area about 10% larger than a conventional cell does owing to the insertion of virtual supply lines and the sleep control line. A sequential circuit cell, such as an MTCMOS DFF with clear, needs an area about twice that of a conventional cell in order to store data even in the sleep period. The area increase for the whole digital core, however, is only 30% in spite of the fact that the DFF's occupy a relatively large part (about 50%) of the total gate counts. This is because the channel area is almost unchanged. Moreover, because all DFF's in an actual LSI aren't expected to hold the date during sleep period, the area penalty can be further reduced by appropriately combining the use of a conventional DFF and the DFF with a special memory function.

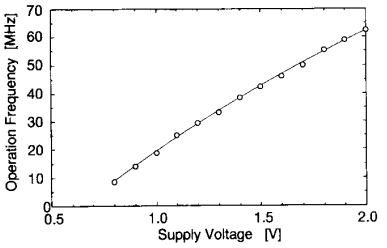


Fig. 12. Operation frequency of the PLL chip.

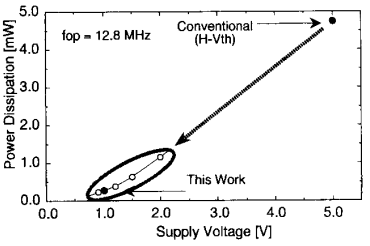


Fig. 13. Power dissipation of the PLL chip versus supply voltage.

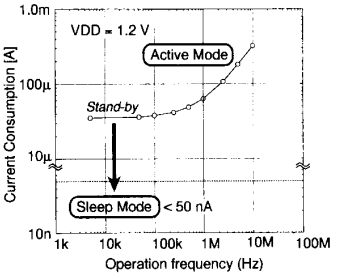


Fig. 14. Power dissipation of the PLL chip versus operation frequency.

B. Chip Performance

Fig. 12 shows the measured operation frequency as a function of supply voltage. At 1 V, the chip operates at 18 MHz which is sufficient for many applications.

Fig. 13 shows the power dissipation in the digital core as a function of supply voltage at an operation frequency of 12.8 MHz. The power dissipation of the conventional 5-V operation PLL is also plotted for comparison. At 1 V, power dissipation is drastically reduced to below 1/20 compared with that of the conventional LSI operated at 5 V.

Fig. 14 shows another aspect of the power performance—the operating current versus the operating frequency for the worst case at a supply voltage of 1.2 V. Although the operating current is proportional to the frequency in the region over 1 MHz, it becomes almost constant in the low-frequency region. This is due to the leakage current caused by using low-V_{th} MOSFET's. In the active mode, the leakage current of about 30 μA in this chip is negligible because it is less

TABLE IV
CHARACTERISTICS OF THE PLL CHIP

Power supply voltage	1.0 V
Core size	2.4 mm x 2.3 mm
Cycle frequency	18 MHz
Power dissipation	200 μW (at 10 MHz)
Stand-by current	< 50 nA
Turn-on time	< 500 ns
Gate counts	5 K gates

than 1/10 of the dynamic current consumption at a desired operating frequency of over 10 MHz. In the sleep mode, on the other hand, the current is dramatically reduced to below 50 nA, so that low stand-by characteristics can be obtained.

Typical PLL LSI features are summarized in Table IV. The turn-on time, which is the time needed to switch from sleep to active mode, is less than 500 ns even in the worst case.

VI. CONCLUSION

Multithreshold-voltage CMOS (MTCMOS) circuit technology has been proposed as a way to achieve a 1-V supply voltage high-speed and low-power LSI operation. This technology uses MOSFET's with two different threshold voltages on a single chip and introduces a sleep control scheme for efficient power management. Low-threshold voltage MOSFET's improve the speed performance at a low supply voltage of 1 V, while high-threshold MOSFET's suppress the stand-by power dissipation. In addition, a standard cell library has been developed to simplify low-voltage LSI designs. To demonstrate the effectiveness of this technology, a PLL LSI based on standard cells was designed as a carrying vehicle using a 0.5-μm CMOS process. High-speed operation of 18 MHz at 1 V confirmed the validity of this new technology.

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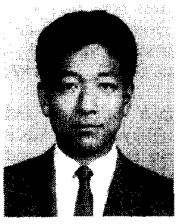

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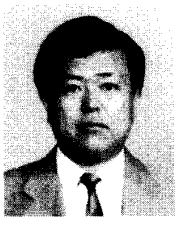

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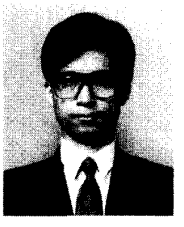

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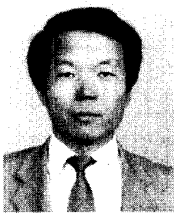

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