Principle and Applications of an Autocharge-Compensated Sample and Hold Circuit

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***Abstract*— This paper describes an autocharge-compensated sample and hold circuit (ACC-SH) for thin film transistor active matrix liquid-crystal displays (TFT-AM-LCD's, TFT-LCD's, or LCD's). The operating principle and actual application problems for TFT-LCD's are also discussed. The applicability of the ACC-SH is verified not only by circuit simulation but also by experimental circuit die measurement.**

I. Introduction

LIQUID-CRYSTAL displays (LCD's) are widely used in TV and computer terminals. Fig. 1 shows the configuration of an LCD module composed of an LCD panel, video signal driver IC's (driver IC's), and a scanning-line controller. Just as with a CRT display, visual information in the form of RGB signals is scanned from left to right. The scanning line is selected by the scanning line controller. The visual information in one horizontal line scanning time is divided and segmented by many driver IC's. The driver IC contains massive parallel sample and hold (S/H) circuits. Each pixel of the LCD panel is composed of a TFT switch and a liquid crystal cell that are also electrically equivalent to a S/H circuit. Comparing these two kinds of S/H circuits, severe performance is not normally demanded of the S/H circuit in each pixel. If the S/H circuit in each pixel shows some deviations, which are random in nature, the human visual information processing system compensates for such deviations. On the other hand, the circuit in the driver IC is responsible for all of the pixels in one column. The deviations are correlated, and the person watching the display perceives such deviations.

A S/H circuit comprising a CMOS switch and a capacitor is a candidate for such a driver IC because of its simple configuration. However, increasing the −3-dB cut-off frequency of the series CMOS switch and capacitor by widening the CMOS switch or reducing the capacitor increases the sampled offset pedestal. Many techniques have been reported to overcome this problem [1], [2]. Conventional approaches are reviewed in Section II.

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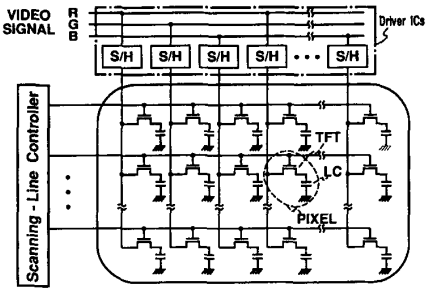


Fig. 1. TFT-LCD module.

The requirements for such a S/H circuit are as follows: 1) sampling frequency $f_{S/H}$, which is determined by

$$f_{S/H} = \frac{\text{number of horizontal pixels}}{\text{horizontal line scanning time}} \tag{1}$$

where no parallel processing is assumed, 2) 5-V full-scale operating range to control LC transparency, 3) wide signal bandwidth, 4) low output offset standard deviation both within a chip and between chips, and 5) simple configuration. These specifications are discussed in Section III.

An autocharge-compensated sample and hold circuit (ACC-SH) that will reduce conventional drawbacks is proposed in this paper. In Section IV, the principle of operation of the proposed S/H circuit is described. In Section V, design considerations for developing the LSI are discussed. Some experimental results are presented in Section VI.

II. Conventional Approaches

To define the problems that must be solved, a few conventional techniques are reviewed. Fig. 2(a) shows the S/H circuit composed of a sample switch and a hold capacitor, where the switch is an N-channel MOS transistor. When the circuit is in sample mode, the transistor is turned ON, and charge Q_c is accumulated in the inversion layer that is located beneath the gate electrode. In hold mode, the transistor is turned OFF, and the input signal is held. At the moment, the input signal is held, channel charge Q_c is split and flows out from the source and drain terminals. Some of the charge is injected to the hold capacitor and is added to the signal charge Q_{signal}. The split and additional charge is called the offset pedestal

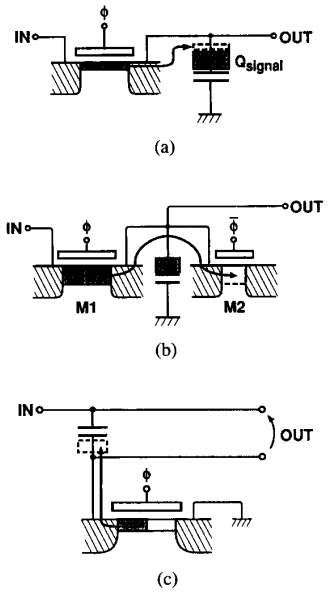


Fig. 2. Conventional S/H circuits. (a) Basic structure. (b) Use of compensation transistor. (c) Wooley's S/H circuit.

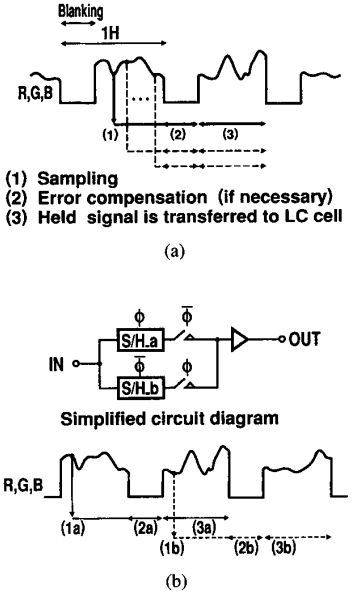


Fig. 3. The role of a S/H circuit for TFT-LCD. (a) Time schedule. (b) Actual time schedule.

of the S/H circuit. (Note that the offset pedestal includes coupling from the gate overlap capacitors. Channel charge is emphasized in this discussion.) Channel charge accumulated on the capacitor shows input voltage dependent nonlinear characteristics because of the operating mechanism of the MOS transistor.

Many techniques exist for reducing the effect of MOS transistor channel charge. Fig. 2(b) and (c) illustrates two such techniques. For effective offset cancellation, the size of M2 in Fig. 2(b) is selected to be half of M1. The circuit shown in Fig. 2(c) does not cancel channel charge itself, but the channel charge effect never shows input voltage dependent nonlinear characteristics because the switch transistor operating point is independent of the input signal [2]. Concerning the application of the S/H circuit for the driver IC, offset deviation should be minimal because more than ten chips are used in an LCD panel.

III. Specification of the Driver IC

A. Specific Specification

The S/H circuit is normally used for quantizing the continuous incoming signal in the time domain. Normally, the S/H circuit functions, which include S/H operation and the inherent error compensation, must be completed during the sampling interval. The S/H circuit described here is not necessarily restricted by such a severe error compensation interval. Fig. 3(a) shows the role of the S/H circuits for the driver IC. Two parallel S/H circuits are driven in turn as shown in Fig. 3(b). In one horizontal interval, the even set of S/H circuits is in sample mode, and the odd set of the S/H circuits is in hold mode. The blanking interval can be used to compensate

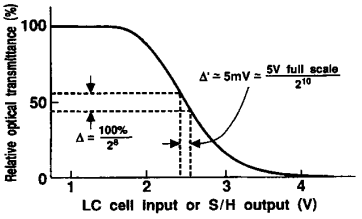


Fig. 4. Relative optical transmittance characteristics.

the S/H circuit's inherent sampling error. For example, in the case that the driver IC's are applied to a workstation display, an error compensation time of a few microseconds is permitted for the S/H circuit.

B. Accuracy Requirement and Operating Range

The relation between the LC cell input and the LC cell optical transmittance is important for specifying the S/H circuit held signal accuracy requirement. Fig. 4 shows relative LC transparency characteristics. The LC cell input in the horizontal axis is equivalent to the output of the S/H circuit. In the vertical axis, 0% represents black and 100% represents white. This figure also shows that a 5-V full-scale operating range is required to control LC transparency.

IV. Principle of Operation of the Proposed ACC-SH

A. Phenomenon of Channel Charge Split

Channel charge split is a dynamic phenomenon. To examine this phenomenon, the test circuit shown in Fig. 5(a) was fabricated for measuring this effect [3]. The experimental

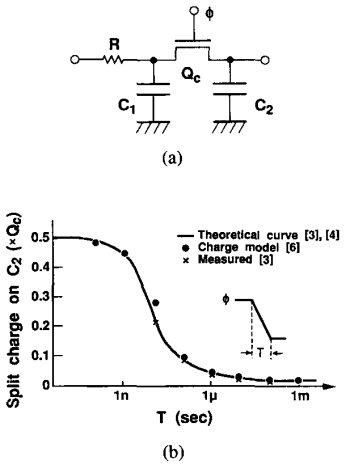


Fig. 5. Channel charge split phenomenon. (a) Test circuit. (b) Measured and simulated results.

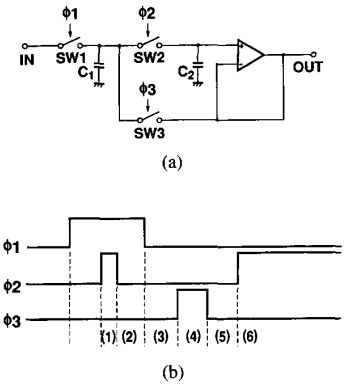


Fig. 6. ACC-SH. (a) Circuit diagram. (b) Switch control sequences, where 1) SW1 and SW2 are ON, both capacitors charge to IN, 2) SW2 turns OFF (SW1 is still ON), $\frac{1}{2}$ SW2 charge is injected to C_2, 3) SW1 turns OFF, $\frac{1}{2}$ SW1 charge is injected to C_1, 4) SW3 turns ON, V_{C_1} matches V_{C_2}, 5) SW3 turns OFF, leaving $V_{C_1} \approx V_{C_2}$, 6) SW2 turns ON, $\frac{1}{2}$ SW1 charge on C_1 returns to SW2.

results in Fig. 5(b) show the characteristics of the channel charge split ratio. Split channel charges are accumulated on capacitor C_1 and C_2, where C_2 is a hold capacitor, and C_1 is connected to a low impedance input voltage source through resistor R. The fabricated test chip characteristics are as follows: fabrication process is 0.8-μm CMOS, capacitors C_1 and C_2 are both 10 pF, the switch transistor gate length is 6.4 μm, and the gate width is 320 μm. The reason a 6.4-μm-long channel gate is used is that the coupling effect from the gate should be relatively small, and a large transistor is used to improve measured data accuracy. In Fig. 5(b), R is set to about 0 Ω. The parameter of this experiment is the fall time T of the switch control signal. The graph shows that if the fall time is long, such as when T is equal to 1 ms, almost all of the channel charge returns to the input voltage source, and very little charge remains on C_2. However, if very quick switching is possible, such as when the fall time is less than 1 ns, exactly half of the channel charge flows to capacitor C_2 and $\frac{1}{2}Q_c$ stays on C_2.

The channel charge-splitting phenomenon is analyzed in [4]. Analytical results predict that the channel charge split ratio is close to 0.5, if the term

$$V_{pp}\sqrt{\frac{\beta T}{C_2}} \tag{2}$$

is small enough, where $\beta = \mu C_x \frac{W}{L}$, μ is mobility, C_x is oxide capacitance per unit area, W is the transistor width, and L is the transistor length. This analysis supports the experimental data [3] and the circuit simulation model in Fig. 5. The circuit operation described later is verified by this charge-oriented MOS transistor model [5], [6].

B. Principle of Operation

The ACC-SH in Fig. 6 consists of a conventional S/H circuit, a buffer amplifier, two additional switches, and one additional capacitor. The ACC-SH can compensate two different types of offset pedestals. One is caused by the switch transistor channel charge, and the other is caused by the overlap capacitors of the transistor.

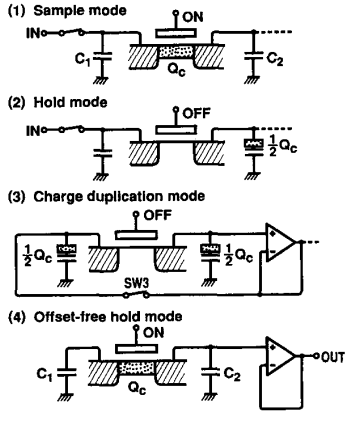


Fig. 7. ACC-SH operations to reduce the effect of channel charge.

Fig. 7 shows the detailed operating mechanism for compensating the offset pedestal in the ACC-SH, where the buffer amplifier is ideal, and the switches are the N-channel MOS transistors. Signal charge Q_{signal} is neglected, and offset charge is emphasized. In sample mode, channel charge Q_c is generated beneath the gate electrode of the switch transistor. In hold mode, the inversion layer vanishes and channel charge leaves the channel. At the beginning of this hold mode, half of the channel charge $\frac{1}{2}Q_c$ is injected to C_2, while the other half returns to the input voltage source. This phenomenon is supported by the experiment previously described. $\frac{1}{2}Q_c$ is the undesirable offset pedestal of the S/H circuit. The buffer amplifier and SW3 are used in charge duplication mode. The voltage across C_2 is sensed and transferred to C_1 through the buffer amplifier and SW3. If C_1 equals C_2, charges accumulated on C_1 and C_2 are also forced to be equal. $\frac{1}{2}Q_c$

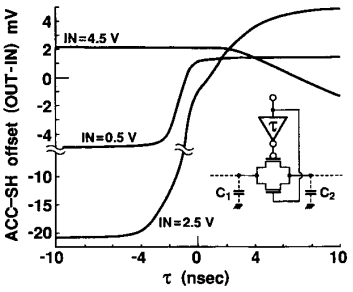


Fig. 8. Simulation of the effect of τ on offset.

on C_2 is duplicated on C_1. The final mode is offset-free hold mode. At the beginning of this mode, the transistor is turned ON again, and the transistor absorbs charge for reforming the channel. The required charge in the reformed inversion layer is Q_c because the operating point of the switch transistor returns to the operating point at the beginning of hold mode. Half of Q_c comes from the source terminal, and the other half comes from the drain terminal. Charges on C_1 and C_2 are completely absorbed into the transistor channel, and the offset pedestal becomes nearly zero.

The offset caused by the gate signal feed-through is also compensated during the above procedure. Because the state of SW2 moves from ON to OFF and back to ON, the final state of SW2 is equal to its initial state, and the offset caused by the gate signal feed-through is cancelled in offset-free hold mode.

V. Design Considerations

In this section, the ACC-SH design considerations that are encountered during the circuit design stage are discussed.

A. CMOS Switch

In the fabricated LSI, the switches are realized by CMOS. In the case that CMOS switches are used in the ACC-SH, the following inherent problems arise. One problem is whether the N-channel MOS transistor or the P-channel MOS transistor is dominant in the CMOS switch. If the input voltage is high, e.g., 4.5 V, mainly the P-channel MOS transistor operates, and the N-channel MOS transistor does not conduct. On the other hand, if the input voltage is low, e.g., 0.5 V, mainly the N-channel MOS transistor operates. In these two cases, the operating scheme in the ACC-SH is successfully applied. However, the difficulty occurs when the input voltage is about 2.5 V, when both transistors are active. The other problem is that the channel charge behavior depends on two applied sampling pulses ϕ and $\bar{\phi}$ for each transistor of the CMOS switch. The difference τ between the delay times of ϕ and $\bar{\phi}$ varies within a chip. The charge-oriented MOS transistor model is used for simulation. The simulated results in Fig. 8 indicate that the switching time difference must be less than 2 ns for the 4 mV peak-to-peak output offset to be attained. It is not difficult to realize such an inverter delay time difference. Therefore, CMOS switches are used in the ACC-SH. An example of a ϕ and $\bar{\phi}$ signal generator is shown in Fig. 9, which satisfies the above specification.

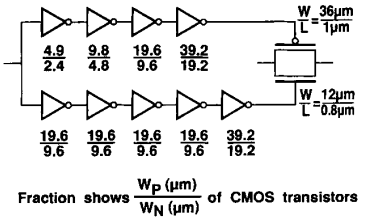


Fig. 9. $\phi, \bar{\phi}$ signal generator for CMOS switch.

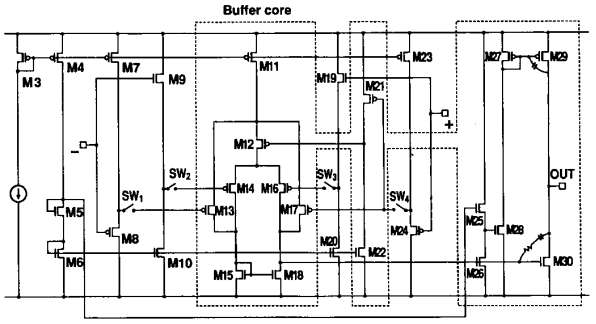
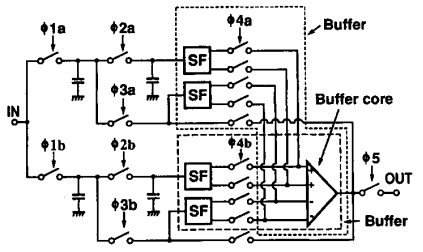


Fig. 10. Schematic diagram of the buffer amplifier.

B. Buffer Amplifier

The unity gain buffer amplifier used is a two-stage amplifier as shown in Fig. 10. The input stage consists of two pairs of P-channel and N-channel source followers M7, M8, M23, M24, and M9, M10, M19, M20, respectively, and one pair of inside and outside differential transistors M14, M16, and M13, M17, respectively. To achieve the rail-to-rail common-mode input voltage range, the inside and outside differential pairs are automatically selected by the +terminal input voltage level. If the +terminal voltage is low, transistor M12 is cut off, and the inside differential transistors M14 and M16 are dead. On the other hand, if the +terminal voltage is high, the inside and outside differential pairs are active. The middle part, which is made by M25, M26, M27, and M28, is the signal inversion stage to drive the class AB output stage, where the gain in this stage is minus one. The class AB output stage is used to reduce power consumption. The measured data for the amplifier shows the following characteristics: open loop gain is 71 dB, CMRR is 67 dB, unity gain bandwidth is 2.5 MHz, and the settling time is less than 2 μs. Using this buffer amplifier, charge duplication mode (3) in Fig. 7 is carried out within about 2 μs.

The switches in Fig. 10, SW1, SW2, SW3, and SW4, are used to separate the buffer-core from the source followers, where the buffer-core is indicated by the dotted line in Fig. 10. The reason such separation is required is that the slow settling time of the buffer amplifier causes a long sampling interval of the ACC-SH if the S/H circuit and the buffer are coupled to each other. Note that the main function of the buffer amplifier is to transmit the sampled signal to the liquid crystal cell



SF : parallel outputs by N-ch source follower and P-ch source follower

Fig. 11. Actual configuration of ACC-SH for TFT-LCD.

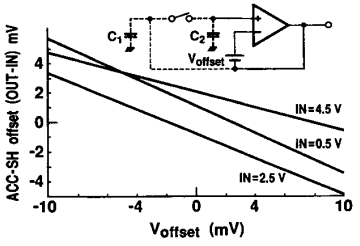


Fig. 12. Buffer V_{offset} effect simulation.

through a transparent wiring capacitance of the LCD panel, which is estimated to be a capacitive load (greater than 100 pF). Further, power dissipation must be minimal since over 192 buffers are necessary for the driver IC. The actually fabricated circuit is shown in Fig. 11. In this figure, two buffer amplifiers are required, where the buffer-core is commonly used for chip size and power consumption reduction.

The buffer amplifier has some undesirable characteristics that cause non-ideal ACC-SH operations. These are 1) nonzero input offset voltage and 2) capacitive input impedance. Fig. 12 is used to explain the effect of the input offset voltage V_{offset}. The ACC-SH operating mechanism does not compensate for the effect of the input offset, although it can slightly reduce it. In the ACC-SH, the effect induced by V_{offset} can be reduced by about one half because the error caused by V_{offset} is added only on capacitor C_1 through the feedback path. No error charge is generated on C_2. Charges on C_1 and C_2 are averaged when the switch is turned ON. The effective buffer amplifier output offset is estimated by

$$-\frac{C_2}{C_1+C_2}V_{\text{offset}}. \tag{3}$$

If $C_1 = C_2$, the effective offset by V_{offset} can be relaxed to one half. To minimize the input offset itself, large-size transistor and common centroid layout techniques are used for the offset-sensitive parts of the circuits in the fabricated LSI. Fig. 13 shows actually measured V_{offset} deviation characteristics. In this figure, the circuit in Fig. 10 is measured. The number of measured samples is 512.

Concerning the problem of the capacitive input of the buffer, where the S/H output terminal is connected to the P-channel and N-channel source followers of the buffer, the input

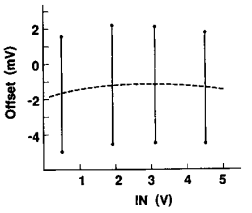


Fig. 13. Buffer amplifier offset standard deviation.

capacitance C_{in} of the source followers is defined by

$$\begin{aligned} C_{\text{in}} &\approx C_{\text{in}}^{P\text{ch}} + C_{\text{in}}^{N\text{ch}} \\ C_{\text{in}}^{P\text{ch}} &= C_{\text{gd}}^{P\text{ch}} + C_{\text{gs}}^{P\text{ch}}(1-A) + C_{\text{gb}}^{P\text{ch}} \\ C_{\text{in}}^{N\text{ch}} &= C_{\text{gd}}^{N\text{ch}} + C_{\text{gs}}^{N\text{ch}}(1-A) + C_{\text{gb}}^{N\text{ch}} \end{aligned} \tag{4}$$

where C_{gd} is the MOS transistor gate-drain capacitance, C_{gs} is the gate-source capacitance, C_{gb} is the gate-bulk capacitance, A is the source follower gain, and superscripts indicate the type of the MOS transistor. Assuming that the source follower input transistors operate in the cutoff or saturation regions because of the rail-to-rail input voltage range, Equation (4) is rewritten as

$$C_{\text{in}} \approx \begin{cases} C_{\text{in}_{\text{Sat}}}^{P\text{ch}} + C_{\text{in}_{\text{Sat}}}^{N\text{ch}} & \text{or} \\ C_{\text{in}_{\text{Cutoff}}}^{P\text{ch}} + C_{\text{in}_{\text{Sat}}}^{N\text{ch}} & \text{or} \\ C_{\text{in}_{\text{Sat}}}^{P\text{ch}} + C_{\text{in}_{\text{Cutoff}}}^{N\text{ch}} \end{cases} \tag{5}$$

where $C_{\text{in}_{\text{Cutoff}}}^{P(N)\text{ch}} = C_{\text{gd}_{\text{Cutoff}}}^{P(N)\text{ch}} + C_{\text{gs}_{\text{Cutoff}}}^{P(N)\text{ch}}(1-A) + C_{\text{gb}_{\text{Cutoff}}}^{P(N)\text{ch}} \approx C_{\text{ox}}^{P(N)\text{ch}}$, $C_{\text{in}_{\text{Sat}}}^{P(N)\text{ch}} = C_{\text{gd}_{\text{Sat}}}^{P(N)ch} + C_{\text{gs}_{\text{Sat}}}^{P(N)\text{ch}}(1-A) + C_{\text{gb}_{\text{Sat}}}^{P(N)\text{ch}} \approx 0$. C_{ox} is the oxide capacitor, and the subscript indicates that the transistor operates in the cutoff or saturation region. Equation (5) is further rewritten as

$$C_{\text{in}} \approx \begin{cases} 0 & \text{where both source followers are saturated,} \\ C_{\text{ox}}^{P\text{ch}} & \text{where N-channel source follower is saturated,} \\ C_{\text{ox}}^{N\text{ch}} & \text{where P-channel source follower is saturated.} \end{cases} \tag{6}$$

The ACC-SH capacitors must satisfy the following equation:

$$C_1 = C_2 + C_{\text{in}}. \tag{7}$$

The following two cases of C_1 are experimentally fabricated to find the optimum C_{in}:

$$C_1 = \begin{cases} C_2 \\ C_2 + \frac{2}{3}C_{\text{ox}}. \end{cases} \tag{8}$$

C. SW3

SW3 is also a CMOS switch. In the transit states to charge duplication mode and to offset-free hold mode, SW3 turns ON and OFF, respectively. The ACC-SH never compensates undesirable channel charge injected from SW3. SW3 is not included in the high speed video signal path. A very small size of SW3 is possible. The other technique is to control the fall time of the SW3 control signals. As shown in Fig. 5, if the fall time is longer than 1 μs, almost all SW3 channel charge returns

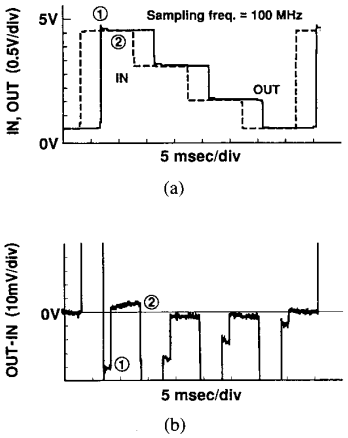


Fig. 14. ACC-SH dynamic waveforms. (a) ACC-SH input and output waveforms. (b) Difference between input and output waveforms.

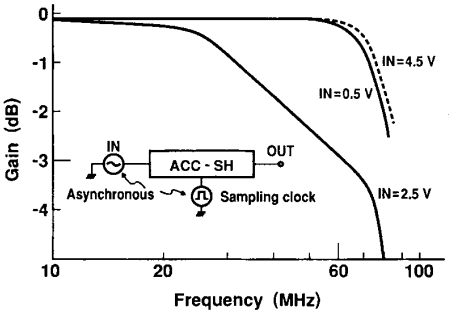


Fig. 15. ACC-SH offset frequency characteristics.

to the low impedance buffer output terminal. The undesirable effect of SW3 is reduced by these two techniques.

VI. Experimental Results

The fabricated LSI is an experimental die to verify the ACC-SH operating mechanism. The main part of the die includes 194 S/H circuits of which two are dummy circuits required to avoid interference from the peripheral circuits. Using two dummy circuits, each 192 S/H circuit is surrounded by the left-hand and right-hand S/H circuits. The remaining part consists of the test circuits. Each S/H circuit is composed of a 1-b shift register, switch control logic, two S/H circuits, and buffer amplifier, and it occupies a rectangle 62 μm by 1200 μm in size.

Fig. 14 shows the measured waveform of one S/H output, where the offset cancellation mechanism of the ACC-SH is observed. Fig. 14(a) shows the ACC-SH input and output waveforms. Fig. 14(b) shows the difference between input and output waveforms. In Fig. 14, digit 1 indicates the voltage of the offset pedestal, and digit 2 indicates the voltage after offset cancellation. Fig. 15 shows the small signal frequency characteristics of the output peak-to-peak voltage that were measured by sweeping sinusoidal input and by applying a sampling clock asynchronously. Sinusoidal input frequency is 20 kHz, the sampling time is 10 ns, and sampling interval

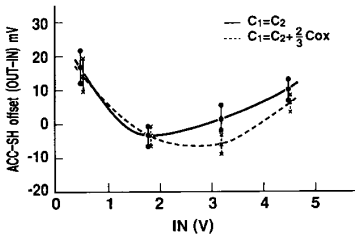


Fig. 16. ACC-SH offset standard deviation.

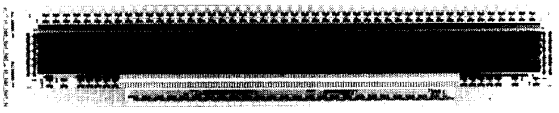


Fig. 17. Photograph of chip.

is about 50 μs. The frequency characteristics were measured under the conditions of 0.5 V, 2.5 V, and 4.5 V input biases. 60 MHz −3-dB cutoff frequency is measured at 2.5-V input bias. In the case of 0.5-V and 4.5-V input biases, −3-dB cutoff frequencies of over 80 MHz are attained for both. Fig. 16 shows the inter-chip averaged values of the ACC-SH offset and their standard deviations σ. The number of measured samples is 512, and the sampling frequency is 100 MHz. Maximum offset standard deviation of 4.7 mVrms is observed. Linearity error is less than 0.3% for 4-V full-scale range. Fig. 17 shows a die micrograph. The chip statistics are as follows: Process: 0.8-μm double-metal single-polysilicon CMOS; die size, 2.47 mm × 13.51 mm. 192 S/H outputs are available on 48 pads by 2-b addressing for experimental use only.

VII. Conclusion

The principle and applications of an ACC-SH are discussed in this paper. Concrete design problems are also discussed. It is concluded that if a S/H circuit is implemented with an interval for error compensation, not only can the ACC-SH concept be applied to LCD panel displays, but the concept can also be employed for other applications.

References

[1] H. Ohara, H. X. Ngo, M. J. Armstrong, C. F. Rahim, and P. R. Gray, "A CMOS programmable self-calibrating 13-bits eight-channel data acquisition peripheral," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 930–938, Dec. 1987.

[2] G. M. Haller and B. A. Wooley, "A 700-MHz switched capacitor analog waveform sampling circuit," in *Proc. 1993 VLSI Circuits Symp.*, Kyoto, Japan, May 1993, pp. 117–118.

[3] M. Shinnya and T. Sugawara, "A study of error for S/H circuit," in *Proc. IEICE 1989 Spring Conf.*, 1989, C-322, (in Japanese).

[4] J. -H Shieh, M. Patil, and B. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 277–281, Apr. 1987.

[5] P. Yang, B. D. Epler, and P. K. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 1, pp. 128–138, Feb. 1983.

[6] T. Shima, "Device and circuit simulator integration techniques," in *Process and Device Modeling*, W. L. Engl, Ed. Amsterdam, The Netherlands: Elsevier, 1986.

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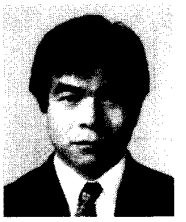

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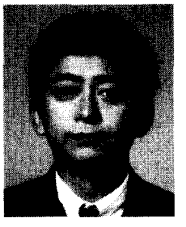

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