Brief Papers

Trimless High Precision Ratioed Resistors in D/A and A/D Converters

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Abstract—**Investigations into realization of high precision ratioed resistors in standard CMOS and BiCMOS processes have been carried out. The results indicate that the layout of the resistors can be optimized with respect to area and matching requirements to yield relative accuracy better than 0.25%. Using an intermeshed ladder architecture, fast converters with resolution up to 10 b are realizable without trimming.**

I. Introduction

In recent years, A/D and D/A converters based on the use of resistor-strings have gained great popularity. The characteristics of such converters include inherent monotonicity, temperature insensitivity, low matching requirements on components, and relative simplicity, making resistor strings useful for high-speed ADC's and DAC's with moderate resolution requirements. Since the resistors in resistive converters are usually arranged as regular arrays, and the same resistor core can be used for both A/D and D/A conversion (Fig. 1), flexible layout generators can be easily realized.

A critical aspect of the resistive concept is the size of layout and component matching requirements. Increasing the resolution by one bit causes the number of resistors in the string to be doubled. But this may not always be a disadvantage, especially in applications where more than one converter is needed, e.g., in a video processor for the red, blue, and green components. For such applications, one resistor core can be used for realizing a high speed multichannel converter with excellent matching behavior because of accessing the same resistor string.

The upper limit of achievable resolution is not only given by how many resistors can be arranged in a defined area but also by precision limits due to lithography errors and process control. Any variation leads to a spread in resistance and can be caused either by gradient or statistical errors. Optimization strategies for resistors that minimize the effects limiting precision are rare and standard approaches (named in the following section) are not applicable to converter designs in which resistor values are fixed owing to speed and power requirements and where the large number of resistors limits the area.

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This paper presents a new optimization technique for resistor matching in resistive dividers that reduces the effects limiting precision and is intended for design of resistive D/A and A/D converters featuring high speed and moderate resolution.

II. Effects Limiting Matching Precision

To realize a resistive n-bit converter, a string of 2^nwell matched resistors must be available. The matching behavior of those resistors, which are arranged in an array, is influenced by several important parameters. These parameters are the spread in sheet resistance, lithography and etching errors, bend effects, contact resistance, and alignment errors.

Lithography and etching errors lead to statistical and deterministic deviations of resistor ratios from the desired value. The precision of converters based on the string principle is independent of the design center resistance value, which is defined as the averaged resistance of all matched resistors in one converter. The absolute value can fluctuate in a range of about 30% from one wafer to another. Statistical deviations from this value are large for small structures and become smaller if structure size increases. Increasing the resistor size, however, must be carried out with care because of the increasing influence of deterministic deviations for larger structures. Thus, gradient errors with respect to the resistor core depend on height, orientation, and slope of the spread in sheet resistance. An optimal geometry for resistor layout has to be found, which reduces the statistical errors to minimum, assuming the statistical errors still dominate when compared with gradient errors.

In hand-crafted analog design it is usual to design well-matched resistors without any bends. In a flexible layout generator for different resolutions (2^n resistors), the resistors must contain bends or the area requirements would become excessive. Effects that decrease matching due to deterministic errors caused by bends, lithography, and etching are minimized by using an identical basic resistor cell for all matched resistors.

Another critical problem stems from contacts interconnecting the array resistors. Their resistance varies widely and can degrade matching behavior. Especially in converters featuring higher resolution in which low-valued resistors ($< 10\ \Omega$) are used, contact resistance can easily dominate over the string resistance. Also, mask tolerances can lead to contact alignment errors. To avoid these problems, the resistors are arranged in groups in which no contacts are used in the current path.

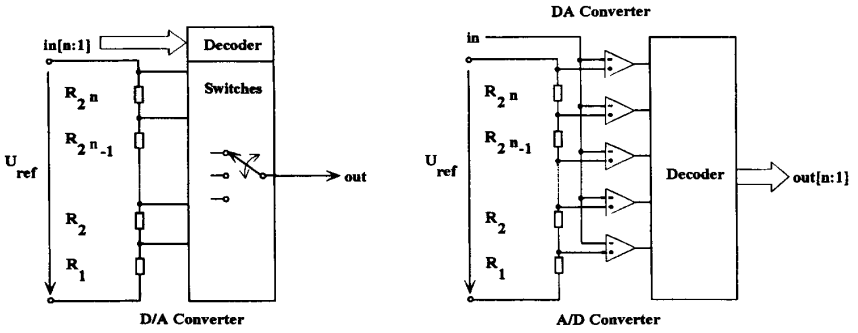

Fig. 1. Parallel resistor-string D/A and A/D converter.

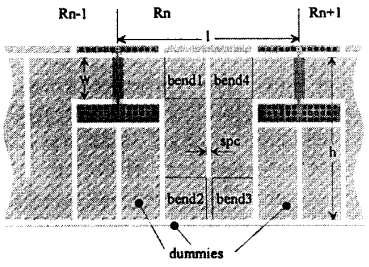

Fig. 2. Layout of basic resistor cell.

The resistors are interconnected without leaving the resistor layer. At the end of each resistor chain, where contacts are unavoidable, arrays of contacts are used for interconnection.

III. Resistor Cell

A flexible resistor layout generator (Fig. 2) has been developed that takes into account all aspects considered before. The resistor generator has been developed for use in a D/A and A/D converter compiler. Independent parameters are the length l, the resistance r, the width w, the spacing spc, and the material with the sheet resistance Rs of the resistor. Dependent parameters are the resulting height h and the number of foldings n.

The contacts for each voltage tap are set outside the reference current path and connected with the resistor layer to the voltage tap. This kind of connection is insensitive to alignment tolerance of the contacts. The use of two symmetrical contact arrays for each tap decreases the tap interconnection resistance and increases speed, since charge time for parasitic capacitances has been reduced. This principle is described in detail in [1]. The spacing between resistor meanders is kept constant. In case of missing meanders from a neighboring resistor, dummy polygons are used instead.

IV. Measurement of Matching Behavior

To investigate the influence of resistor parameters on matching behavior independent of technology, several test circuits with a string of 11 identical resistors were realized in a 0.8 μm-BiCMOS technology [2] and a 1.5 μm-HT-SIMOX process [3]. The resistor type used in converters with moderate resolution (9–12 b) has to have a low sheet resistance (< 50 Ω/square). Resistors in the SIMOX process were fabricated in polysilicon and exhibited 18 Ω/square. In the BiCMOS technology, an additional process step (silicide) decreased the sheet resistance of polysilicon to 1.2 Ω/square. Because of this additional process step in the BiCMOS technology, a better matching behavior for the SIMOX resistors was expected. The process modules used for resistor fabrication in the SIMOX process were the same as in a standard CMOS process. Fig. 3 summarizes the measured results of the test circuits.

The measurement of test structures yielded several important results described below. The maximum of measured relative accuracy exceeded values known from open literature. The maximum of measured relative accuracy was found to be 0.24% for SIMOX and 0.32% for BiCMOS technology (for untrimmed resistors). Values known from literature vary in the range of 0.5–1%, but these are based mostly only on paired resistors and have high area requirements ($w > 25$ μm [4]). In the measured range, the number of bends (varied between 4 and 20) had no influence on matching behavior. Matching behavior was found independent from the current density in the evaluated range of 40–1500 μA per μm line width (Fig. 3). Meander spacing in the range of 2–4 μm had also no effect on accuracy.

A direct dependence of the relative accuracy on resistor area was confirmed. The measurements corroborate our statement made above. Statistical errors dominate the resistors mismatch for small structures and deterministic errors due to gradients dominate in the case of large structures, so that an optimum can be easily determined. Thus, in the range below the maximum accuracy ($a < a_{crit}$, $\approx 10\,000$ μm^2 in BiCMOS), where statistical deviations dictate the matching behavior of resistors, a heavy dependence between matching error p and design area a is apparent (Fig. 4). In the double logarithmic diagram, all resistor types exhibit the same slope but different offsets for different fabrication processes. This behavior is almost independent of the realized resistance; only the area determines the precision and not the resistor width in cases where statistical errors dominate the resistor mismatch. Measurement results lead to a simple equation, which allows modeling of the statistical precision errors (1). This yields an area optimization procedure for the resistor core with respect

Type	Technology	Material	R	l/h	Area	No. of bends	spc	w	Current density	Matching * error p *	Standard deviation
		(Ω/□)	(Ω)		(μm²)		(μm)	(μm)	(μA/μm)	σ_m, 11 res.	σ, 15 str.
1	BiCMOS	Silicide (1.2)	10	2	1220	4	2	8	1500	0.90 %	0.143 %
2	BiCMOS	Silicide (1.2)	10	1.4	2568	4	2	12	1025	0.60 %	0.112 %
3	BiCMOS	Silicide (1.2)	10	1.1	4340	4	2	16	750	0.51 %	0.165 %
4	BiCMOS	Silicide (1.2)	100	2.4	2640	20	2	4	300	0.56 %	0.116 %
5	BiCMOS	Silicide (1.2)	100	0.7	9040	12	2	8	160	0.32 %	0.070 %
6	BiCMOS	Silicide (1.2)	100	0.5	12960	8	2	8	160	0.34 %	0.070 %
7	BiCMOS	Silicide (1.2)	100	0.1	51288	4	2	16	75	0.63 %	0.422 %
8	SIMOX	Poly (18)	500	1.5	572	8	2	2.6	140	0.66 %	0.117 %
9	SIMOX	Poly (18)	500	1.1	1778	8	2	5	64	0.38 %	0.100 %
10	SIMOX	Poly (18)	500	1	4330	8	2	8	40, 370	0.25 %	0.046 %
11	SIMOX	Poly (18)	500	1	4330	8	3	8	40	0.24 %	0.058 %
12	SIMOX	Poly (18)	500	1	4330	8	4	8	40	0.24 %	0.050 %

* averaged over 15 structures consisting of 11 resistors each

Fig. 3. Matching behavior of different types of resistors.

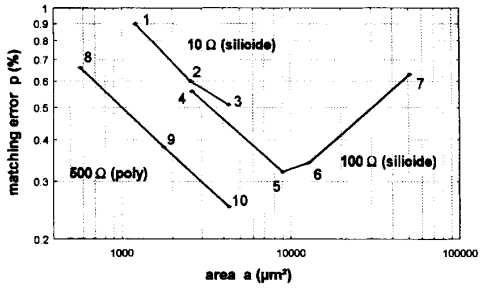

Fig. 4. Measurement results.

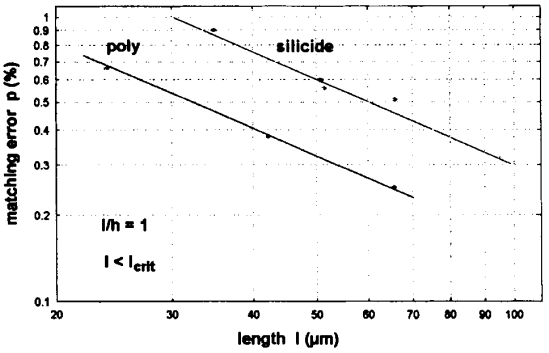

Fig. 5. Modeling of statistical errors.

to precision requirements for a defined converter resolution

$$p = \frac{1}{\sqrt{a'}}$$

$$a' = \frac{a}{a_{ref}}$$

and

$$a \leq a_{crit} \tag{1}$$

with

- p expected matching error in percent,
- a' normalized area of single resistor,
- a area of single resistor,
- a_{ref} reference resistor area (1% target precision) (SIMOX: $a_{ref} = 260\ \mu\text{m}^2$, BiCMOS: $a_{ref} = 900\ \mu\text{m}^2$).

In the range $a \leq a_{crit}$, the matching behavior is dominated by statistical mismatch, and the matching precision can be doubled by quadrupling the area of the resistors. Since this equation is valid for l/h ratios from 0.7–2.4, measurement results can be transformed to squared resistors ($l/h = 1$). In this case, the matching precision is proportional to the edge l of the resistor (Fig. 5). For $a > a_{crit}$, gradient errors degrade matching behavior. This area range should be avoided.

V. Resistor Core

Next, precision requirements imposed on resistors to be used in the core of an n-bit A/D or D/A converter will be analyzed to estimate the achievable resolution of conversion with this type of resistor. The matching tolerance $tol(Rx)$ can be defined as the relative error according to the average value Rm of all resistors of a string

$$tol(R_i) = \frac{R_i - \overline{R}}{\overline{R}} \cdot 100\%$$

with

$$\overline{R} = \frac{1}{j} \cdot \sum_{i=1}^{j} R_i \quad j\text{: number of resistors in a string.} \tag{2}$$

Only the matching tolerance decreases matching behavior, not a shift of Rm. The voltage at each node of a n-bit converter resistor string is found as

$$V_x = \frac{\sum_{i=1}^{x} R_i}{\sum_{i=1}^{2^n} R_i} \cdot V_{ref} = \frac{x + \sum_{i=1}^{x} \frac{tol(R_i)}{100\%}}{2^n} \cdot V_{ref} \quad 1 \leq x \leq 2^n. \tag{3}$$

The difference between V_x and $V_{x,ideal}[tol(Ri) = 0]$ has to be less than ± 0.5 LSB at all nodes of the string to meet specification.

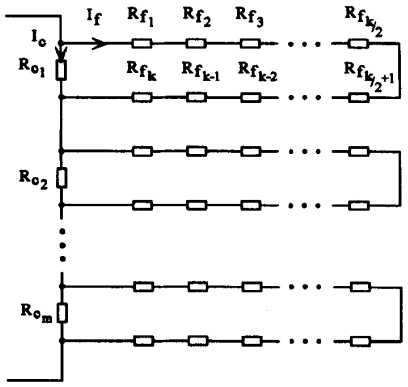

Fig. 6. Intermeshed ladder.

In a first approach worst case precision, requirements based on sensitivity analyses [9] are compared, which allow analysis of the influence of small parameter variations on the operating point of a circuit. The influence of correlated small resistor variations on the critical node of a resistor-string (center of the string) can determined with (4)

$$\Delta V_{crit} = \left|\frac{\partial V_{crit}}{\partial R_1} \cdot \frac{R_1}{100\%} \cdot tol(R_1)\right| + \left|\frac{\partial V_{crit}}{\partial R_2} \cdot \frac{R_2}{100\%} \cdot tol(R_2)\right| + \cdots + \left|\frac{\partial V_{crit}}{\partial R_2^n} \cdot \frac{R_2^n}{100\%} \cdot tol(R_2^n)\right| \leq \frac{V_{ref}}{2^{n+1}}. \quad (4)$$

With use of the same type of resistor (same layout) for all resistors in the string, (4) results in

$$tol(R_{string}) \leq \frac{100}{2^n}\% \quad (2^n \text{ resistors}). \quad (5)$$

Equation 5 defines the precision requirement for an n-bit string converter in which all 2^n resistors are connected in series. A limitation of the string principle is the area required for the resistor layout. Each additional bit requires doubling of the number of resistors. Also, the accuracy requirements imposed on the resistors are doubled, which considerably increases the area of each resistor (Fig. 4).

Chip size requirements can be relaxed by using an intermeshed resistor ladder [5]–[8]. The use of a small number of additional coarse resistors (Fig. 6) decreases precision requirements on the ladder resistors (6), which are arranged in decoupled groups of fine resistors. The intermeshed ladder architecture allows building of smaller and faster converters (owing to decreasing parasitic capacitances) than converters featuring the same resolution and using standard string structure.

The intermeshed ladder consists of two critical nodes. The first is found in the center of the coarse ladder on which the sensitivity for variation of the coarse resistors is maximal, and the second is found in the center of one of the direct neighbored fine-strings on which the sensitivity for variation of the fine resistors is maximal. With respect to the sensitivities of those critical nodes on deviations of the coarse resistors

Concept	Components for Core	Additonal Parameters	Matching Requirements	Area for Resistors
a) 7 bit				
string	128 Rs	-	tol (R) 0.8%	0.077 mm²
interm. ladder	4 Rc, 128 Rf	r=10, m=4	tol (Rc) 0.6% tol (Rf) 0.8%	0.061 mm²
b) 8 bit				
string	256 Rs	-	tol (R) 0.4%	0.512 mm²
interm. ladder	8 Rc; 256 Rf	r = 10; m=8	tol (Rc) 0.26% tol (Rf) 0.80%	0.151 mm²

Fig. 7. Comparison of matching requirements.

Rc and the fine resistors Rf, precision requirements can be estimated by

$$\frac{r}{r+1} tol(R_c) + \frac{1+\frac{r}{m}}{r+1} tol(R_f) \leq \frac{100}{2^n}\% \quad (2^n \text{ resistors } Rf,\ m \text{ resistors} Rc) \quad (6)$$

with

n resolution,
$tol(x)$ matching tolerance of x,
m number of coarse resistors,
k number of fine resistors attached to one coarse resistor,
$m * k = 2^n$,
$r = Ic/If = k * Rf/Rc$.

The table in Fig. 7 allows a comparison of the presented concepts. Based on matching measurements given in the previous section and the worst case considered (i.e., 100% yield), the achievable resolution for each concept is shown. Thus, considering the worst case, a resolution of 8 b can be realized using an intermeshed ladder.

Since statistical errors in matching precision dominate for the applied resistors, matching requirements are excessive for the worst case. For the string converter, the worst case has been found for all resistors in the upper half of the string being increased by the worst case tolerance and in the lower half being decreased by the worst case tolerance (or vice versa). The error at the node in the center of the string has to be below $\pm\frac{1}{2}$ LSB to reach the desired resolution. In reality, higher resolutions can be obtained considering the measured degree of matching. Measurements have shown that the matching error has a Gaussian distribution along the design center value. Therefore, a second approach was made that is based on statistical analysis of the resistor core and seems to be the more realistic one. Nevertheless, the statistical approach may be too optimistic for a higher number of coarse resistors ($m \geq 32$) in the intermeshed ladder architecture since the influence of gradients increases.

Monte Carlo simulations have been carried out using the simulator Pspice modeling, the matching error of the intermeshed ladder with a Gaussian distribution function. The simulations were restricted to the coarse resistors only ($m = 16$) because of their dominant matching requirements. In the case of a desired resolution of 10 b, the fine resistors have to match only within a 6-b precision. All error-sensitive nodes

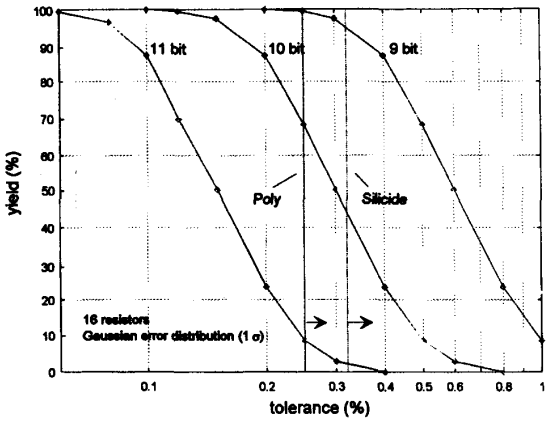

Fig. 8. Yield dependence on matching of resistors (Monte Carlo simulation).

(15) were monitored. A string was considered acceptable, if all nodes had an error below $\pm\frac{1}{2}$ LSB. The yield dependence for converters (9–11 b) on the degree of matching (Gaussian distribution 1σ) was analyzed, and the result is shown in Fig. 8. It can be seen that the measured precision can be realized for resistive converters with up to 10-b resolution with an acceptable yield.

VI. Conclusion

Based on the known effects limiting precision of resistor matching, methods for realizing high precision ratioed resistors in standard processes have been presented. Several test structures have been realized in a 1.5 μm HT-SIMOX and a 0.8 μm BiCMOS technology. The evaluation of dependence of matching behavior on resistor size showed that statistical errors dominate the resistor mismatch for small structures, while gradient (i.e., deterministic) errors dominate the mismatch for large resistors. Hence, an optimum size for resistor arrays can be found, which yields an optimum precision. In the SIMOX process [3], a matching precision of 0.25% was reached. It was found that bending had no measured influence on resistor precison. A worst case analysis showed that a converter resolution of 8 b can be reached using the intermeshed ladder principle. With a more realistic statistical analysis the intermeshed ladder converter can reach 10-b resolution with the SIMOX technology and 65% yield.

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