A Low-Power CMOS Time-to-Digital Converter

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***Abstract*— A time-to-digital converter, TDC, with 780 ps lsb and 10-μs input range has been integrated in a 1.2-μm CMOS technology. The circuit is based on the interpolation time interval measurement principle and contains an amplitude regulated crystal oscillator, a counter, two pulse-shrinking delay lines, and a delay-locked loop for stabilization of the delay. The TDC is designed for a portable, low-power laser range-finding device. The supply voltage is 5 ± 0.5 V, and the operating temperature range is −40 to +60°C. Single-shot accuracy is 3 ns and accuracy after averaging is ±120 ps with input time intervals 5–500 ns. In the total input range of 10 μs, the final accuracy after averaging is ±200 ps. Current consumption is 3 mA, and the chip size is 2.9 mm * 2.5 mm.**

I. Introduction

In a pulsed time-of-flight laser range-finder, the time interval between sending a laser pulse (start) to the target and receiving the reflected pulse (stop) is measured (Fig. 1). A distance of 1 m to the target corresponds to a 6.7-ns time interval. Typical values for the pulse length and the pulsing frequency are 10 ns and 1 kHz–1 MHz, respectively. The reflected light pulse is converted to current in a photodetector, converted further to voltage and amplified. Logic-level timing pulses are generated in a timing discriminator for the time interval measurement block.

Laser range-finding is used in many industrial applications where, for example, the large size of the target or the high temperature of surfaces makes conventional methods impractical. Examples are the measurement of dimensions of ship blocks in shipyards, profiling of steel converters for detection of damage in refractory lining, inspection of oil level in large tanks, vibration measurements, and robot vision [1]. Current versions of laser radar are based on commercial circuits. Depending on the application (reflectivity of the target, optical/electrical gain control, amount of averaging, etc.) they achieve mm or cm level accuracy.

This work is part of a project that aims at developing a low-power, portable laser radar. In the present discrete version, the amplifier channel together with the timing discriminator and the time interval measurement unit occupy one Euro-1 (10 cm * 16 cm) circuit board each, and both have high power consumption of 5 W due to the ECL-based implementation. By integrating the amplifier channel, the timing discriminator and the time interval measurement circuitry in 5-V CMOS/BiCMOS technology, the radar could be constructed using only a few low-power ASIC's and some discrete components such as a laser diode and photodetector. The aim is to achieve cm/dm class accuracy and a measurement range of 1 km in a large temperature range of −40 to +60°C.

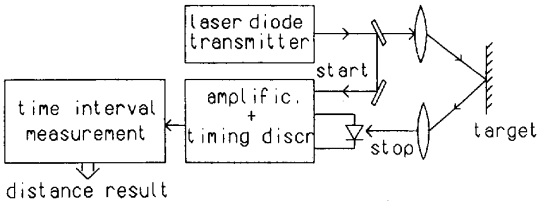

Fig. 1. Block diagram of the pulsed time-of-flight laser range-finder.

The amplifier channel has been integrated in a 1.2-μm CMOS process [2] and a new BiCMOS version, which also includes the timing discriminator, is under fabrication. The time interval measurement unit, time-to-digital converter (TDC), has been integrated on one chip and is presented here. In Section II, the potential time interval measurement methods for realization of the time measurement unit are discussed. In Section III, the implemented circuit is presented. In Section IV, experimental results from prototype chips are given. Other possible applications for the TDC are, for instance, particle detectors and automatic test equipment (ATE) devices.

II. Basic Design Considerations

In time measurement, the distance measurement range required of the integrated laser radar corresponds to 6.7 μs, and a distance measurement accuracy of 2–3 cm corresponds to 100–200 ps. There is no single method for time interval measurement that can simultaneously achieve subnanosecond resolution, a linear measurement range of several microseconds, and low power consumption. In practice, the only alternative for realization of the wide linear range in integrated circuit technology is to use a counter with a stable reference clock. However, the worst case single-shot resolution is limited to one clock period, since the maximum error in one measurement is ±1 period. Subnanosecond single-shot resolution requires a clock frequency of over 1 GHz, which consumes power and is difficult to implement with standard CMOS technology. Thus, a crystal oscillator operating at a fundamental frequency of 20 MHz was chosen as the frequency reference, and other complementary methods to improve resolution were considered.

Since the measurement here is asynchronous, i.e., the start pulse has a random phase with respect to the circuit clock, averaging can be used to improve the resolution of the counter method at the expense of measurement time which increases. When a single time interval with a random phase with respect to the system clock (T_{fref}) is measured repeatedly, the expected value of the average equals the time interval to

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be measured. Since averaging is a statistical process, the value of the standard deviation (σ) is used to estimate the variation in the result, i.e., to determine the time interval measurement resolution of the system. The standard deviation reduces proportionally to the square root of the number of results averaged (N) and has a worst case value of $\sigma = (0.5T_{\text{fref}})/\sqrt{N}$ [3]. A systematic error in the mean value, on the other hand, is not affected by averaging and sets the limit for the achievable accuracy. Systematic errors include, for example, linearity and stability errors. Here, the resolution of the system is expressed as twice the value of the standard deviation. Using the 20 MHz frequency reference to achieve a resolution of 100 ps, 250 000 samples need to be averaged. Operating at a typical 10-kHz measurement frequency, measurement time for one result is 25 s, which is unacceptably long. Thus, a better single-shot resolution is preferable to reduce the need for averaging.

Various methods of improving resolution without increasing the clock frequency are described in [4]. These techniques can be divided into two groups: methods that are based on the use of more than one oscillator such as the vernier-principle, and methods that combine one oscillator with separate interpolators, such as time-to-voltage converters or delay lines.

The most straightforward implementation of the first type of methods is to use a multiphase oscillator with a separate counter for each phase. The measurement resolution improves proportionally to the number of phases, which for a feasible realization is limited. For example, if a ring oscillator used as the multiphase oscillator has a 1-ns phase length, 10 elements, and thus, 10 counters, are needed to operate the counters at a reasonable frequency of 50 MHz. In the vernier method, only two startable oscillators with slightly different frequencies are used. The input is the time interval between the rising edge of the start pulse and the rising edge of the stop pulse. The start pulse enables the oscillator with a lower frequency, and the stop pulse initiates the oscillator with a higher frequency. Two counters record the pulses from the oscillators until their phases coincide. Measurement resolution is equal to the difference between the oscillator periods. A further improved version is the dual vernier method, in which the start and stop oscillators have equal frequencies and their phase crossover points with a third, continuously running oscillator are detected. An advantage compared with the traditional vernier method is that the offsets in the start and stop channels cancel. Vernier methods have good single-shot resolution, but due to their high power consumption are not suitable for portable devices [5], [6].

The time interval measurement principle shown in Fig. 2 is based on the use of two separate interpolators [7]. The input time interval is roughly digitized by counting the reference clock periods during this interval. The counter is enabled at the first clock pulse following the start pulse and disabled at the first clock pulse following the stop pulse. The resulting time interval $T12$ is synchronized to the clock and is, therefore, accurately measured. The fractions $T1$ and $T2$ are digitized separately using either time-to-voltage converters or delay lines.

In a time-to-voltage converter, a capacitor is discharged with a constant current during the input time interval (Fig. 3(a)). The change in the capacitor voltage is proportional to the input time and can be converted into a digital form with a conventional A/D converter or, alternatively, the pulse stretching principle can be utilized. In pulse stretching, the capacitor is charged back to the initial voltage with a current smaller than the discharging current. Thus, when clock periods are counted during the charging time, resolution improvement compared with direct counting during the discharging time is proportional to the stretch factor. Time-to-voltage converters easily achieve subnanosecond single-shot resolution [8], [9]. However, in 5-V CMOS technology, they have a relatively short linear measurement range [10].

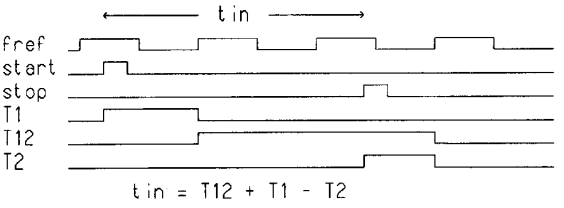

Fig. 2. Time interval measurement method based on the use of two separate interpolators.

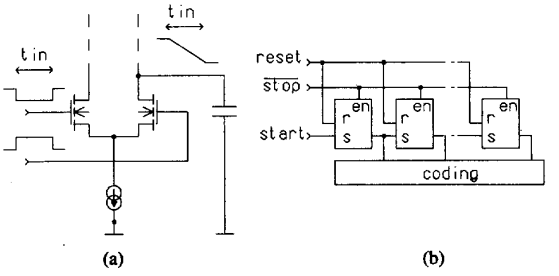

Fig. 3. Principle of (a) time-to-voltage conversion and (b) time interval measurement with a delay line.

Logic delay lines use gate delay as the basic element in measurement. In Fig. 3(b), an example is shown. The start pulse sets flip-flops until the stop pulse arrives. The number of the first element not set is coded as the measurement result. The delay of the element must be controllable to compensate for the effects of process variations and temperature and supply changes on the delay. Single-ended elements are usually based on inverters and the control parameter can be the bias current [11], [12] or the load of the element [13]. Differential delay elements are used especially in ring oscillators due to their better power supply noise rejection [14], [15].

Since low power consumption is essential in portable devices, the method of using two separate interpolators with one oscillator is preferable to the methods based on multiple oscillators. As interpolators, delay lines are more compatible with 5-V CMOS technology than time-to-voltage converters. As the oscillator period, 50 ns, is rather long, and the number of delay elements needed to achieve nanosecond resolution is thus large, single-ended delay lines, instead of differential ones, were chosen to limit the power consumption and the size of the circuit. By combining a counter and two CMOS delay line interpolators, the wide linear range of the first can thus be combined with the good single shot resolution of the second without using a high clock frequency.

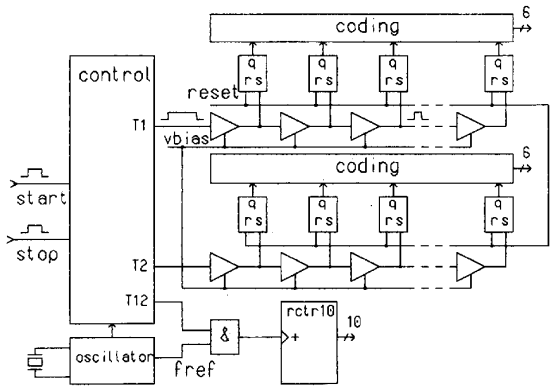

Fig. 4. Block diagram of the TDC.

III. Description of the Time-to-Digital Converter

The main parts of the time measurement chip (Fig. 4) are a crystal oscillator used as a stable frequency reference, a 10-b ripple counter, two pulse-shrinking delay lines, and the delay stabilization loop shown in Fig. 7. The crystal oscillator has a maximum fundamental frequency of 20 MHz [16]. Amplitude regulation is implemented to limit power consumption. The input to the TDC is the time between the rising edge of the start pulse and the rising edge of the stop pulse. The input time interval is digitized according to the principle shown in Fig. 2, and the result is read from eight data lines in three parts.

A novel pulse-shrinking delay line has been used since it has better resolution than ordinary delay lines [17]. In a pulse-shrinking element, the resolution depends on the difference of two delays, which can be made smaller than the minimum gate delay. The input pulses $T1$ and $T2$ for the pulse-shrinking delay lines are generated as shown in Fig. 2. As $T1$ ($T2$) travels through the delay line, the width of the pulse shrinks in each element by a fixed amount, until the pulse entirely disappears. The rs flip-flops connected to the inputs of the delay elements are set by the propagating pulse, until the pulse vanishes, after which the following flip-flops are left reset. The address of the first flip-flop not set is coded to the output. Both delay lines have 64 elements. This gives an overall time measurement resolution of $T_{\text{fref}}/\ 64 = 50$ ns $/\ 64 = 780$ ps with the 20-MHz frequency reference.

The schematic of the pulse-shrinking element, which consists of two inverters, and the corresponding rs flip-flop is shown in Fig. 5. The propagation of the rising edge of the input pulse is slowed down by the current starving transistor $N3$ while the falling edge travels fast. Thus, in each element, the pulse shrinks with an amount of tr-tf. The falling edge propagates at a rate that varies freely with process parameters and temperature and supply voltage changes while the propagation of the rising edge is controlled by the gate voltage of $N3$ (vbias). The simulated propagation delays for the rising edge (tr) and falling edge (tf) of the pulse as a function of this bias voltage are shown in Fig. 6. Simulations are done with nominal (nominal process parameters, +25°C, 5-V supply), slowest (slow parameters, +60°C, 4.5-V supply) and fastest (fast parameters, −40°C, 5.5-V supply) tf. In all conditions,

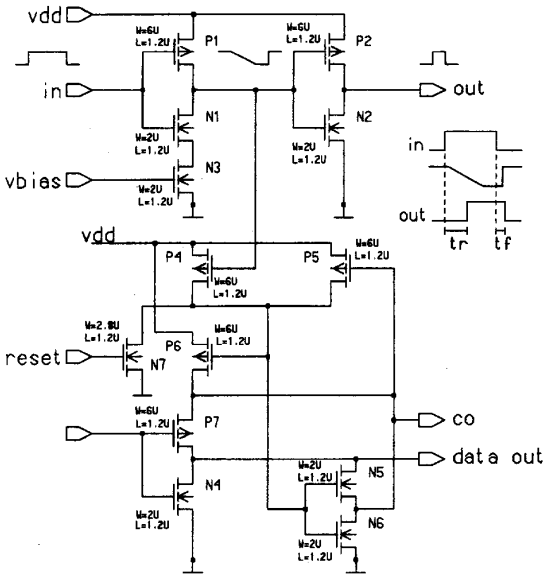

Fig. 5. Schematic diagram of the pulse-shrinking delay element.

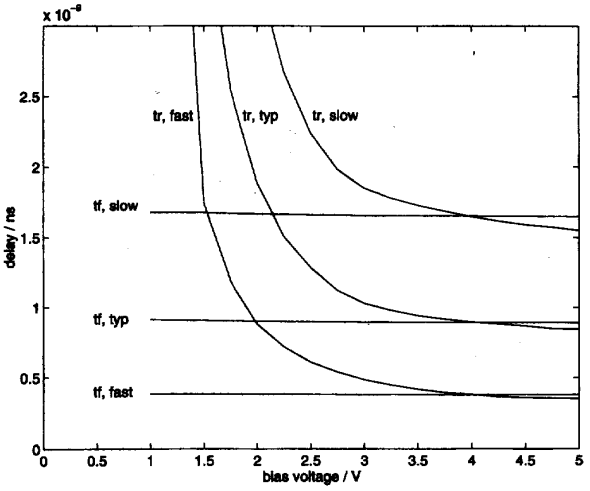

Fig. 6. Simulated propagation delays of the pulse-shrinking element for the rising (tr) and falling (tf) edge of the input pulse as a function of the bias voltage.

the desired resolution (tr-tf = 780 ps) is achieved with a suitable bias. The steep part of the control characteristics should be avoided, since even a small disturbance in the bias voltage causes a large change in tr.

The delay elements are stabilized with a delay-locked loop, which generates the bias voltage vbias, as shown in Fig. 7. The delay line indicated is one of the two delay line interpolators of Fig. 4. The other interpolator is calibrated identically, and calibration cycles are repeated automatically inside the circuit until an external measurement request is received. Basically, the bias voltage is adjusted so that a pulse of width T_{fref}, which is equal to the maximum input time interval of the interpolator, just disappears in the last delay element. At the beginning of a calibration cycle, an en_cal pulse that enables the calibration

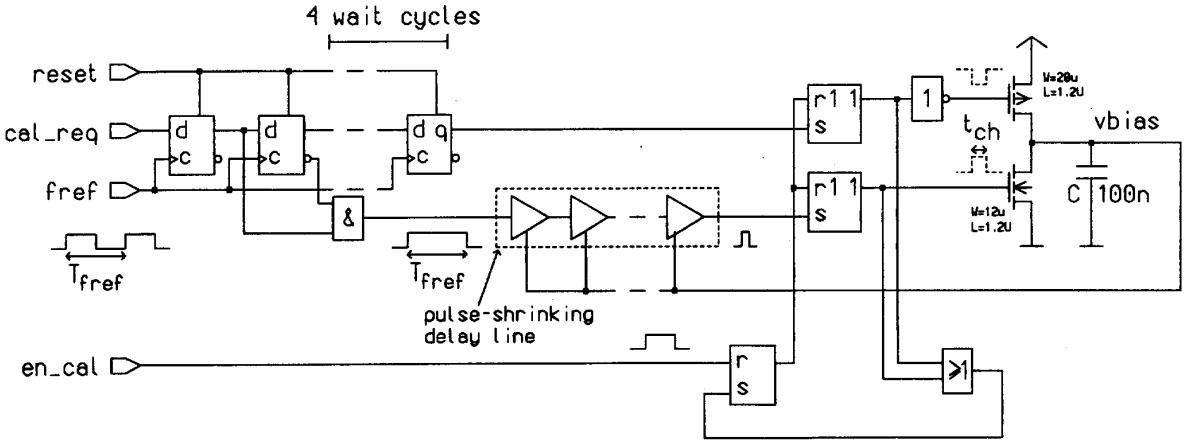

Fig. 7. Conceptual schematic of the delay-locked loop for delay stabilization.

is generated. Next, a pulse of width T_{fref} is fed into the delay line. If it disappears in the delay line, the bias voltage is automatically adjusted upwards after four wait cycles. If the pulse does not shrink enough and comes out of the delay line, it corrects the bias voltage downwards before the wait cycles have passed and disables the upwards adjustment. When balance is achieved in every other calibration cycle, the bias voltage is adjusted upwards and in every second cycle downwards with a fixed step. With a charge pump output current I and adjustment pulse width t_{ch}, the voltage step is $\Delta u = Q/C = I \cdot t_{\text{ch}}/C$. The resulting change in the length of the delay line is $\Delta t_D = 64 \cdot K \cdot \Delta u$, where K is the gain (s/V) of the delay element, i.e., the slope of the tr curves in Fig. 6. Δt_D must be limited to a fraction of the LSB and can be controlled by the off-chip capacitor value. With the component values shown in Fig. 7 and $t_{\text{ch}} = 4$ ns (nominal value of gate delays in the feedback loop), Δt_D is approximately 50 ps. In the future, it will possible to integrate the capacitor on-chip. However, since the capacitor value has to be scaled down, also the charge pump output current and t_{ch} have to be reduced.

The 64-stage pulse-shrinking delay lines are physically relatively long, and thus have a nonneglible amount of integral nonlinearity due to process gradients. In single-shot measurements, the nonlinearity deteriorates resolution. Averaging converts the nonlinearity to an offset [18], and thus ideally, when using two identical delay lines, the offsets from the delay lines cancel in the final averaged result. In practice, the delay lines are not identical, and some offset is left uncancelled. Also, in the control block (Fig. 4), the mismatches of the logic gates creating the time intervals $T1$ and $T2$ and not included in the path of the calibration pulse cause offset. The offset in itself is not a serious problem in this application, since every circuit will be tested prior to use, and the processor controlling the laser radar could subtract a constant offset from the final measurement result. However, the offsets are temperature and supply voltage dependent.

To compensate the offsets, two separate methods, which are both depicted in Fig. 8, were implemented in the control logic block of Fig. 4. In the first scheme, each circuit is tested

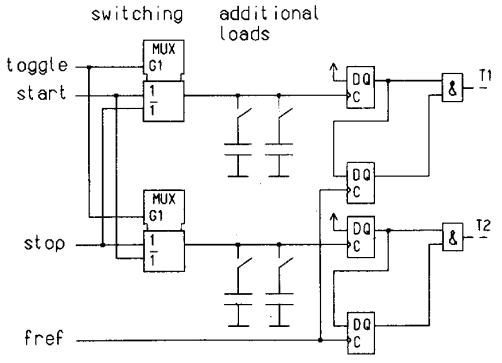

Fig. 8. Compensation of offset by adding extra load to start/stop channel or by switching start and stop channels.

separately to measure the size and sign of the offset. Additional capacitive load is then connected to either the start or the stop signal path to eliminate the offset. The connecting switches are actually transistors, which are opened or closed according to control data stored on a register. This register is written through the eight data lines, which are bidirectional, when the circuit is powered up. Both the offset from the delay lines and the offset from the control logic can be compensated with an accuracy that is limited by the size of the unit load. In the second method of Fig. 8, the start and stop signal paths are switched. In every second measurement, the start pulse is directed to the logic and delay line usually used for the stop pulse, which in turn is directed to the logic and delay line usually used for the start pulse. For each input time interval, two measurements are made, and the average of these is calculated. The input pads and multiplexers used to switch start and stop are not inside the compensation scheme resulting in a small offset. There is now no need to test the circuits before use.

The start and stop inputs are asynchronous with respect to the circuit clock so there is a possibility of metastability in the flip-flops clocked by fref. If a start (stop) pulse arrives

near the rising edge of fref, the propagation delay of the corresponding flip-flop can increase, and the time interval $T1$ ($T2$) will be erraneous. The probability of metastable states could be decreased by using double synchronization [8], but the maximum input time interval of the delay line interpolators would be twofold. Doubling the length of the interpolators from 64 elements to 128 elements would result in an integral nonlinearity considerably larger than ± LSB. Since the probability of metastable states is small and the impact of one corrupted measurement is reduced by averaging, the double synchronization scheme was not employed.

IV. Measured Performance

The experimental results presented here are from prototype chips fabricated in a 1.2-μm CMOS process. The size of the circuit is 2.9 mm * 2.5 mm. The average current consumption, when time interval measurements were made at a rate of a few kHz was measured to be 3 mA from a 5-V supply. Since the calibration rate between measurements is approximately 2 MHz, most of the power is lost there, and the power consumption of the circuit can easily be reduced by lowering the calibration rate.

A. Single-Shot Accuracy

The single-shot resolution was measured as the 2σ-value of the distribution of single-shot measurements. Additional loads were used for offset compensation. The measured worst case resolution varied between 1.5–2.5 ns from chip to chip due to variations in delay line nonlinearities. Resolution on each chip is worst when the input time interval is a multiple of half of the clock period and best when the input time interval is a multiple of the clock period (Fig. 9). The results in a) and b) are from a typical chip and correspond to resolutions of 1.7 ns and 0.7 ns, respectively. Ideally, the graph in a) would consist of two bars and the graph in b) of only one bar. The main reason for the deterioration of the resolution from the theoretical value is the nonlinearity of the delay lines. In asynchronous measurements, all the values of the time intervals $T1$ and $T2$ have equal probability independent of the actual input time interval. Thus, nonlinearity in the delay lines appears as random variation between successive measurements.

The differential nonlinearity of a delay line can be measured by collecting the distribution of $T1$ ($T2$) in asynchronous time interval measurements. In Fig. 10(top), the differential nonlinearities of the two delay lines on one chip have been measured using this method. The delay line is folded from the middle resulting in the first half of the channels being longer than the second half. It was also discovered that $T1$ and $T2$ were never zero and that the maximum value 63 was twice as probable as the values 1–62. From this it was concluded that the time intervals $T1$ and $T2$, which are generated in the control block, have a positive bias. As long as $T1$ and $T2$ are both too long, no error is present in the final result. But if the correct value of $T1$ ($T2$) is 63, it can not be any larger, and the final result will have an error of +LSB (−LSB).

The measured integral linearity error for the stop interpolator of one circuit is shown in Fig. 10(bottom). It was measured

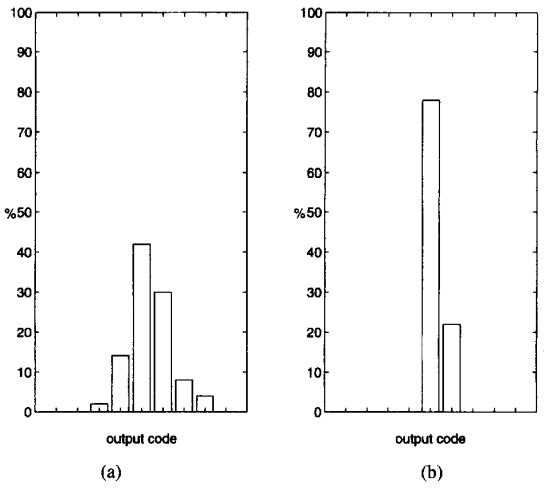

Fig. 9. Typical distribution of single-shot measurement results in 50 measurements. In (a), the input time interval is a multiple of half the clock period, and in (b), the input time interval is a multiple of the clock period.

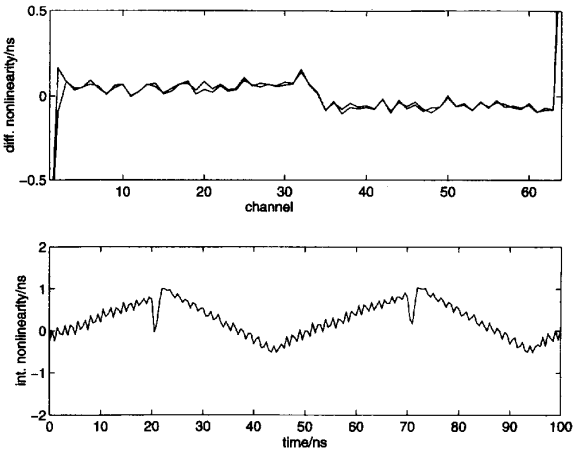

Fig. 10. Measured (top) differential nonlinearity of the two delay lines on one chip and (bottom) integral nonlinearity of one delay line.

by synchronizing the start pulse with the clock of the TDC (i.e., $T1$ was kept constant), and the input time interval was incremented so that $T2$ swept through all the 64 possible values. The abrupt change in nonlinearity occurs between the last and first element of the delay line. A typical peak-to-peak value for the measured integral linearity error is 2 ns.

The measured resolution improves in proportion to the square root of the number of results averaged, as expected. To achieve a resolution of 100 ps, 600–700 results need to be averaged. With a typical measurement rate of 10 kHz, this can be accomplished in 60–70 ms, which is usually an acceptable measurement time. It is important to notice that the accuracy of an averaged result is not directly influenced by the nonlinearity of delay lines or the bias in $T1$ and $T2$, since the sum of the errors in average $T1$ and $T2$ are equal and cancel out. Instead, the accuracy of an averaged result is limited by system nonlinearity and stability errors which, of course, also deteriorate the single-shot accuracy.

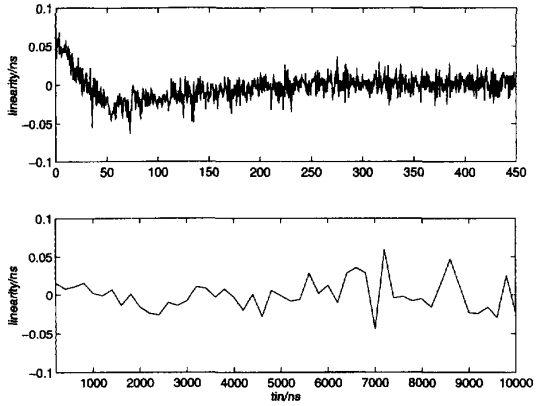

Fig. 11. Measured linearity of the TDC.

B. Linearity

The linearity and stability measurements were made with CMOS-level input time intervals taken from a pulse generator. One hundred samples were averaged per measurement result. Since the pulse generator output was known to be nonlinear, the same time intervals were also measured with a HP5328A Universal Counter. One hundred thousand samples were averaged to achieve a measurement resolution of 84 ps. The linearity of the TDC was taken as the deviation between the TDC output results and the universal counter results (Fig. 11). The linearity curve for input time intervals 0–450 ns was measured with a 0.5-ns step and for input time intervals 0–10 μs with a 100-ns step. The approximate ±50-ps nonlinearity with small input time intervals is probably due to the arriving stop pulse, which disturbs the measurement of $T1$. From the arrival of the start pulse, it takes 70–80 ns before the digital measurement result $T1$ is ready.

C. Stability

To choose the proper load compensation value, the size and sign of the offset in a circuit has to be measured. In principle, this can be done by measuring known time intervals and detecting the error in the output results of the TDC. However, it is difficult to create time intervals with absolute accuracy in the picosecond range. Thus, a more cumbersome, but perhaps more reliable method was used. Time interval measurements were made in several temperatures with each compensation value, and the one resulting in minimum drift was chosen.

The measured offset level variation in the temperature range −40 to +60°C is 50 ps with both offset compensation methods. The variations due to supply voltage change from 4.5 to 5.5 V were 140 ps and 100 ps with load and switching compensation schemes, respectively. The drifts are due to the amount of offset left untrimmed because of the 200-ps trimming step in the load compensation and the 500-ps gate delays not included in the switching compensation scheme. The measured overall accuracy for one circuit using the switching method for offset compensation is shown in Fig. 12. In practice, the supply voltage accuracy can be expected to be ± 50 mV resulting in an overall drift of 60–70 ps.

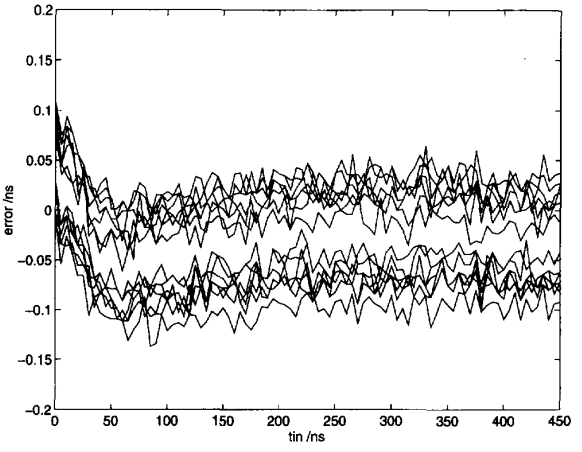

Fig. 12. Measured error due to temperature and supply changes. The error is the difference between the measured and the nominal value, which was measured with 5-V supply voltage at a temperature of +25°C. The upper set of curves was measured with 4.5-V supply at temperatures of +60, +40, +10, 0, −10, −20, and −40°C. The lower set of curves was measured with 5.5-V supply at the same temperatures.

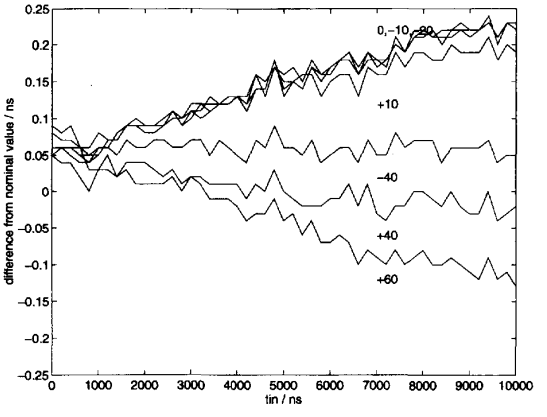

Fig. 13. Effect of temperature dependency of the oscillator on the measurement results at temperatures of +60, +40, +10, 0, −10, −20, and −40°C. Nominal value was measured at the temperature of +25°C.

According to the test results, the crystal oscillator has no noticeable static supply sensitivity in the 4.5 to 5.5 V range. Temperature sensitivity of the oscillator induced a ±200-ps error in the 10-μs measurement range (Fig. 13).

One chip was tested for long-term stability. Eight time intervals were measured repeatedly, once an hour for 66 hours. No drift tendency was apparent in the measurement results. The measurement results are summarized in Table I.

V. Summary

A low-power CMOS time-to-digital converter, TDC, has been presented. The input time interval is roughly digitized with a counter and a 20-MHz crystal oscillator frequency reference. To improve the single-shot resolution, pulse-shrinking delay lines are used as interpolators. The delay elements are adjustable to stabilize the delay in the large temperature (−40 to +60°) and supply voltage (4.5–5.5-V) ranges. Stabilization

TABLE I
MEASURED PERFORMANCE OF THE TDC

PARAMETER	VALUE
lsb width	0.78 ns
input range	10 us
clock frequency	20 MHz
time resolution	σ = 1.25 ns (worst case)
integral linearity error	± 50 ps
temperature sensitivity	50 ps (-40 - +60 °C)
supply sensitivity	100 ps / V
supply voltage	5 V
power consumption	15 mW
chip size	2.9 mm * 2.5 mm

is implemented with a delay-locked loop, which uses the crystal oscillator period as reference.

The single-shot time measurement accuracy of the circuit is ±1.5 ns, which includes both the statistical variation and the systematic linearity and stability errors in the total temperature and supply range. The achievable accuracy after averaging is limited by temperature and supply sensitivities and is ±120 ps in the measurement range 5–500 ns. In the 10-μs range, the final accuracy after averaging is limited by the temperature dependency of the oscillator and is ± 200 ps. The measured power consumption of the circuit is 15 mW.

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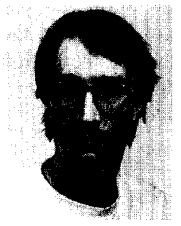

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