

A One Volt Four-Quadrant Analog Current Mode Multiplier Cell

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Abstract—This paper describes a four-quadrant analog multiplier cell that can operate below one volt dc bias. This new multiplier cell is specially designed for low voltage portable communication equipment. The multiplier cell consists of two translinear loops. We have operated this new multiplier cell at as low as 0.8 V. With the exception of the low voltage operation, the output current of the multiplier cell is a true product of the input currents, and there is no limitation on the input dynamic range as with the conventional Gilbert cell.

I. INTRODUCTION

CONSUMER electronics have been the main driving force for lower supply voltage integrated circuits to reduce power consumption and battery size. The ideal supply for most portable audio consumer electronic equipment is a single AA or AAA 1.2-V battery. The Gilbert multiplier cell [1]–[4] has been the most popular multiplier circuit for the past twenty-five years. However, the Gilbert cell cannot be operated with a single 1.2-V supply because of the stack of two saturated collector-emitter junctions and a forward bias base-emitter junction. Thus, there is a need for a new low supply voltage analog multiplier cell. Recently, a design for a low supply voltage analog multiplier cell [5] using unbalanced emitter-coupled pairs was published. This new circuit requires a complex layout to achieve the multiplication function. We propose a new design of a low voltage multiplier cell that requires no complex layout and no limitation on the input dynamic range.

II. NEW CURRENT MODE MULTIPLIER CELL

Fig. 1 illustrates the basic architecture of the new multiplier cell. We use two translinear loops to perform true current mode analog multiplication. Consider the first translinear loop $Q1 - Q2 - Q3 - Q4$

$$\begin{aligned} V_{BE1} + V_{BE4} &= V_{BE2} + V_{BE3} \\ \frac{I_{c1}}{I_{c2}} &= \frac{I_{c3}}{I_{c4}} \end{aligned} \quad (1)$$

Neglecting the base current, then (1) becomes

$$\frac{I_{x1}}{I_{x2}} = \frac{I_{c3}}{I_{c4}} \quad (2)$$

Similarly, consider the loop $Q1 - Q2 - Q5 - Q6$

$$\frac{I_{x1}}{I_{x2}} = \frac{I_{c6}}{I_{c5}} \quad (3)$$

The differential output current ($I1 - I2$) is equal to

$$I1 - I2 = I_{c3} + I_{c5} - I_{c4} - I_{c6}. \quad (4)$$

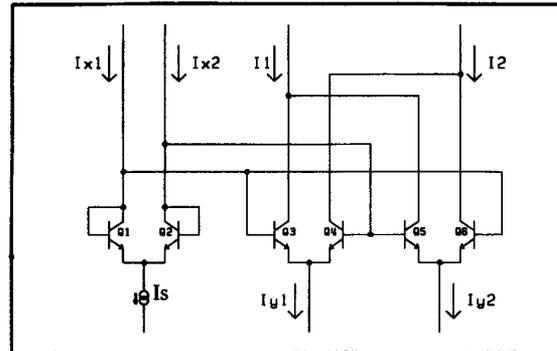


Fig. 1. Two translinear loops multiplier cell.

For

$$I_{y1} = I_{c3} + I_{c4} \quad (5)$$

and

$$I_{y2} = I_{c5} + I_{c6} \quad (6)$$

substitute (5) and (6) into (4)

$$I1 - I2 = I_{y1} + I_{y2} - 2(I_{c4} + I_{c6}). \quad (7)$$

Solve I_{c4} and I_{c6} in terms of I_{x1} , I_{x2} , I_{y1} , and I_{y2} . Then, (7) becomes

$$I1 - I2 = \frac{(I_{y1} - I_{y2})(I_{x1} - I_{x2})}{(I_{x1} + I_{x2})}. \quad (8)$$

Let

$$I_x = I_{x1} - I_{x2}$$

$$I_y = I_{y1} - I_{y2}$$

and

$$I_s = (I_{x1} + I_{x2}).$$

Then, (8) becomes

$$I1 - I2 = \frac{I_x \cdot I_y}{I_s}. \quad (9)$$

The new multiplier cell can perform true four-quadrant multiplication as indicated by (9). The parallel architecture has eliminated the series connected transistors to reduce the supply voltage below 1 V. Unlike, the conventional Gilbert multiplier, which has a severe limitation on the input dynamic range, the new multiplier is a true current mode multiplier, which has no limitation on the input dynamic range.

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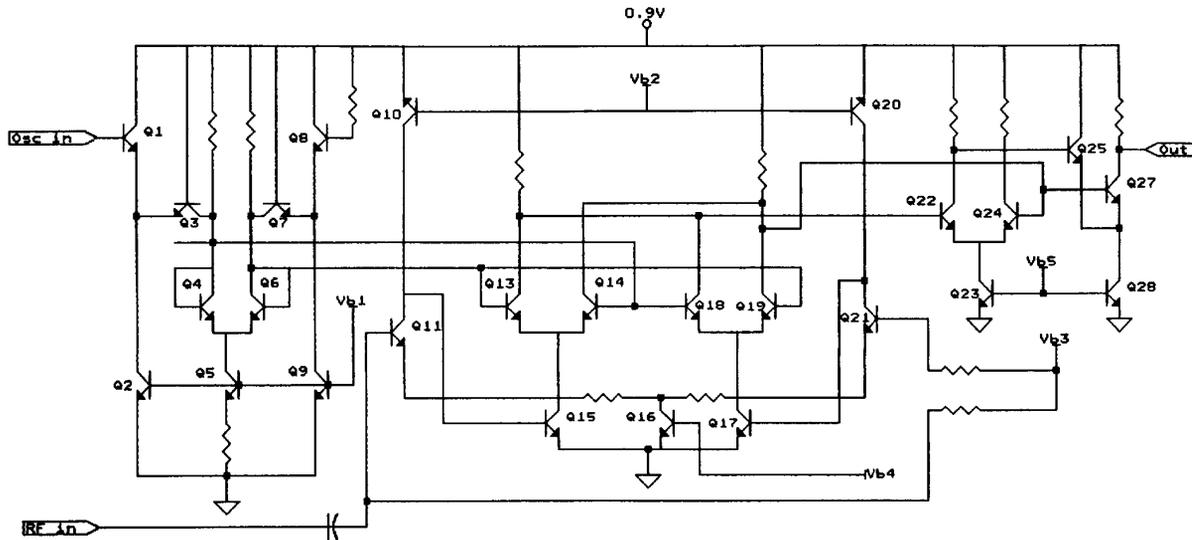


Fig. 2. Schematic diagram of the low voltage FM demodulator circuit.



Fig. 3. Measured input (10 mVpp, 10 MHz) and output (130 mVpp, 44 kHz) waveforms of the test circuit.

III. MEASUREMENT

To further demonstrate the operation of the new multiplier cell, we have built a 0.9-V FM demodulator using the new multiplier cell. A schematic diagram of the test circuit is shown in Fig. 2. Transistors *Q*4, *Q*6, *Q*13, *Q*14, *Q*18, and *Q*19 form the two translinear loops multiplier cell. The voltage to current interface circuit to the local oscillator is composed of transistors *Q*1, *Q*3, *Q*7, and *Q*8. The RF input interface circuit consists of an active-load differential amplifier (*Q*10, *Q*11, *Q*20, and *Q*21) with degenerate resistors to enhance linearity. With a 0.9-V dc bias, the multiplier circuit

consumes 0.5 mA. The RF input is a 10 MHz, 10 mVpp signal, and the local oscillator input is at 10.45 MHz with a peak-to-peak voltage of 42 mV. The output of the FM demodulator is a 450 kHz IF signal with a peak-to-peak magnitude of 160 mV. The conversion gain of the FM demodulator is 33 dB. The measured input and output waveforms are shown in Fig. 3.

IV. CONCLUSION

We have designed a new low-voltage and low-power analog multiplier cell that is tailor-made for the next generation of portable audio and communication electronics. This new multiplier cell has a very simple architecture that can perform true analog four-quadrant multiplication with no limit on the input dynamic range. A low-voltage FM demodulator circuit is built with this new multiplier cell. The FM demodulator consumes 450 μ W with a conversion gain of 33 dB.

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