CMOS Analog Divider and Four-Quadrant Multiplier Using Pool Circuits

Shen-Iuan Liu and Cheng-Chieh Chang

Abstract—**CMOS divider and four-quadrant multiplier circuits using the pool circuits are presented. Using CMOS differential amplifiers and MOS transistors biased in the saturation region, the new analog divider and multiplier are presented. Experimental and simulation results are given to verify the theoretical analyses. The proposed circuits are expected to be useful in analog signal processing applications.**

I. Introduction

ANALOG CMOS signal processing circuits have received significant attention [1]–[3]. An analog divider is an important building block in analog computation, fuzzy control, and instrumentation [1]–[3], etc. Many analog continuous-time and sampled-data divider circuits have been presented in the literature [4]–[9]. However, using passive resistors or MOS transistors biased in the triode region and operational amplifiers as building blocks to synthesize the division function will limit the high-frequency operation and accuracy of the divider [5], [7], [9]. Moreover, it will also increase the cost, power consumption, and chip areas. Hence, development of an all-MOS analog divider will be beneficial.

Analog CMOS circuits based on the square-algebraic identity can be realized since the squaring function can be obtained from the well-known square-law model of the MOS transistors in saturation [10]–[14]. In this paper, we describe two nonlinear computational circuits, i.e., a divider and a four-quadrant multiplier based on the square-algebraic identity and the pool circuits [10], [11]. Experimental and simulation results are given to demonstrate the feasibility of the proposed circuits. The proposed circuits are expected to be useful in analog signal processing applications.

II. Circuit Description

The basic idea to realize the divider is to utilize the following equation:

$$(a+b)^2-(a-b)^2=4ab\equiv c. \tag{1}$$

If "b" and "c" are assumed to be two different input signals and "a" is an output signal, the division function can be obtained easily. Fig. 1 shows the so-called pool circuit [10], [11]. Assume that all the NMOS devices in Fig. 1 are biased in the saturation region with individual wells connected to their sources to eliminate the body effect. Let the transconductance parameter and the threshold voltage of M_1 through M_4 be equal to K and V_T, respectively. I_{B1} $(=I_B)$ and I_{B2} $(=I_B)$ are two dc current sources. The currents I_1 and I_2 in the pool circuit can be given as

$$I_1=K(v_1-v_o)\sqrt{\frac{2I_B}{K}-(v_1-v_o)^2} \tag{2}$$

and

$$I_2=K(v_2-v_3)\sqrt{\frac{2I_B}{K}-(v_2-v_3)^2}. \tag{3}$$

Therefore, at the equilibrium state

$$v_o=v_1+v_2-v_3. \tag{4}$$

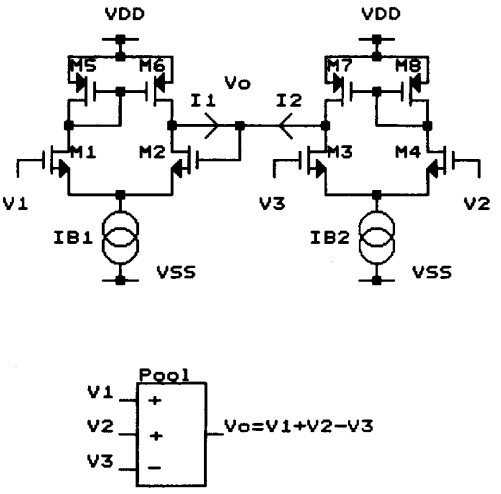

Fig. 1. The pool circuit proposed by Tsay and Newcomb.

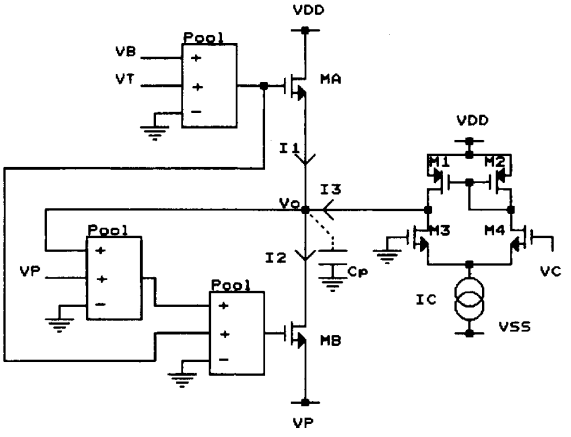

Fig. 2. The proposed divider.

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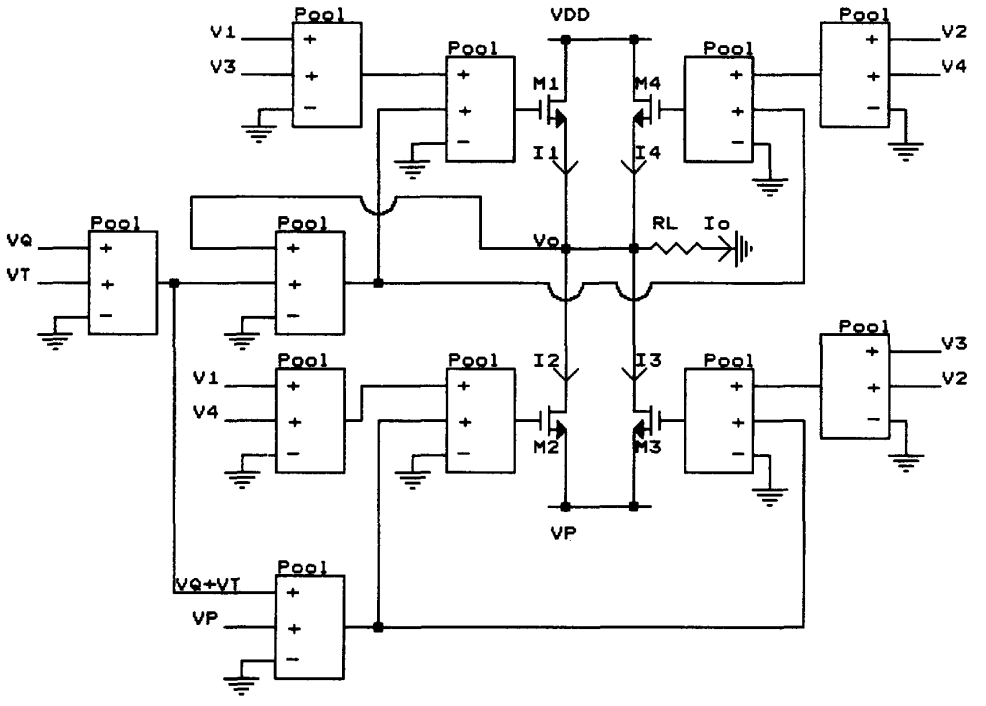

Fig. 3. The proposed four-quadrant multiplier.

This circuit operates as a pool [11] in the sense that the currents flowing in and flowing out are in equilibrium at the output node v_o. One can obtain the addition and subtraction functions from Fig. 1. The proposed CMOS divider consisting of three pool circuits, one CMOS transconductance amplifier and two NMOS devices is shown in Fig. 2. The threshold voltage V_T can be generated by V_T extractor in [15]. The gate-to-source voltages of the devices M_A and M_B in Fig. 2 can be expressed as

$$V_{GSA} = V_B - V_o + V_T \tag{5a}$$

and

$$V_{GSB} = V_B + V_o + V_T \tag{5b}$$

where V_B is an input signal (i.e., divisor) of the proposed divider, V_T is the threshold voltage of M_A and M_B. Assume that K_A is the transconductance parameter of M_A and M_B. The drain currents of M_A and M_B can be obtained as

$$\begin{aligned} I_1 - I_2 &= K_A(V_B - V_o)^2 - K_A(V_B + V_o)^2 \\ &= -4K_A V_B V_o. \end{aligned} \tag{6}$$

The current I_3 can be approximated as

$$I_3 \cong g_m V_C \quad \text{if} \quad \frac{2I_C}{K_C} \gg V_C^2 \tag{7}$$

where $g_m = \sqrt{2K_C I_C}$, K_C is the transconductance parameter of the devices M_3 and M_4 in Fig. 2 and I_C is the dc current source. V_C is also an input signal (i.e., dividend). Therefore, a division operation can be obtained with

$$V_o = \frac{g_m V_C}{4K_A V_B}. \tag{8}$$

The following condition should be satisfied for proper operation:

$$-V_B < V_o < V_B \quad \text{if} \quad V_B > 0. \tag{9}$$

If a parasitic capacitor C_p exists at the output node V_o, then (8) can be rewritten as

$$V_o = \frac{g_m V_C}{sC_p + 4K_A V_B}. \tag{10}$$

To be stable for this circuit, the pole of this circuit must be in the left-hand plane (LHP), which indicates that $V_B > 0$.

According to (1), if "a" and "b" are two different inputs and "c" is the output, one can obtain the multiplication function easily. The proposed four-quadrant multiplier is shown in Fig. 3. The addition of various voltages at the gates of devices M_1–M_4 can be realized by the pool circuits similarly. The output current I_o of this four-quadrant multiplier can be given as

$$\begin{aligned} I_o &= I_1 + I_4 - I_3 - I_2 \\ &= K(v_1 + v_3 + V_Q)^2 + K(v_2 + v_4 + V_Q)^2 \\ &\quad - K(v_2 + v_3 + V_Q)^2 - K(v_1 + v_4 + V_Q)^2 \\ &= 2K(v_1 - v_2)(v_3 - v_4) \end{aligned} \tag{11}$$

where V_Q is the dc voltage and K and V_T are the transconductance parameter and the threshold voltage of the devices M_1–M_4 in Fig. 3, respectively.

III. Performance Analysis

Our analysis of the proposed circuits was based so far on the assumption that all the transistors are characterized by the perfect square-law equation. However, the second-order effects of the devices will degrade the performance of the proposed circuits. The effect of the channel length modulation can be reduced by using the long channel transistors (i.e., $L > 10$ μm). In this section, the second-order effects such as mobility reduction and transistor mismatch are described separately.

A. Pool Circuit Error

Considering the pool circuit shown in Fig. 1, assume that the aspect ratios of M_1 and M_2 are equal to $K + \Delta K/2$ and those of M_3 and M_4 are equal to $K - \Delta K/2$. If the dc current sources $I_{B1} = I_B + \Delta I/2$ and $I_{B2} = I_B - \Delta I/2$, one can obtain

$$v_o \cong v_1 + (v_2 - v_3)\left(1 - \frac{\Delta I}{2I_B} - \frac{\Delta K}{2K}\right). \tag{12}$$

Simulation results show that 5% change of K contributes to 1% linearity error of v_o and 5% change of I_B contributes to 2% linearity error of v_o. The gain error of the pool circuit can be improved by increasing the bias current I_B and K.

B. Mobility Reduction

The simplified *I-V* characteristic of a NMOS transistor operated in the saturation region can be modeled [16] by

$$I_D = \frac{K(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)} \tag{13}$$

where θ is the mobility degradation parameter, which has a value of 0.15 V^{-1} in our simulations. According to (6), (7), and (13), (8) can be rewritten as

$$V_o \cong \frac{g_m V_C}{4K_A V_B - 6\theta K_A V_B^2} \quad \text{if} \quad V_B \gg \frac{\theta V_o^2}{2} \tag{14}$$

where the higher order terms of θ are neglected. Equation (14) indicates that mobility reduction effect will result in the errors of the denominator. Simulation results show that 5% change of θ_n for M_A and M_B results in 4% linearity error of v_o for $0 < V_B < 1$ V and $V_C = 0.35$ V.

C. Transistor Mismatch

Assume that the transconductance parameters of M_A and M_B, shown in Fig. 2 are equal to $K_A + \Delta K_A/2$ and $K_A - \Delta K_A/2$, respectively. Equation (8) can be rewritten as

$$V_o \cong \frac{g_m V_C + \Delta K_A V_B^2}{4K_A V_B}. \tag{15}$$

Equation (15) indicates that such transistor mismatches will result in the errors of the numerator. Simulation results show that 5% change of K_A for M_A and M_B results in 7% linearity error of v_o for $0 < V_B < 0.8$ V and $V_C = 0.35$ V.

TABLE I
THE ASPECT RATIOS OF THE DEVICES IN FIGS. 1–3

Device	M_1–M_4 in Fig. 1	M_5–M_8 in Fig. 1	M_A, M_B in Fig. 2	M_1–M_4 in Fig. 3
W/L (μm/μm)	10/30	60/10	10/10	10/40

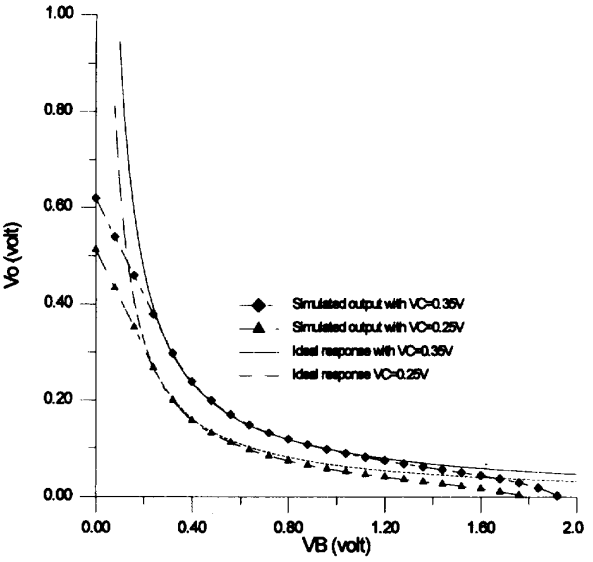

Fig. 4. The simulated transfer curves of Fig. 2 with $V_C = 0.35$ V and 0.25 V.

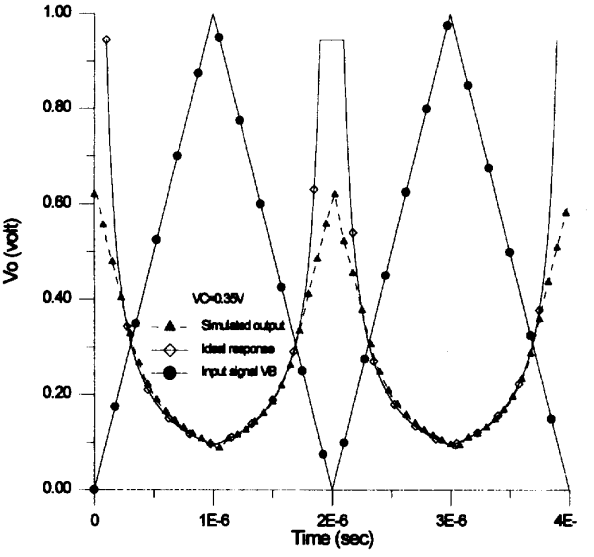

Fig. 5. A typical output waveform of Fig. 2 where a 0.5 MHz triangular signal changing from 0–1 V is applied to V_B and $V_C = 0.35$ V.

IV. Simulation and Experimental Results

The performance of the proposed CMOS divider and four-quadrant multiplier was verified by SPICE simulations. They

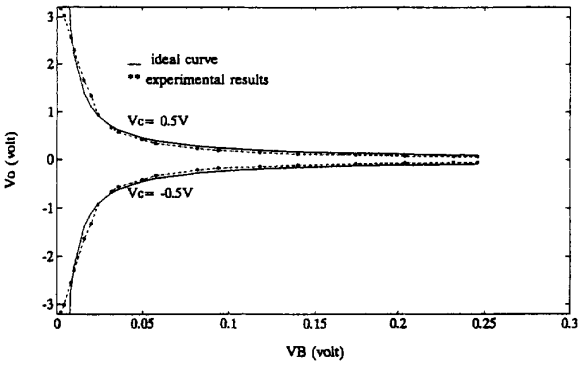

Fig. 6. The dc transfer functions of Fig. 2 with $V_C = 0.5$ V and -0.5 V.

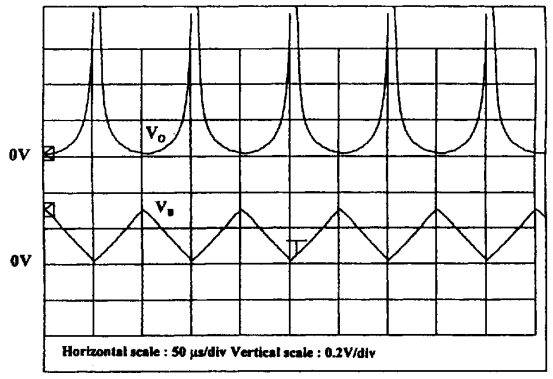

Fig. 7. A typical output waveform of Fig. 2 where V_B is a 0.28 V_{p-p} triangular signal of 10 kHz with 0.14 V dc offset voltage. The horizontal scale is 50 μs/div and the vertical scale is 0.2 V/div.

are obtained with 2-μm p-well parameters and MOSFET transistors with $V_{Tn} = 0.99$ V, $V_{Tp} = -0.8$ V, $K_n = 61.3$ μA/V^2, $K_p = 25.9\mu$A/V^2, $\theta_n = 0.15$ V^{-1}, and $\theta_p = 0.04$ V^{-1}. The aspect ratios for all the devices in Figs. 1–3 are listed in Table I. For the divider in Fig. 2, the simulation conditions are: power supply is ± 5 V, $V_T = 1$ V, $V_P = -1.95$ V, and $I_{B1} = I_{B2} = I_B = 59.4$ μA for pool circuits. The simulated transfer curves are shown in Fig. 4. The linear region for V_B is from 0.3–0.8 V with the linearity error less than 1%. Its -3-dB bandwidth was also simulated to be 9 MHz. A 0.5 MHz triangular signal that changes from 0–1 V is applied to V_B in Fig. 2 and $V_C = 0.35$ V. Its output waveform compared with the ideal one is shown in Fig. 5. To verify the functionality of the proposed divider, we implemented the circuit in Fig. 2 by using 15 CMOS transistor arrays (CD4007). The power supply is ± 5 V, $V_T = 1$ V, $V_P = -4$ V, and $I_{B1} = I_{B2} = I_C = I_B = 0.5$ mA. V_B is a 0.28 V_{p-p} triangular signal of 10 kHz with a 0.14 V dc offset voltage. The transfer curves of Fig. 2 are shown in Fig. 6 with $V_C = 0.5$ V and -0.5 V, respectively. Fig. 7 shows the typical output waveform of Fig. 2 with $V_C = 0.5$ V.

The dc transfer functions of the proposed four-quadrant multiplier in Fig. 3 are also simulated and given in Fig. 8 with $V_1 = -V_2$ and $V_3 = -V_4$. The simulation conditions are: power supply is ± 5 V, $V_T = 1$ V, $V_P = -1.95$ V, $V_Q =$ 1 V, and $R_L = 20$ KΩ. The input range with linearity error less than 1% is up to ± 1.3 V. The total harmonic distortion is less than 1% with input range up to ± 1 V. Its -3-dB bandwidth is about 7 MHz.

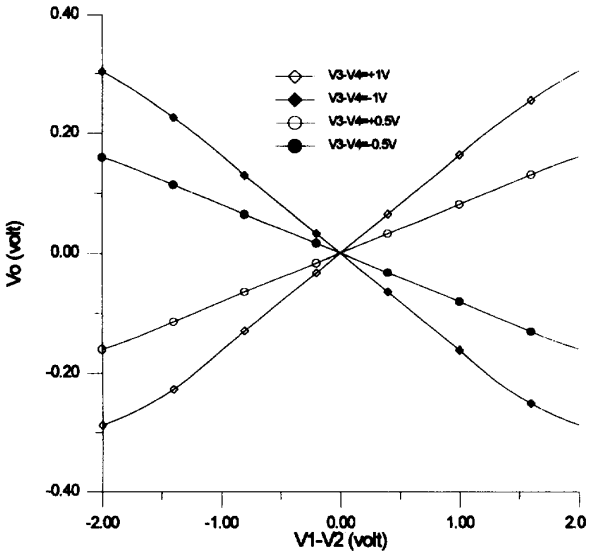

Fig. 8. The dc transfer curves of the proposed multiplier in Fig. 3 with $V_1 = -V_2, V_3 = -V_4, V_Q = 1$ V, $V_T = 1$ V, and $R_L = 20K\Omega$. $V_3 - V_4$ changes from -1 to 1 V and $V_1 - V_2$ changes from 2 to -2 V.

V. Conclusion

New analog CMOS divider and four-quadrant multiplier circuits using pool circuits are developed in this paper. Experimental and simulation results have been given to demonstrate the feasibility of the proposed circuits. The results are expected to be useful in the analog signal processing applications.

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References

[1] C. Mead and M. Ismail, *Analog VLSI Implementation of Neural Systems*. Norwell, MA: Kluwer, 1989.
[2] D. H. Sheingold, Ed., *Nonlinear Circuit Handbook*. Norwood, MA: Analog Devices, 1974.
[3] T. Yamakawa, "High-speed fuzzy controller hardware system: The mega-FIPS machine," *Inform. Sci.*, vol. 45, pp. 113–128, 1988.
[4] E. Sanchez-Sinencio, J. Ramirez-Angulo, B. Linares-Barranco, and A. Rodriguez-Vazquez, "Operational transconductance amplifier-based nonlinear function synthesis," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1576–1586, Dec. 1989.
[5] D. Ghosh and D. Patranabis, "A simple analog divider having independent control of sensitivity and design condition," *IEEE Trans. Instrum. Meas.*, vol. 39, pp. 522–526, June 1990.
[6] Th. L. Laoppoulos and C. A. Karybakas, "A simple analog division scheme," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 779–782, Aug. 1991.
[7] N. I. Khachab and M. Ismail, "A nonlinear CMOS analog cell for VLSI signal and information processing," *IEEE J. of Solid-State Circuits*, vol. 26, pp. 1689–1698, Nov. 1991.
[8] P. Aronhime, M. Desai, and J. Stephens, "Quotient circuits employing VVR," *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 679–684, Oct. 1992.

[9] S. I. Liu, D. S. Wu, H. W. Tsao, J. Wu, and J. H. Tsay, "Nonlinear circuit applications with current conveyors," *IEE Proc.-G*, vol. 140, pp. 1–6, Feb. 1993.

[10] R. R. Torrance, T. R. Viswanathan, and J. V. Hanson, "CMOS voltage to current transducers," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 1097–1104, Nov. 1985.

[11] S. W. Tsay and R. Newcomb, "A neuro-type pool arithmetic unit," in *Proc. IEEE ISCAS'91 (Singapore)*, 1991, pp. 2518–2521.

[12] H. J. Song and C. K. Kim, "An MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers," *IEEE J. Solid-State Circuits*, vol. 25, pp. 841–847, June 1990.

[13] S. I. Liu and Y. S. Hwang, "CMOS four-quadrant multiplier using bias-offset crosscoupled pairs," *Electron. Lett.*, vol. 20, pp. 1737–1738, Sept. 1993.

[14] S. P. Singh, J. V. Hanson, and J. Vlach, "A new floating resistor for CMOS technology," *IEEE Trans. Circuits Syst.*, vol. 36, pp. 1217–1220, Sept. 1989.

[15] Z. Wang, "Automatic V_T extractors based on an $n \times n^2$ MOS transistor array and their application," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1277–1285, Sept. 1992.

[16] S. Wong and C. A. Salama, "Impact of scaling on MOS analog performance," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 106–114, Feb. 1983.