Low-Power Chip Interconnection by Dynamic Termination

Takayuki Kawahara, Masashi Horiguchi, Jun Etoh, Tomonori Sekiguchi, Katsutaka Kimura, and Masakazu Aoki

Abstract— **A low-power dynamic termination scheme is proposed and demonstrated as a way to reduce power dissipation for high-speed data transport. In this scheme, the transmission lines are terminated only if the signals change. The gate of a switching MOS transistor connected to a termination resistor is driven by differentiating the transmission signal with a resistor and a capacitor. The power dissipation of the terminating resistor can be reduced to 1/5 in the conventional dc termination scheme, and overshoot can be reduced to 1/5 that in the open scheme. This scheme is promising for use with palm-top equipment, facilitating high-speed low power operation.**

I. Introduction

THE operating frequency of microprocessor units (MPU's) will soon exceed 100 MHz. At this frequency, data transmission via conventional Transistor Transistor Logic (TTL) and Low Voltage Transistor Transistor Logic (LVTTL) interfaces is impossible. This is because of its large switching power dissipation due to the large voltage signal swing and its large signal distortion due to reflection inherent in the open transmission line scheme. Therefore, a small-swing signal on a transmission line with termination [2], [3] seems suitable for use in high-speed PC's.

However, the power dissipation of this scheme is still large for high-speed palm-top digital equipment operated with a small battery capacity. The power dissipation in a terminated environment is mainly related to the dc path between the power supply of the transmission line driving circuit and the termination. Fig. 1 shows that the power dissipation depends little on the operating frequency.

The power dissipation in the driver P_{DD} and termination circuits P_{DT} in the terminated LVTTL scheme are approximately expressed as

$$P_{DD} = I_{OL} \cdot V_{OL} \cdot \left(1 - \frac{\text{duty}}{100}\right) + |I_{OH}| \cdot V_{OH} \cdot \frac{\text{duty}}{100} + \frac{1}{2} f C_O \cdot V_{sig}^2 \quad (1)$$

$$P_{DT} = R_T \cdot I_{OL}^2 \cdot \left(1 - \frac{\text{duty}}{100}\right) + R_T \cdot I_{OH}^2 \cdot \frac{\text{duty}}{100} \quad (2)$$

where V_{OL} and V_{OH} are the low and high levels of the signal, I_{OL} and I_{OH} are the current at those levels, duty is the ratio (%) when the signal is at the high level, f is the operating frequency of system clock, C_O is parasitic capacitance on the transmission line, and V_{sig} is the voltage amplitude of the signal. Other interfaces are also examined using same type equations. According to these equations, 90% of total power dissipation in Gunning Transceiver Logic (GTL) or Center Tapped Termination (CTT) is related to dc at 100 MHz, and 50% of it is related to dc at 1 GHz (Fig. 1).

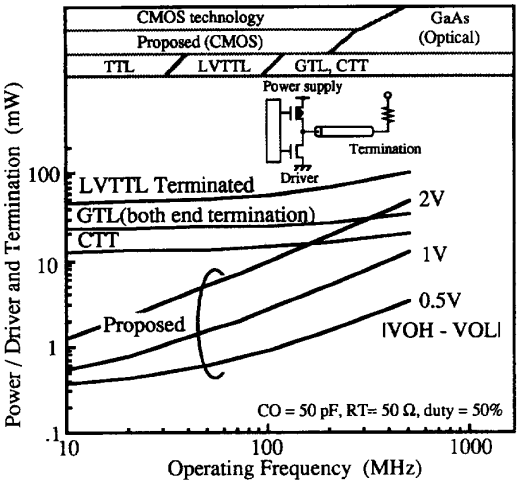

Fig. 1. Power comparison of interface circuits with termination.

This paper therefore proposes a low-power termination scheme called dynamic termination, in which the transmission lines are terminated only if the signals change. This scheme simultaneously reduces both the signal reflection by impedance matching and power dissipation by termination because it eliminates the dc current.

The concept of dynamic termination and actual circuits employing this concept are described in Section II. The performance of the proposed circuit is discussed in Section III, and some experimental results are shown in Section IV.

II. Circuit and Operation

The concept of dynamic termination is illustrated in Fig. 2. It features a variable resistor RT that changes its resistance to match that of the characteristic impedance of the transmission line in the transient state of the signal and remains at high impedance in other states. This scheme reduces power dissipation because the current from the termination voltage VTT flows only during the transient state. Furthermore, reflection is reduced by matching the resistance of the transmission line (its characteristic impedance) to that of RT in the transient state. The output voltages are determined by V_{OH} and V_{OL} at the output buffer.

Fig. 3 shows the proposed dynamic termination circuits used in this scheme. These are composed of terminating resistors

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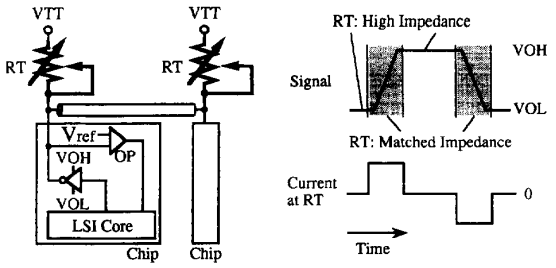


Fig. 2. Concept of dynamic termination.

$RT1$ and $RT2$, switching MOS/bipolar transistors connected to the terminating resistors, and capacitors and resistors to control the switching gates/bases. The CMOS scheme using MOS transistor switches, shown in Fig. 3(a), is suitable for medium-large voltage swing on the transmission line. The BiCMOS scheme using bipolar transistor switch, Fig. 3(b), is suitable for small voltage swing.

In the CMOS scheme, the proposed circuit is composed of terminating resistors $RT1$ and $RT2$, switching MOS transistors $M1$ and $M2$, and control circuits for the resistors $R1$ and $R2$ and capacitors $C1$ and $C2$. The terminating voltages are V_{OH} for $RT1$ and V_{OL} for $RT2$. The resistance of both $RT1$ and $RT2$ is set to match the characteristic impedance of the transmission line when they are added to the ON resistances of $M1$ and $M2$, respectively.

Operation proceeds as follows. When a signal on the transmission line is at V_{OL}, the gate voltage of MOS $M2$ is V_{OL}. Because the source voltage, which is connected to $RT2$, is also V_{OL}, $M2$ is OFF. And $M1$ is also OFF because the gate and the source voltages are both V_{OH}. There is no current flow. When the signal changes from V_{OL} to V_{OH}, the voltage at $N2$ rises due to capacitor coupling. If this level is higher than $V_{OL}+V_{th}$, where V_{th} is the threshold voltage of $M2$, $M2$ turns ON. In this state, the resistor, which is located between the termination voltage V_{OL} and the transmission line, has a total resistance equal to the sum of the ON resistance of $M2$ and the resistance of $RT2$. The transmission line is terminated by this serial resistance. $N2$ then decays to V_{OL} with a time constant determined by $C2$ and $R2$. $M2$ remains ON, at increasing resistance, until $N2$ drops below $V_{OL}+V_{th}$. The gate of the $M2$ is operated by signals generated by a simple circuit having a resistor and a capacitor that differentiates the signal. This part is well-known RC differentiator. Moreover, the gate voltage $N1$ of $M1$ rises above V_{OH} due to the capacitor coupling of $C1$. However, since the source voltage remains at V_{OH}, $M1$ remains OFF.

Next, the signal changes from V_{OH} to V_{OL}, and $N1$ is reduced due to the capacitor coupling of $C1$. When this level is lower than $V_{OH}-|V_{th}|$, where V_{th} is the threshold voltage of $M1$, $M1$ turns ON. Thus, $M1$ and $RT1$ provide dynamic termination for falling signals in a way similar to $M2$ and $RT2$ for rising signals.

In this way, the power is reduced because the current flows only when the signal changes. Note that if the threshold voltage of $M1$ and $M2$ is 0 V, smaller voltage swings can operate the switching MOS transistors.

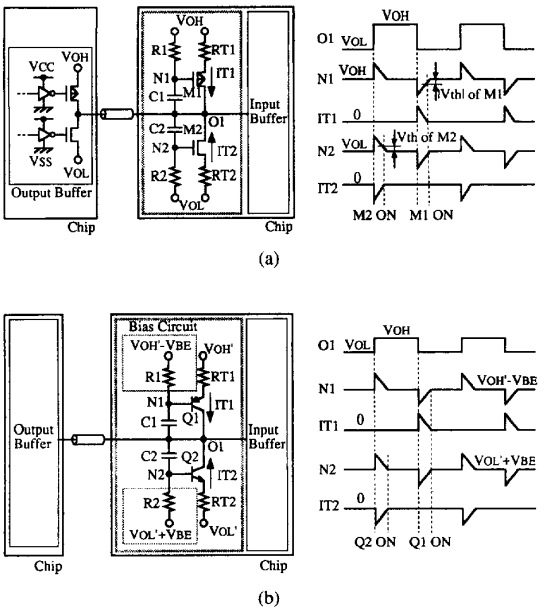


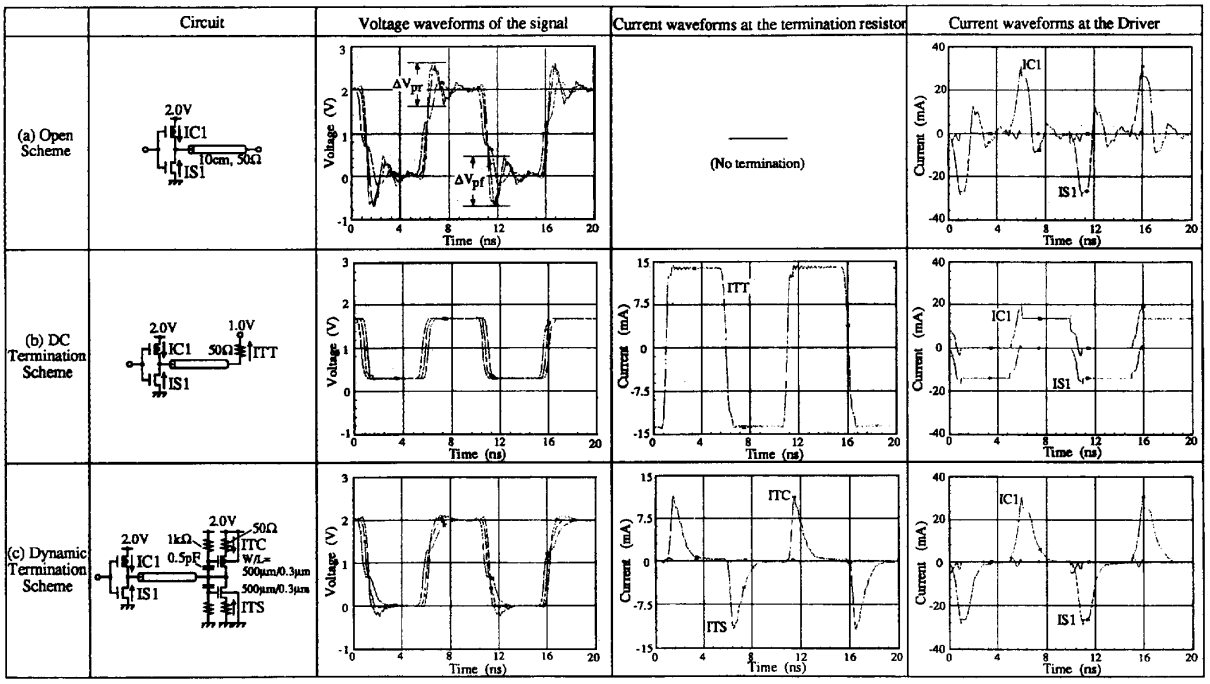
Fig. 3. Circuit structure and operation. (a) CMOS scheme. (b) BiCMOS scheme.

The BiCMOS dynamic termination circuit is composed of terminating resistors $RT1$ and $RT2$, the bipolar switching transistors $Q1$ and $Q2$, and control circuits of the resistors $R1$ and $R2$ and capacitors $C1$ and $C2$. $R1$ and $R2$ can be connected to the base voltage bias circuit for high performance. The terminating voltages are V'_{OH} for $RT1$ and V'_{OL} for $RT2$. These can be set to different voltages than V_{OH} and V_{OL}, which determine the voltages at the output buffer. The resistance of both $RT1$ and $RT2$ is set to match the characteristic impedance with the ON resistances of $Q1$ and $Q2$, respectively. The BiCMOS scheme operates in the same way as the CMOS scheme. The bases of the bipolar switching transistors $Q1$ and $Q2$, which are connected in series to the terminating resistors $RT1$ and $RT2$, are operated by differentiating the transmission signal. This scheme facilitates a small voltage swing because the current changes exponentially relative to the base voltage if the base-emitter voltage is biased a little below V_{BE}. To prevent the saturation of the bipolar transistors, the termination voltages V'_{OH} and V'_{OL} can be different from the driver voltages of V_{OH} and V_{OL}.

III. Performance of the Proposed Circuit

The voltage waveforms on the transmission line and the current through the terminating resistor of the proposed scheme are compared to those of the open scheme and the dc termination scheme to determine relative performance by circuit simulation. We assume characteristic impedance of 50 Ω on the transmission line, a 10-cm transmission-line length, and point-to-point transmission. The operating frequency is 100 MHz. This is assumed to be a system with direct data transport between the MPU and memory in palm-top equipment for the high-speed operation required to handle digital moving-pictures.

TABLE I
SIMULATED WAVEFORMS



The voltage waveforms related to the open scheme are shown in Table I(a). The three waves represent the sending point, mid-point, and receiving point. Large waveform distortions emerge because of reflections at the unterminated receiving end of the transmission line. The amplitude from top to bottom of the first overshoot ($\Delta V_{\rm pr}$) is 0.98 V and that of the first undershoot ($\Delta V_{\rm pf}$) is 1.16 V. The current in the driving circuit is distorted due to the reflections. The voltage waveforms of the signal and current waveforms related to dc termination are shown in Table I(b). There is no distortion in the voltage waveforms because of the matched termination voltage under point-to-point transmission. However, the current at the terminator (ITT) is 13 mA, which flows forward or backward, according to the signal. The current in the driver is also as large as that in the termination. Thus, the open scheme has large waveform distortion and the dc termination scheme has large power dissipation.

In contrast, the proposed dynamic termination scheme reduces both the distortion and the power, as shown in Table I(c). In the voltage waveforms, the amplitude of the first overshoot is 0.12 V and that of the first undershoot is 0.25 V. This is 1/5 that of the open scheme. Moreover, the current flows only when the signal is changed. The average current is 1.24 mA (ITC: terminating at $V_{\rm OH}$) and 1.37 mA (ITS: terminating at $V_{\rm OL}$). This is 1/5 that of the dc termination scheme. The current in the driver consists of the small termination current and the loading-line current. Therefore, data transmission with both small distortion and low power are achieved simultaneously by dynamic termination.

The time constant of the gate-driving circuit is an important design parameter in the proposed scheme. When the time constant is ∞, the termination MOS is always ON. That corresponds to dc termination. On the other hand, when the time constant is 0, the termination MOS immediately turns off. That corresponds to the open scheme. The time constant of $R1C1$ and $R2C2$ should be chosen as follows: Suppose the signal frequency is f. It is reasonable to set the output driver slope smaller than 10% of $1/f$ (cycle time) for reliable high-speed operation. And the time of flight is the same order of this period, which means the termination is needed. The time constant of the gate-driving circuit should set to be around $0.1/f$ where the terminator is active (and the termination current decade exponentially). The drivability of the switching transistor $M1$ and $M2$ determine that the termination is sufficient or not. That depends on the area penalty, gate capacitance overhead, and the process technology. To increase the frequency limit of the proposed scheme needs smaller gate capacitance and larger drivability. This means maximum frequency exists in every process technology step. In 0.3-μm technology, 250 MHz is the maximum frequency. Simulation examples are shown in Fig. 4. The reduction ratios of overshoot and power dissipation are compared to those of the open scheme and dc termination scheme, respectively, in terms of dependence on $R1$ and $R2$, which discharge the gate node. To avoid the influence of diode termination on the overshoot results, the well voltage (VNW) of the pMOS transistor is 1 V higher than $V_{\rm OH}$ and the back-bias voltage (VBB) is 1 V lower than the $V_{\rm OL}$. This was not done in the cases shown in Table I. In diode termination, the voltage overshoot of the transmission line is clamped by the drain/nwell diode of the pMOS $M1$ or the drain/substrate diode of nMOS $M2$. Table I shows the simulation-based real

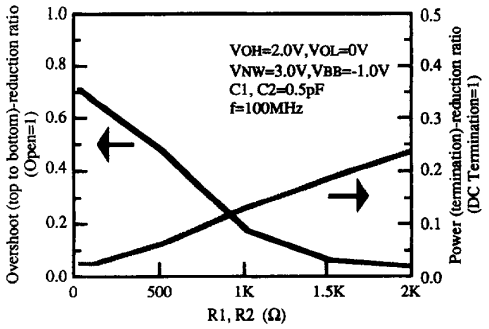


Fig. 4. Reduction of overshoot and power.

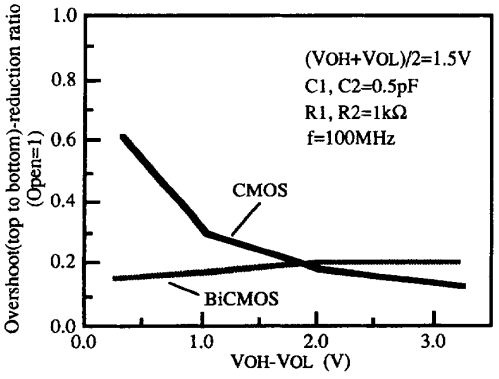


Fig. 5. Efficiency under low voltage swing.

case comparison involving substrate and well diode. In Fig. 4, the smaller $R1$ and $R2$ values correspond to the open scheme, and the larger ones are for dc termination. At $R1$ and $R2 = 1$ kΩ with $C1$ and $C2 = 0.5$ pF, the reduction ratio of overshoot is only 0.2, and the reduction ratio of power dissipation is 0.24. In the actual device, the appropriate RC can be chosen at the wafer test in the factory or on board test while using when some sets of capacitors or resistors are prepared on the chip. The reason that the reflection is not completely absorbed is the finite turn on time. Since the turn on time consists of capacitor coupling time and the cut-off frequency of MOS, the appropriate MOS performance should be chosen according to the operating frequency.

The dependence of the overshoot reduction ratio on the voltage swing of the signal ($V_{OH} - V_{OL}$) is shown in Fig. 5, in the case that $(V_{OH} + V_{OL})/2 = 1.5$ V. The CMOS scheme is useful for voltage swings of over 1.0 V, and the BiCMOS scheme is useful even for swings as small as 0.5 V. Clearly, the proposed simple circuits are useful for small voltage swings.

Another approach to dynamic termination has been proposed [4]. In this scheme, a feedback circuit turns off the termination circuits after the signal is changed. The main advantage of our dynamic termination scheme, as shown in Fig. 3, is its ability to operate under low voltage swing signals [5].

When crosstalk induces voltage on the transmission line, that turns on the termination circuits. The current dissipation itself is increased by this crosstalk. However, since the induced

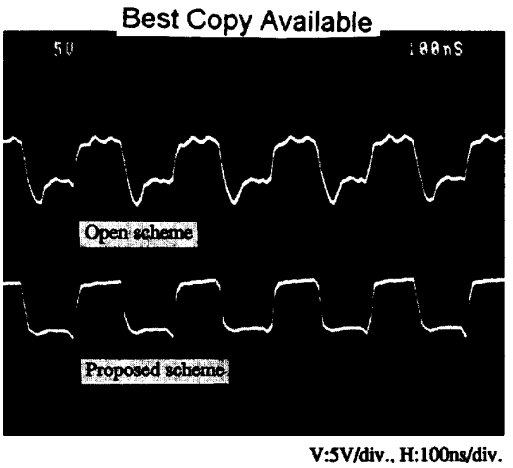


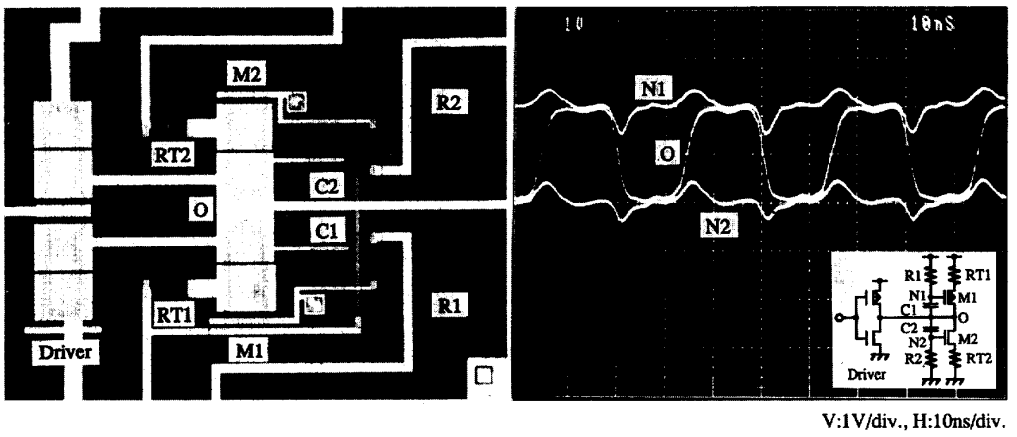
Fig. 6. Measured waveforms of the BiCMOS scheme.

voltage is quickly absorbed by the termination circuit, the increase in power dissipation is small, and the correct signal is kept on the transmission line. That is the same when the glitch noise is emerged on the line. The glitch noise turns on the termination circuit then, but the correct signal is kept.

IV. Experimental Results

To evaluate the proposed circuits, a simple breadboard test was conducted for the BiCMOS scheme (Fig. 6). The transmission line was 3-m long, and f_T of the bipolar transistors was 200 MHz. Comparing the waveforms of the proposed and the open schemes shows that the proposed scheme is effective in reducing overshoots. A simple test circuit was also fabricated using 0.16-μm technology with relaxed lines and spaces (Fig. 7(a)). It contained only an output CMOS driver and the dynamic termination circuit of the CMOS scheme. The gate node of the MOS capacitor was connected to the gate of the termination MOS, and the source and drain were commonly connected to the output of CMOS driver. This scheme is suitable for well and substrate voltages, which are usually equal to V_{OH} and V_{OL}, respectively, when the voltages of the gate nodes of the termination MOS are above V_{OH} or below V_{OL}. The operation waveforms of output from the CMOS driver and the capacitor-coupled gate node at on-wafer measurement are shown in Fig. 7(b). This figure confirms the basic operation of dynamic termination.

A comparison of current for the dc termination and the proposed dynamic termination is shown in Fig. 8. DC termination is estimated when the gate node of the termination MOS is set to the voltage that normally turns on the MOS. The additional power dissipation due to $C1$ and $C2$, which serve no purpose for the dc scheme, is small because there is a little increase on operating frequency from 1–10 MHz. The termination voltage is $V_{CC}/2$ at dc termination. The current under dc termination is four times larger than that under the dynamic termination at 20 MHz. However, the power-reduction ratio is small compared to the simulations shown in Table I and Fig. 4. This is because the values of resistance and capacitance driving the gate node seem to be larger than



(a) (b)

Fig. 7. Measured waveforms of the CMOS scheme. (a) Microphotograph of the test chip. (b) Waveforms.

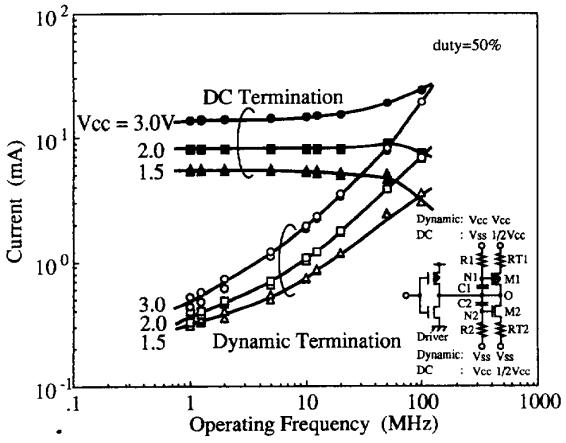


Fig. 8. Measured current comparison.

the designed values. If these values are tuned up, the power-reduction ratio is improved. And the current in dc termination tends to decrease at high frequency under low V_{CC}. This is because the driving ability of the driver under low V_{CC} in dc termination is less than the value needed for the termination resistor. The amplitude of the signal becomes smaller with increasing frequency. Thus, the difference between the signal voltage and the termination voltage is reduced, which means the power is also reduced.

V. Conclusion

A dynamic termination scheme is proposed and demonstrated to reduce power dissipation in high-speed data transport. In this scheme, the transmission lines are terminated only if the signals are changed. The gate/base of a switching MOS/bipolar transistor connected to a termination resistor is driven by differentiating the transmission signal generated by a simple circuit containing a resistor and a capacitor. The power dissipation of the terminating resistor can be reduced to 1/5 that in the conventional dc termination scheme, and overshoot can be reduced to 1/5 that in the open scheme. This scheme is promising for use with palm-top equipment, facilitating the high-speed operation required to handle digital moving pictures with low power requirement.

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