Novel W-Band Monolithic Push-Pull Power Amplifiers

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***Abstract*—Monolithic W-band push-pull power amplifiers have been developed using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic T-gate power HEMT technology. The novel design approach utilizes a push-pull topology to take advantage of a virtual ground between the device pair, eliminating the series feedback of the via hole inductance, and thus improving the performance of power amplifier at millimeter-wave frequencies. For a two-stage design presented in this paper, the measurement results show that a small signal gain of 13 dB, a saturated output power of 19.4 dBm at 90 GHz. The best power added efficiency of 13.3% has been achieved at an output power of 18.8 dBm under a lower bias condition. The gain and efficiency results represent state-of-the-art performance. These are the first reported monolithic push-pull amplifiers at millimeter-wave frequencies.**

I. Introduction

MILLIMETER-WAVE (MMW) power amplifiers (PA's) are key components for transmitters in many systems. The existing MMW monolithic PA designs using microstrip lines from 35–94 GHz [1]–[6] utilize common source HEMT devices with multifingers in parallel and via holes for dc and RF grounding. Since the via hole inductances contribute to source inductance and provide series feedback in the common source HEMT device, the gain performance of this type amplifiers at MMW frequencies is therefore degraded significantly. Consequently, the output power and power added efficiency are affected accordingly, especially at W-band (75–110 GHz) frequencies and higher.

The push-pull PA configuration is well-known for its ability to eliminate the distortion introduced by the nonlinearity of the dynamic transfer characteristic of a transistor in very low frequency ranges [7]. It has been previously used to demonstrate an X-band amplifier in a hybrid MIC form [8]. Using the push-pull scheme has an additional significant advantage through improving the performance of MMW monolithic PA's by eliminating the RF ground inductance. This occurs because of the virtual ground (VG) that exists between the devices in the push-pull HEMT device pair which, in effect, shorts out the via hole inductance. Moreover, the sizes of the baluns required in the push-pull PA design to provide a pair of input signals 180° out of phase are smaller at higher frequencies and thus make this approach more attractive for MMIC design at W-band than at lower frequencies.

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This paper presents the first reported monolithic PA's implemented at MMW frequency with a push-pull scheme using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic (PM) T-gate power HEMT technology. A single-stage and a two-stage PA using different topologies have been designed, fabricated, and tested. The single-stage design demonstrated a small signal gain of 7 dB at 94 GHz. A measured small signal gain of 13 dB is achieved for the two-stage PA at 90 GHz. It also demonstrates 19.4-dBm output power with 7.4-dB saturated gain at 90 GHz. The best power added efficiency (PAE) of 13.3% is achieved at an output power of 18.8 dBm under a lower bias condition. The gain and PAE performance of this two-stage PA represents state-of-the-art results for monolithic W-band PA's. The output power density is 272 mW/mm, which is close to the best discrete device performance reported at this frequency [9]. Moreover, the 0.1-μm AlGaAs/InGaAs/GaAs PM T-gate power HEMT MMIC process used to fabricated these push-pull amplifiers is a production process, as described in [12].

In Section II, the 0.1-μm power HEMT device characteristics and modeling are described. Section III presents the push-pull MMIC PA design. The measured performance and comparison with simulation results are addressed in Section IV and followed by a brief summary.

II. Device Characteristics and Modeling

The W-Band HEMT structure is grown using molecular beam epitaxy (MBE) on 3-in substrates and uses a PM $In_{0.22}Ga_{0.78}As$ channel. The structure shown in Fig. 1 is based on a double heterostructure design originally developed for high efficiency V-band power HEMT's [10] and modified to achieve a high aspect ratio for 0.1-μm gate lengths. The 0.1-μm power HEMT MMIC process has been validated in our HEMT MMIC production line and shares many of the same process steps as the 0.2-μm gate length low noise and 0.15-μm gate length power HEMT production MMIC processes, ensuring high producibility [11]. The devices are passivated with plasma enhanced chemical vapor deposition (PECVD) silicon nitride for good reliability and robustness. Extensive characterization and statistical process control are employed for material analysis, electron beam lithography, metal-insulator-metal (MIM) dielectric thickness and capacitance, metal thickness, linewidth, resistivity, dc, and RF device electrical parameters. The devices typically exhibit gate-to-drain breakdown voltages of 6 V measured at a gate current of 0.1 mA/mm [16], peak dc transconductance of 600 mS/mm, maximum current of 600 mA/mm, unit current gain frequency

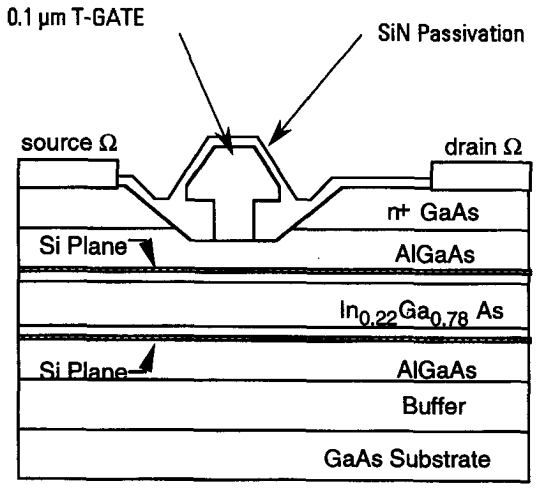
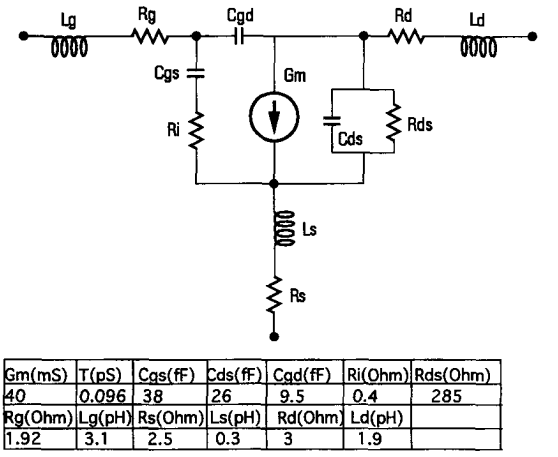


Fig. 1. Device cross section of the 0.1-μm gate planar doped channel PM AlGaAs/InGaAs/GaAs power HEMT.

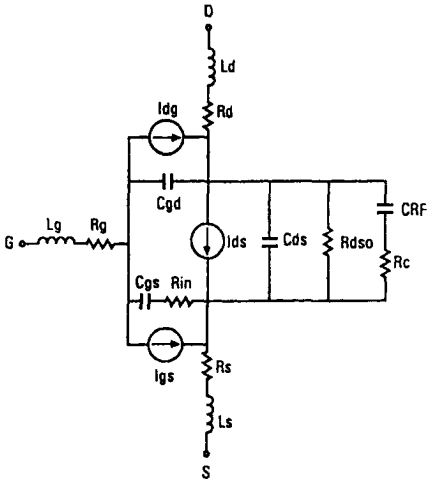
f_T of 110 GHz, and maximum oscillation frequency $f_{\max}$ of greater than 250 GHz at 2-V drain bias [12].

The PA design requires both linear and nonlinear simulations to predict the gain and output power performance. The harmonic balanced technique is used for the nonlinear simulation. The HEMT linear small signal equivalent circuit parameters were obtained from curve fitting of the measured small signal S-parameters up to 50 GHz. Part of these parameters were initially estimated from device physical dimensions and parameters. Certain limits were then set during the curve fitting of the small signal S-parameters to avoid nonphysical parameters in the model. The Curtice–Ettenberg FET asymmetric model was used to describe the HEMT device nonlinear behavior [13]. The nonlinear transconductance coefficients were then obtained from fitting the dc–IV measurement of the HEMT device. Fig. 2 shows both the linear and nonlinear equivalent circuit model and the model parameters of a four-finger HEMT with 80-μm total gate periphery which is used as the unit device cell in the push-pull PA design.



Gm(mS)	T(pS)	Cgs(fF)	Cds(fF)	Cgd(fF)	Ri(Ohm)	Rds(Ohm)
40	0.096	38	26	9.5	0.4	285
Rg(Ohm)	Lg(pH)	Rs(Ohm)	Ls(pH)	Rd(Ohm)	Ld(pH)	
1.92	3.1	2.5	0.3	3	1.9	

(a)



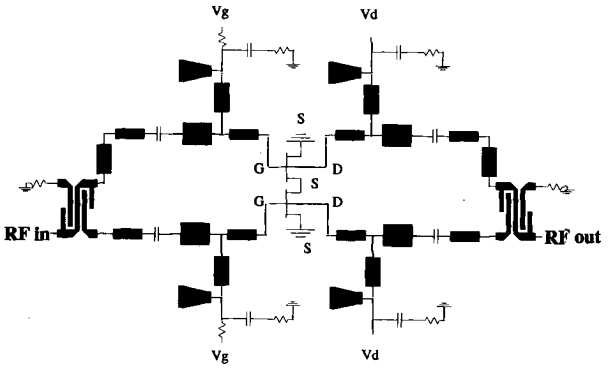
(b)

Fig. 2. The 0.1-μm power HEMT device equivalent circuit model and model parameters. (a) Small signal linear model at 4-V drain bias voltage with 25-mA drain current (near peak dc transconductance). (b) Nonlinear model (Curtice–Ettenberg asymmetric model). a_0 = 0.35325E-01 A, a_1 =0.48567E-01 A/V, a_2 = −0.12554E-01 A/V^2, a_3 = −0.25386E-01 A/V^3 β = 0.82456E-02 V^{-1}, γ = 2.9342 V^{-1}, R_{dso} = 374.62 Ω.

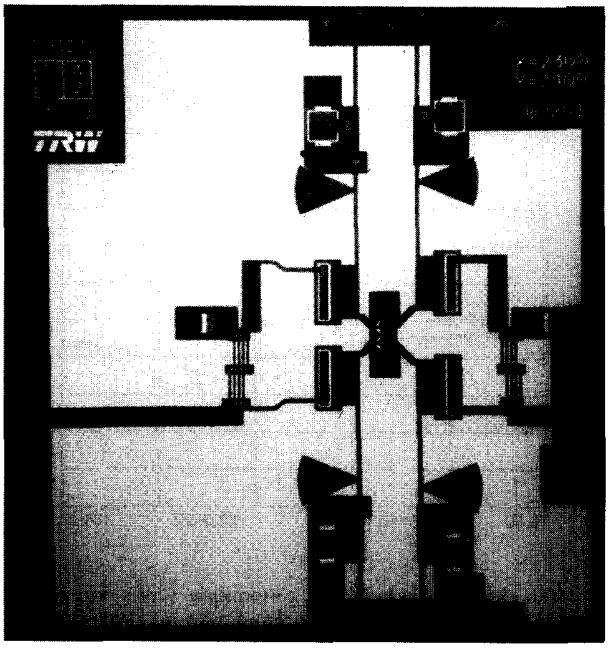
III. Circuit Design

Fig. 3(a) and (b) shows the schematic diagram and photograph of the single-stage amplifier with a chip size of 2.3 × 2.4 mm^2. This single-stage PA utilizes a push-pull HEMT device pair with a total gate width of 160 μm. Due to the advantage from the VG of the push-pull HEMT device pair of eliminating the 30-pH via hole inductance of each via hole, a total of zero ground inductance can be obtained if perfect symmetry is maintained. The maximum stable/available gain of a single four-finger 80-μm gate width common source HEMT is therefore higher than that of the same HEMT grounded with a pair of via holes. The calculated maximum stable gain for the common source device model shown in Fig. 2 without the grounding via hole inductance is 8.8 dB, while the same device model with two parallel grounding via holes only has a maximum available gain of 6.4 dB. Therefore, higher gain and output power are expected for the push-pull design.

The matching circuit in Fig. 3(a) for the single-stage push-pull PA is designed as a trade-off between high gain and high output power based on reactive matching technique. The matching networks for both upper and lower half for the push-pull pair HEMT devices are symmetrical and separated by the VG. They are comprised of cascaded high-low impedance microstrip lines on a 100-μm thick GaAs substrate. MIM capacitors are used for dc blocking, and radial stubs are employed for RF bypassing. Shunt *RC* networks are used in the bias network to ensure low frequency stability, and reactive ion etching (RIE) process is used to fabricate back side via holes for dc grounding. Lange couplers together with 90°-delay microstrip lines are used as the baluns to provide 180° out-of-phase signals for the push-pull amplifier mainly for physical size and layout simplicity concerns. Since the gate and drain pads of two devices in the push-pull pair are isolated from each other, the dc bias must be applied separately. The



(a)

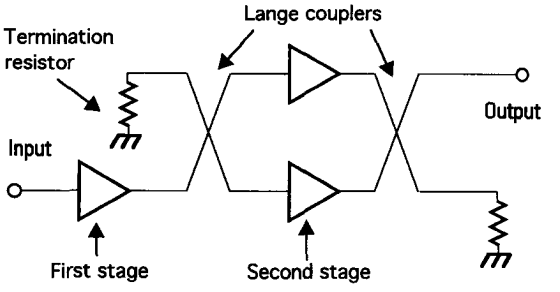


(b)

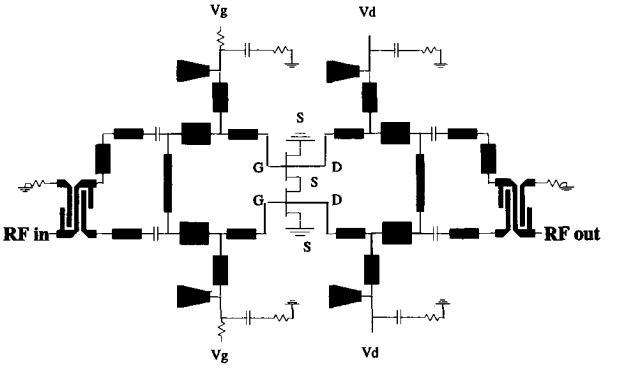
Fig. 3. The (a) schematic diagram. (b) Chip photograph for the single-stage W-band push-pull PA. The chip size is 2.3 × 2.4 mm^2.

two set dc bias networks are designed on both sides of this chip, as shown in Fig. 3(b).

The block diagram of a two-stage design consisting of single-stage push-pull amplifiers with a different matching network topology as building blocks is shown in Fig. 4(a). This PA includes a single-ended push-pull PA as the first stage to drive a balanced push-pull PA output stage. The output stage is constructed by using two identical building blocks and two 90° Lange couplers. Each building block consists of a push-pull HEMT device pair of 160-μm total gate width. Therefore, the first stage has 160-μm total gate periphery and the second stage has 320-μm total gate periphery. The schematic diagrams of the first and second stage are presented in Fig. 4(b) and (c), respectively. These partial circuits have a similar topology as the single-stage PA, as shown in Fig. 3(a), except that a shunt high impedance line is added in the matching network mainly for the dc connection of the push-pull pair of amplifiers so as to enable dc bias from either side of the push-pull amplifier



(a)



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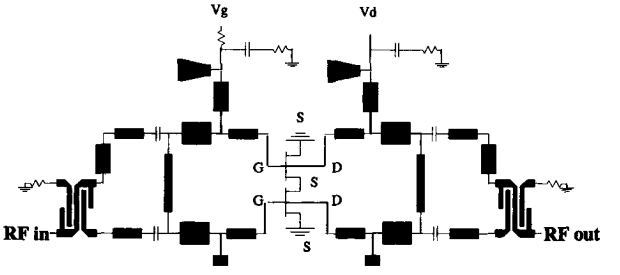
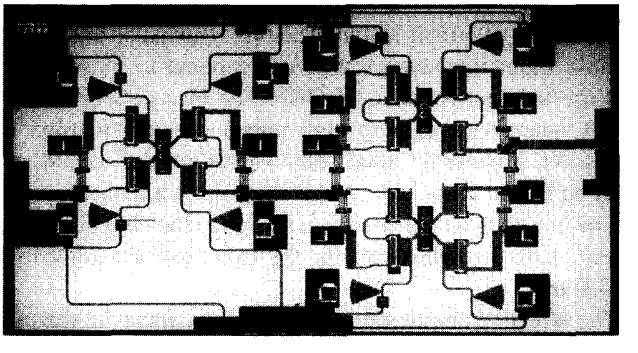


(c)



(d)

Fig. 4. (a) The block diagram of the two-stage push-pull PA. The schematic diagrams of (b) the first stage and (c) the second stage of the two-stage push-pull PA. (d) The chip photograph of the two-stage push-pull PA with chip size of 4.4 × 2.4 mm^2.

building block. The first stage shown in Fig. 4(b) is designed to maintain the symmetry by including the bias networks on both sides of the push-pull cell, while for the second-stage design, as shown in Fig. 4(c), both of the bias networks located on the same side of the push-pull device pair are eliminated for the

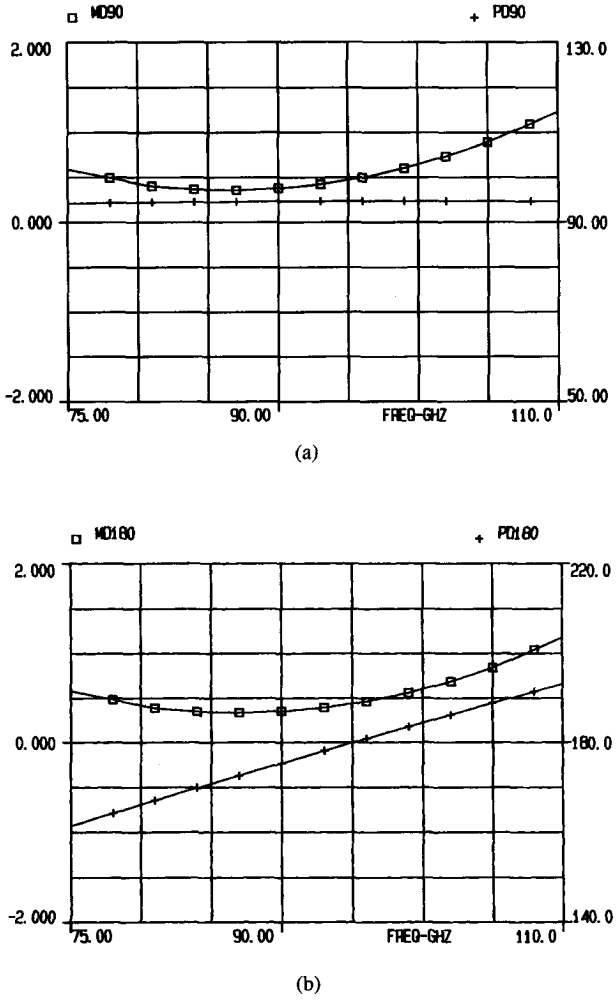


Fig. 5. The (a) amplitude (MD90) and phase imbalances (PD90) of the 90° coupler. (b) Amplitude (MD180) and phase imbalances (PD180) of the 180° coupler used in the circuit simulation from 75–110 GHz. The unit of the axis for magnitude imbalances is dB, while the unit for phase difference is degree.

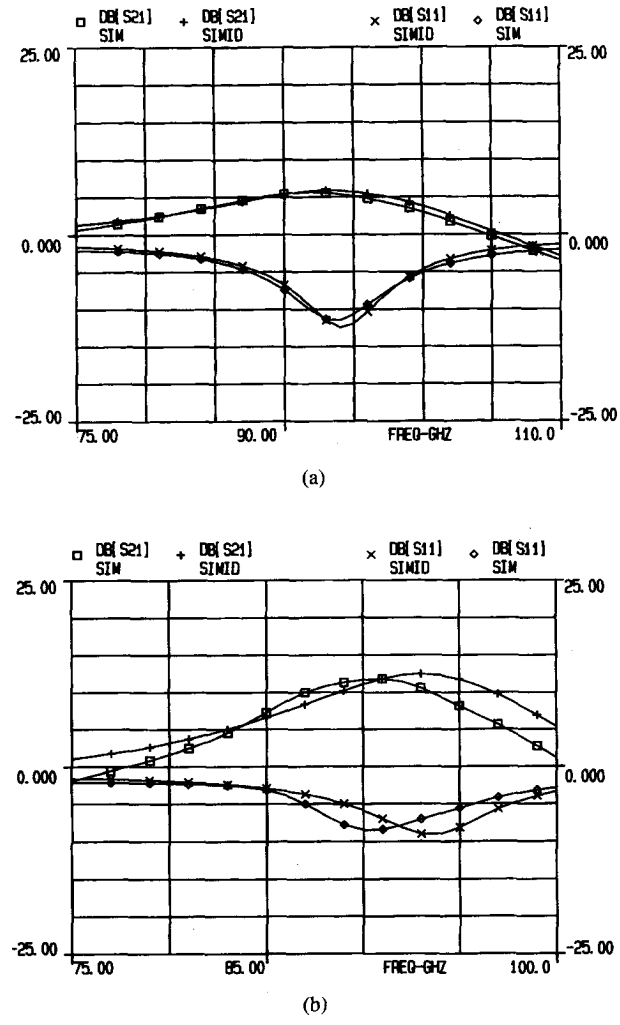
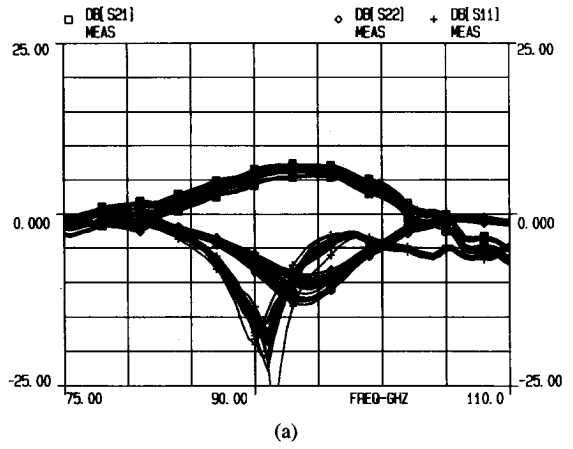


Fig. 6. The simulated push-pull PA performance versus frequency using ideal (SIMID) and nonideal (SIM) couplers for the (a) single-stage and (b) two-stage design.

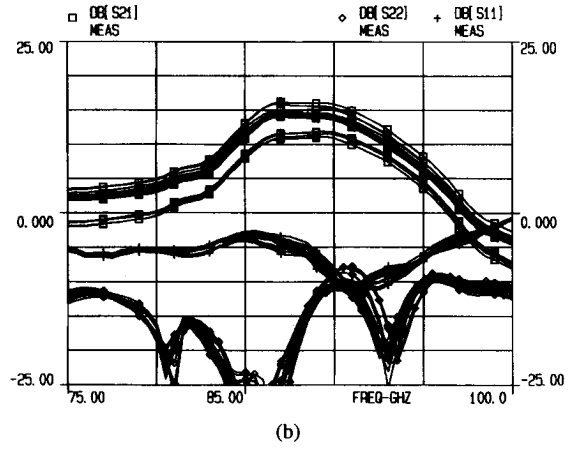
convenience of circuit layout. The tiny open stubs are adjusted to have input impedances that are identical to those looking into the bias networks at 94 GHz. The bias networks have a nearly quarter wavelength high impedance transmission line with a RF grounding radial stub. Therefore, the second stage must be biased from both side of the chip, while the first stage can be biased from either side as shown in the chip photograph in Fig. 4(d). The chip size for the two-stage amplifier is 4.4 $\times$ 2.4 mm^2.

The effect of amplitude and phase imbalances on the push-pull amplifier design has been investigated. Fig. 5(a) and (b) shows the amplitude and phase imbalances of the models for the 90° and 180° 3-dB couplers (Lange coupler and Lange coupler plus a delay line) used in the PA simulations, respectively. For the 90° coupler, there are 0.6–1.1-dB amplitude imbalances from 80–100 GHz, while the phase difference maintain 95° across the entire band. The 180° coupler shows a linear phase difference from 162–194° from 75–110 GHz due to the delay line and has a similar magnitude difference as that of the 90° coupler. The simulated small signal gain and input return loss performances of both the single- and two-stage push-pull PA using these nonideal couplers are compared with those simulated using ideal 90° and 180° couplers as plotted in Fig. 6(a) and (b). It is observed that the frequency response of the single-stage PA is almost unaffected. However, the two-stage design has shown a 2–3 GHz frequency shift. This is attributed to the extra shunt lines in the matching network of the two-stage design that can be offset due to imbalances of the 180° coupler. In addition, this effect can be enhanced for a multiple-stage PA. Therefore, the two-stage design is more sensitive to the amplitude and phase imbalances.

Full-wave EM analysis tool is used for most passive elements to eliminate the uncertainties due to quasistatic models in the design. Moreover, this tool can provide models for the arbitrary structures, e.g., the multiport junctions of the blocking MIM capacitors in the matching network, which is not available in the conventional circuit simulation tools. A design procedure using full-wave electromagnetic analysis for the passive structures was incorporated in this paper as well as many previous W-band monolithic designs. The design methodology has been described in detail elsewhere [14].



(a)



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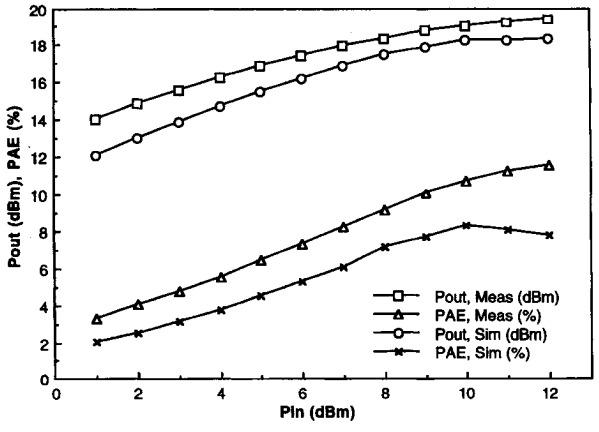
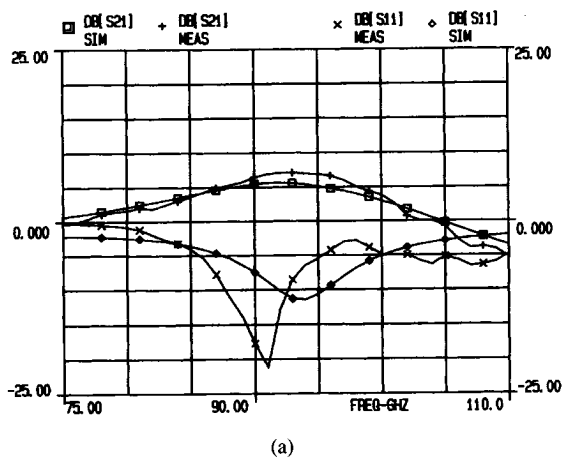


(c)

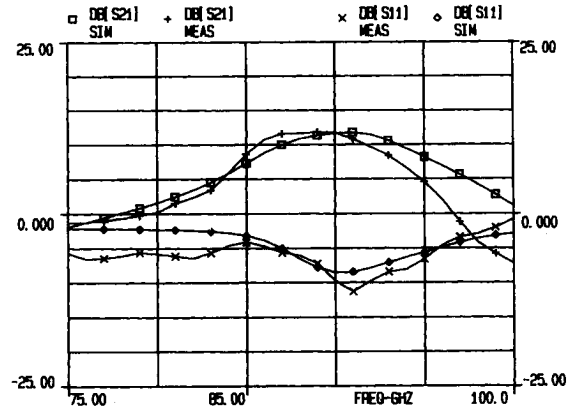
Fig. 7. The measured small signal gain and return losses as functions of frequency for (a) 21 sites of the single-stage push-pull PA, (b) 19 sites of the two-stage push-pull PA, and (c) the measured and simulated output power and PAE versus input power at 90 GHz for the two-stage push-pull PA.

IV. Measurement Results

The small signal gain of single-stage PA was tested with a verified on-wafer test set [15]. Fig. 7(a) shows the measured small signal gain and return losses from 75–110 GHz for 21 of 24 sites for the single-stage PA uniformly distributed across the 3-in wafer. A typical small signal gain of 7 dB is achieved from 92–96 GHz at a bias of $V_d = 4$ V with the gate voltage biased at peak dc transconductance (G_{mpk}) for both top and bottom cells, which results in 50-mA total drain current.



(a)



(b)

Fig. 8. The simulated small signal linear gain and input return loss (SIM) compared with measured data (MEAS) for the (a) single-stage and (b) two-stage push-pull PA.

The small signal gain of the two-stage PA was also tested with on-wafer probing. Fig. 7(b) presents the measured small signal gain and return losses from 75–100 GHz for 19 of 24 sites of the two-stage PA uniformly distributed across the 3-in wafer. A typical gain of 13 dB is achieved from 87–90 GHz for the same bias condition as the single-stage PA. The wafer was then diced and a PA chip with typical performance was selected to be measured in a WR-10 waveguide test-fixture for output power performance. The circuit demonstrates 19.4-dBm output power with 7.4-dB saturated gain at 90 GHz. The measured and simulated output power and PAE versus input power at 90 GHz and a 4-V drain bias on both stages are plotted in Fig. 6(c). The peak PAE is 11.7% at output power saturation with a 4-V bias. The best PAE of this push-pull PA is 13.3% and occurs at 3.5-V drain bias with an associated output power of 18.8 dBm and an input power of 11 dBm. Compared with the previously reported data [4], [5], this PA demonstrates better gain performance, similar output power, and higher PAE since it only uses half of the device periphery.

Fig. 8 presents the simulated circuit performance for linear small signal gain and input return loss compared with a typical measured data of the single-stage and two-stage push-pull PA. Reasonable agreement is observed between simulation results and measurement data. The measured passband shift to a lower

frequency of the two-stage PA is probably due to the more sensitivity of the matching topology as discussed earlier. In the nonlinear simulation for output power performance, the simulated results show 1.5–2 dB lower power than the measured data as plotted in Fig. 7(c). The main reason is suspected to be that the harmonic balanced technique requires several higher order harmonic signals in the circuit analysis. Those frequencies can be much higher than 200 GHz, at which frequency most of the models have questionable accuracy. This possible reason for the simulation discrepancy is still considered as one of major bottlenecks for W-band nonlinear MMIC design.

V. Summary

We have presented the first report of the MMW monolithic push-pull PA's developed using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic T-gate power HEMT technology. This novel design approach has been demonstrated to be effective in improving the PA performance at MMW frequencies. State-of-the-art performance of the monolithic W-band PA's has been achieved for the two-stage push-pull PA design with a small signal gain of 13 dB, an output power of 19.4 dBm with PAE of 11.7% at 4-V drain bias, and a peak PAE of 13.3% under 3.5-V drain bias with an associated output power of 18.8 dBm measured at 90 GHz.

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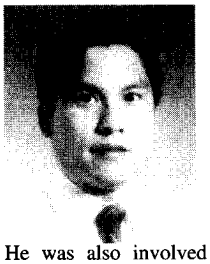

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For contributions to the application of GaAs MMIC in spacecraft payloads, Dr. Allen was awarded TRW's 1992 Chairman's Award for Innovation.