Low Voltage Circuit Design Techniques for Battery-Operated and/or Giga-Scale DRAM's

Tadato Yamagata, *Member, IEEE*, Shigeki Tomishima, Masaki Tsukude, Takahiro Tsuruda, Yasushi Hashizume, and Kazutami Arimoto

Abstract— **This paper describes a charge-transferred well (CTW) sensing method for high-speed array circuit operation and a level-controllable local power line (LCL) structure for high-speed/low-power operation of peripheral logic circuits, aimed at low voltage operating and/or giga-scale DRAM's. The CTW method achieves 19% faster sensing and the LCL structure realizes 42% faster peripheral logic operation than the conventional scheme, at 1.2 V in 16 Mb-level devices. The LCL structure realizes a subthreshold leakage current reduction of three or four orders of magnitude in sleep mode, compared with a conventional hierarchical power line structure. A negative-voltage word line technique that overcomes the refresh degradation resulting from reduced storage charge (Q_s) at low voltage operation for improved reliability is also discussed. An experimental 1.2 V 16 Mb DRAM with a RAS access time of 49 ns has been successfully developed using these technologies and a 0.4-μm CMOS process. The chip size is 7.9 $\times$ 16.7 mm^2 and cell size is 1.35 $\times$ 2.8 μm^2.**

I. Introduction

RECENTLY, low voltage operation has become an urgent requirement for DRAM's to save power consumption and to maintain high reliability. The power supply voltage level is moving from 5 V to 3.3 V to reduce the system power dissipation. For reliability reasons, low voltage operation is also needed to avoid electrical stress on thin oxide films and hot electron effects in transistors. For DRAM's in particular, the operating voltage must be decided considering on-chip voltage boosting for word lines. For example, in a 64 Mb DRAM with a thin gate oxide film of 10 nm and 0.3 $\sim$ 0.35-μm process, the supply voltage is internally converted to roughly 2.5 V using an on-chip voltage regulator. The operating voltage will be decreased to 2 $\sim$ 2.5 V for the 256 Mb generation, and to 1.5 $\sim$ 1.8 V for the 1 Gb generation.

On the other hand, as battery operated equipment, such as hand held computers and (personal digital assistant) PDA's, become widely used, the demand for low voltage/low power DRAM's will increase. Already employed in these applications are 3.3 V 4 Mb/16 Mb DRAM's. Battery operated applications will need even lower voltage DRAM's. Therefore, low voltage DRAM technology is a very important consideration for giga-scale DRAM's and battery operated applications. There have been some reports that discuss the potential of DRAM in the sub 2 V range [1]–[4]. However, higher performance and a wider operating margin are needed to broaden the application of low voltage DRAM's.

This paper is mainly concerned with descriptions of three low voltage DRAM circuit techniques. First, the charge-transferred well (CTW) sensing method for high-speed array circuit operation is introduced. Second, the level-controllable local power line (LCL) structure for high-speed/low-power operation of peripheral logic circuits is explained. Third, the negative-voltage word line technique is discussed to improve refresh characteristics and reliability in the low voltage range. Using these technologies and a 0.4-μm CMOS process, an experimental 1.2 V 16 Mb DRAM has been successfully developed and we obtained a RAS access time of 49 ns.

The CTW sensing method and LCL structure are explained in Sections II and III, respectively. The access time improvement due to the CTW sensing and the LCL structure is introduced in Section IV. The negative-voltage word line technique is discussed in Section V. Furthermore, a well-barrier structure that enhances soft error immunity is described in Section VI. Finally, the characteristics of the experimental 1.2 V 16 Mb DRAM are outlined [5].

II. Charge-Transferred Well (CTW) Sensing

A. Conventional Sensing

Fig. 1 shows a conventional sense circuit. In the stand-by period, the bit lines (BL, /BL) and sense drive lines (SN, SP) are precharged to the $V_{cc}/2$ level by an equalizing circuit. When the device enters active mode, the word line (WL) is activated and memory cell data is read out on bit lines. This initial readout data is usually 100 to 150 mV. After that, the SN is pulled down and the SP is pulled up in response to the activation of sensing signals S0F and /S0F, and a few nanoseconds later, S0 and /S0 is activated to accelerate the sensing. Assuming that the NMOS sense amplifiers are activated first, the sense operation starts when the difference between the BL level ("H" data side) and the SN level becomes larger than the V_{th} (threshold voltage) of the NMOS sense amplifier transistor. At this time, the V_{th} of the sense amplifier transistor is increased by a body effect because the back bias is effectively negative considering the SN and GND biased well (VW_p). The V_{th} increase causes a large sensing delay especially in low voltage operation. Therefore, in low voltage DRAM's, making the sense operation free from the body effect is a key issue.

Manuscript revised August 24, 1995.

The authors are with the ULSI Laboratory, Mitsubishi Electric Corporation, Hyogo, 664, Japan.

IEEE Log Number 9415344.

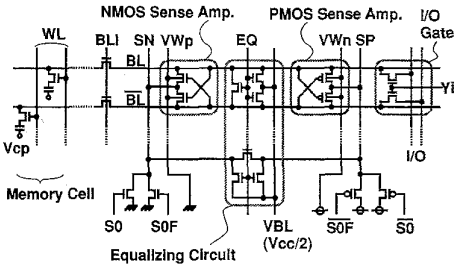
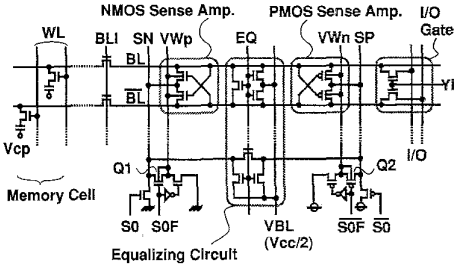
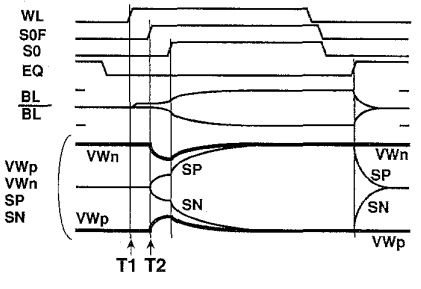


Fig. 1. Conventional sense circuit. This is the case that p-well under sense amp. is biased to GND.



(a)



(b)

Fig. 2. CTW sensing method. (a) Sense circuit diagram. (b) Operating timing sequence.

B. CTW Sensing

Fig. 2(a) shows a sense circuit for CTW sensing and Fig. 2(b) shows its operating timing sequence. In stand-by mode, the drive line (SN) of the NMOS sense amplifier and p-well (VW_p) are set to $V_{cc}/2$ and GND, respectively. After cell data is read out on bit lines (BL, /BL) at time T1, SN and VW_p are shunted via a transistor Q1 in response to the activation of the first sensing signal (S0F) at time T2, and the SN level drops. At the same time, the VW_p level rises and so the increase in V_{th} of the NMOS sense amplifier transistors due to the body effect is suppressed, and thus high-speed sensing can be carried out. The PMOS sense amplifier also behaves in the same manner.

As a means for low-voltage/high-speed sensing, the well-synchronized sensing method has been reported [6]. This method maintains the VW_p and VW_n levels so as to synchronize them with the SN and SP levels, respectively, and allows the sense operation to be free from the body effect. However, this method involves charging the well VW_p and VW_n from the power supply, and so the active current

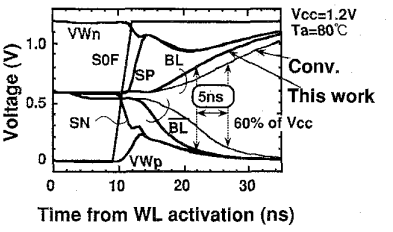


Fig. 3. Simulated waveforms of CTW sensing and conventional sensing. ($V_{thn} = 0.4$ V @ $V_{bb} = -0.5$ V, $V_{thp} = -0.5$ V, @ $V_{bb} = 0$ V).

increases by 4% compared with conventional sensing. On the other hand, CTW sensing is not accompanied by well-charging from the power supply, and results in no power loss. The well-synchronized sensing also has the drawback of small noise-immunity because of the forward-bias state between the bit line and the well before sense starting. With our new method, the well potential is always less than $V_{cc}/2$ level, and can avoid the above problem.

Fig. 3 shows the simulated waveforms of the CTW sensing method and conventional sensing at 1.2 V and 80°C. The simulation assumes memory cell capacitance of 35 fF and bit line capacitance of 180 fF. Furthermore, the V_{th} of the NMOS sense amplifier transistors is assumed to be 0.4 V at the back bias V_{bb} of -0.5 V, and the V_{th} of the PMOS sense amplifiers is assumed to be -0.5 V at the V_{bb} of 0 V. Conventional sensing assumes that the NMOS sense amplifiers have a back gate bias of -0.5 V. The sensing signal S0 is activated 3 ns after S0F activation. The sense operation in the new method is faster by 5 ns, that is 19% faster, than that of the conventional method at 1.2 V.

III. Level-Controllable Local Power Line (LCL) Structure

A. Conventional Hierarchical Power Line Structure

The use of low-V_{th} transistors can effectively achieve high-speed circuit operation in the low voltage range. However, the subthreshold leakage current in MOS transistors drastically increases and this is a very serious problem for low voltage DRAM's. To solve this problem, hierarchical power line structures have been proposed [7]–[9]. However, these structures still have problems. Fig. 4 shows a conventional hierarchical power line structure with inverters as logic circuits. The inverters consist of low-V_{th} transistors for high speed operation. The transistors that are cut-off during the stand-by period are connected to local power lines and the others are connected to main power lines. In stand-by mode, the subthreshold current is limited mainly by resistors R1 and R2, and the local V_{cc} level drops by ΔV_p and the local V_{ss} level rises by ΔV_n. The drop and rise stops at the level where the total subthreshold current ($\sum I_{leak}$) of the logic circuits equals the current (I_r) that flows through R1 and R2. Therefore, the values of ΔV_p and ΔV_n are decided by R1 and R2. The descent and ascent of the local power lines brings a circuit delay, as follows. As shown in Fig. 4, when the device enters active mode from stand-by mode, the local power lines need

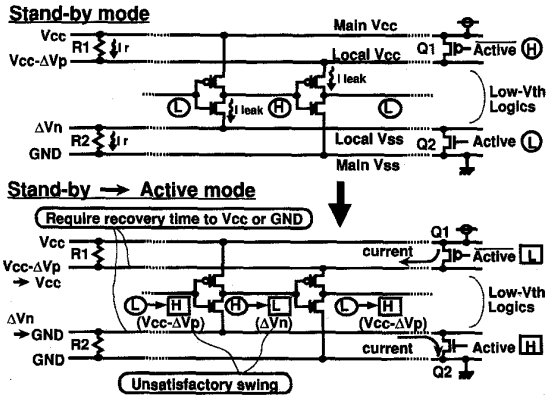


Fig. 4. Conventional hierarchical power line structure when entering active mode from stand-by mode.

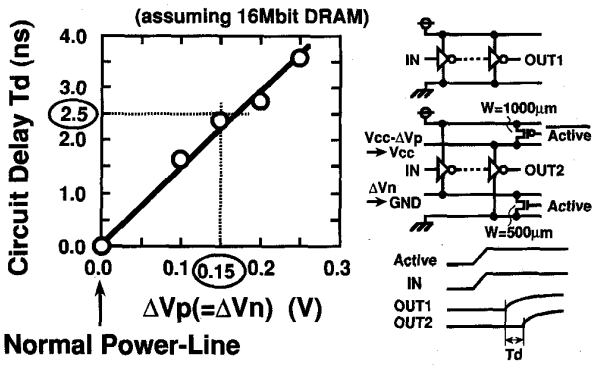


Fig. 5. Simulated circuit delay dependence on $\Delta V_p (= \Delta V_n)$ assuming 16 Mb DRAM with hierarchical powerline structure. (30-stage inverters with $L_n/W_n = 0.4\ \mu$m/10 μm, $L_p/W_p = 0.45\ \mu$m/20 μm, $FO = 5$ and local power line capacitance of 400 pF).

time to recover to V_{cc} or GND level as current flows through transistors Q1 and Q2. Also, the input level of each inverter is not satisfactory. The low level can be ΔV_n and the high level can be $V_{cc} - \Delta V_p$, as shown in Fig. 4. When ΔV_p and ΔV_n are large, drastic circuit delays or fatal errors can occur. Fig. 5 shows the simulated circuit delay dependence on ΔV_p (ΔV_n) in a conventional hierarchical power line structure, assuming a 16 Mb DRAM. For example, ΔV_p and ΔV_n must be designed so as to be less than 0.15 V to suppress the circuit delay to less than 2.5 ns. However, small ΔV_p and ΔV_n result in large subthreshold current.

A small R1 (R2) value results in a small ΔV_p (ΔV_n) and reduces active circuit delay. It also causes an increased stand-by current due to the large subthreshold current, especially in giga-scale DRAM's that have a large total channel width. On the other hand, a large R1 (R2) value results in a small stand-by current, but also a large access delay.

B. LCL Structure

We propose a new hierarchical power line structure that provides a very small subthreshold leakage current in a data retention (sleep) mode and achieves high speed operation in normal mode. Fig. 6 shows the proposed LCL structure

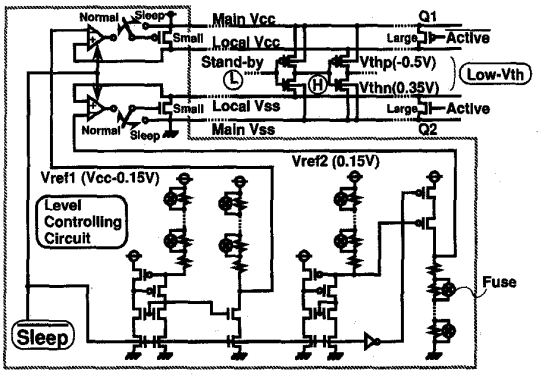


Fig. 6. LCL structure.

that controls the local power line levels in normal mode and in sleep mode. Low-V_{th} transistors, 0.35 V for NMOS and -0.5 V for PMOS, are used for high speed operation in this work. The new structure controls the local power line levels in normal mode by a level controlling circuit that consists of V_{ref1} and V_{ref2} generators and differential amplifiers. In stand-by mode, the local V_{cc} and V_{ss} are set to $V_{cc}-0.15$ V and 0.15 V respectively to suppress the recovery time to 2.5 ns, as previously described. In sleep mode, the level controlling circuit is separated from the hierarchical power lines and the subthreshold current in the logic circuits can be drastically reduced with large ΔV_p and ΔV_n. Though this control involves large ΔV_p and ΔV_n (the values are decided by the subthreshold current of transistors Q1 and Q2) and causes a long recovery time in self refresh operations, this is not problem because self refresh operations do not require high-speed. Furthermore, by cutting the power consumption of the level controlling circuit in sleep mode, lower power data retention is achieved. Moreover, the V_{ref1} and V_{ref2} generators are designed so as to be able to tune the voltage levels in normal mode by fuse-blowing after the wafer process, according to the V_{th} variation due to the process parameter fluctuations. This scheme was used because V_{th} variations become more serious with lower voltage and smaller geometry devices [10]. In our structure, the back-gates of the transistors that constitute the logic circuits are connected to the main power lines to avoid an increase of capacitance of the local power lines and to achieve high-speed recovery, as shown in Fig. 6.

Fig. 7 shows the trend of the subthreshold leakage current of a whole chip excluding the memory cell transistors, in which we assume an NMOS V_{th} of 0.35 V and a PMOS V_{th} of -0.5 V in the logic circuits, and a subthreshold swing S-factor of 100 mV/dec. The transistor Q1 in the LCL structure (See Fig. 6) has a V_{th} of -0.72 V and a 1000 μm channel width, while the V_{th} and channel width of Q2 are 0.57 V and 500 μm, respectively. The level controlling circuit is assumed to consume 0.5 μA in the LCL structure. When ΔV_p and ΔV_n are set to 0.15 V for high-speed operation, a conventional hierarchical power line can reduce the subthreshold current in stand-by mode to 3% of that of the normal power line structure. However, the subthreshold current reaches several μA in giga-

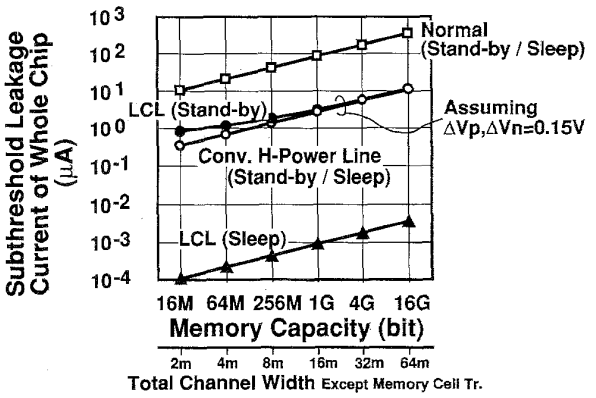
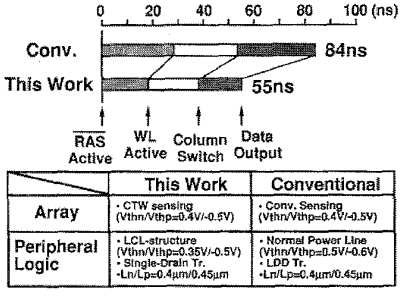


Fig. 7. Trend of subthreshold leakage current for normal power line, conventional hierarchical power line and LCL structure.



	This Work	Conventional
Array	• CTW sensing (Vthn/Vthp=0.4V/-0.5V)	• Conv. Sensing (Vthn/Vthp=0.4V/-0.5V)
Peripheral Logic	• LCL-structure (Vthn/Vthp=0.35V/-0.5V) • Single-Drain Tr. •Ln/Lp=0.4μm/0.45μm	• Normal Power Line (Vthn/Vthp=0.5V/-0.6V) • LDD Tr. •Ln/Lp=0.4μm/0.45μm

Fig. 8. Access time comparison between our work and conventional 16 Mb DRAM at 1.2 V and 80°C by simulation.

scale DRAM's, because of the increase of total channel width over the whole chip, which is still too large for sleep mode. By using the LCL structure, the subthreshold current can be reduced by three or four orders of magnitude in sleep mode, compared with the conventional hierarchical power line.

IV. Access Time Improvement Owing to CTW Sensing and LCL Structure

Next, we will describe the access time improvement attributed to CTW sensing and the LCL structure, assuming a 16 Mb DRAM. Fig. 8 indicates an access time comparison between this work and a conventional 16 Mb DRAM at 80°C by circuit simulation. Considering 1.2 V operation, low-$V_{\rm th}$ sense amplifiers ($V_{{\rm th}n} = 0.4$ V/$V_{{\rm th}p} = -0.5$ V) and low-$V_{\rm th}$ peripheral logic circuits ($V_{{\rm th}n} = 0.5$ V/$V_{{\rm th}p} = -0.6$ V) are assumed in the conventional device. In our work, for peripheral logic circuits in the LCL structure, $V_{{\rm th}n} = 0.35$ V/$V_{{\rm th}p} = -0.5$ V are assumed. Low-voltage operation allows single-drain transistors to be used without reliability degradation due to the hot-electron phenomenon. In this simulation, single-drain transistors are also used in peripheral logic circuits connected to the LCL structure. Furthermore, 0.4 μm channel length for NMOS and 0.45 μm for PMOS are assumed in the peripheral logic circuits.

In the array circuits, CTW sensing achieves 5 ns (19%) faster operation than conventional sensing at a $V_{\rm cc}$ of 1.2 V as described in Section II. In the peripheral circuits, 24 ns (42%) faster operation is obtained at a $V_{\rm cc}$ of 1.2 V by the low-$V_{\rm th}$, single-drain transistors in the LCL structure. As a result, the access time can be reduced from 84 ns to 55 ns at 1.2 V and 80°C, using CTW sensing and the LCL structure, which is 35% faster.

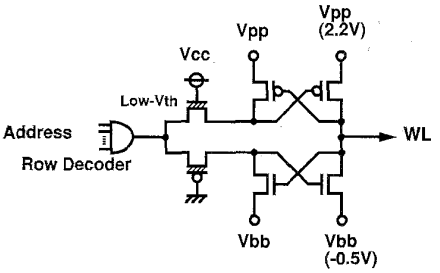


Fig. 9. Negative-voltage word line driver.

V. Negative-Voltage Word Line Technique

To improve the refresh time degradation resulting from reduced Q_s at low voltage operation, a shallow $V_{\rm bb}$ level (−0.5 V) was adopted in our device. Refresh characteristics are determined mainly by the junction leakage current under the storage node and the subthreshold leakage current of a memory cell transistor. The shallow $V_{\rm bb}$ level can reduce the electric field between the storage node and the p-well under the memory cell, resulting in a small junction leakage. However, the shallow $V_{\rm bb}$ level reduces the $V_{\rm th}$ of memory cell transistors and increases the subthreshold leakage current. As a method to suppress the subthreshold leakage current of memory cell transistors, the boosted sense-ground (BSG) scheme has been reported [11]. However, the BSG method is not suitable for low voltage operation, because the bit-line swing is less than $V_{\rm cc}$.

In this work, a negative-voltage word line (WL) technique was applied to suppress the increase in subthreshold leakage current due to the shallow $V_{\rm bb}$. Fig. 9 shows a circuit diagram of the negative-voltage WL driver in which the low level of the WL is set to −0.5 V using $V_{\rm bb}$. The combination of the shallow $V_{\rm bb}$ level of −0.5 V and the negative WL level of −0.5 V improves the refresh time by 2.5 ∼ 3 times, compared with the conventional WL control with a $V_{\rm bb}$ of −2 V. Therefore, these techniques achieve good refresh characteristics in spite of a reduced Q_s in low voltage operation.

Furthermore, since the negative-voltage WL technique allows the $V_{\rm th}$ of the memory cell transistors to be small, the WL's "H" level can be reduced to level lower than the conventional method. The required WL's "H" level is indicated in Fig. 10. In the negative-voltage WL method, 1.2 V cell restore can be readily achieved using a boosted voltage level ($V_{\rm pp}$) of $2V_{\rm cc}$, which can be easily generated by a conventional $V_{\rm pp}$ generator. Therefore, this method also facilitates the design of the $V_{\rm pp}$ generator and brings high reliability.

VI. Soft Error Immunity Enhancement

The Q_s reduction resulting from low voltage operation also increases α-particle induced soft errors. To overcome this

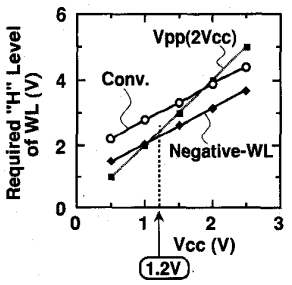


Fig. 10. Required WL's "H" level on negative-voltage WL and conventional method.

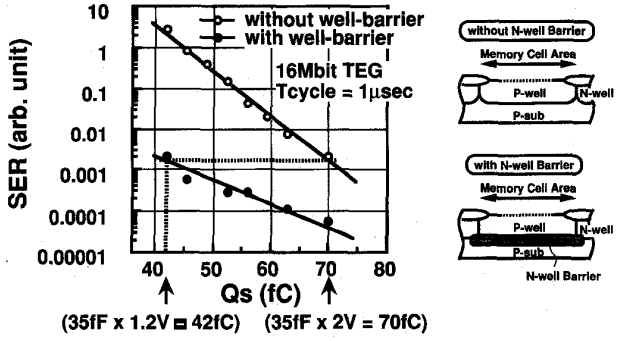


Fig. 11. Soft error comparison between with and without n-well barrier.

problem, an n-well barrier was provided under the memory cell area using a triple-well structure. Fig. 11 shows a soft error rate (SER) comparison between with an n-well barrier and without a well barrier, measured on a 16 Mb test chip. The n-well barrier reduces the SER by 2 $\sim$ 3 orders of magnitude and improves the SER at $V_{cc} = 1.2$ V to almost the same level as that of $V_{cc} = 2$ V without a barrier structure.

VII. Experimental 1.2 V 16 Mb DRAM

Using a 0.4-μm CMOS process (0.5 μm design rules with peripheral transistor channel lengths $L_n/L_p = 0.4$ μm/0.45 μm), an experimental 1.2 V 16 Mb DRAM has been successfully developed. In this device, single-drain transistors are used in peripheral logic circuits and connected to hierarchical power lines for high speed circuit operation. A triple-well structure is employed to realize CTW sensing and to create an n-well barrier against soft-error. For the sense control circuits of CTW sensing, the transistors controlled by S0 or /S0 are placed adjacent to bit-line pairs, and the transistors controlled by S0F or /S0F are placed at the intersection of the sense amplifier area and the WL shunting area. The chip area overhead of the CTW sensing with triple-well structure is 4.4%.

Fig. 12 is a chip photo micrograph and the chip size is 7.9 $\times$ 16.7 mm^2. Stacked capacitor cells are adopted and the cell size is 1.35 $\times$ 2.8 μm^2. Fig. 13 shows the output waveform. The RAS access time of 49 ns was obtained at 1.2 V under typical conditions. The main features of the experimental 16 Mb DRAM are summarized in Table I.

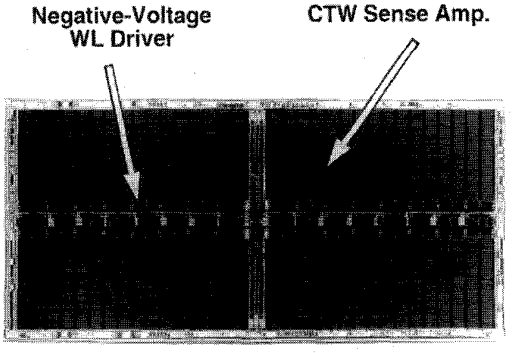


Fig. 12. Chip photo micrograph of experimental 16 Mb DRAM. Chip size is 7.9 mm $\times$ 16.7 mm.

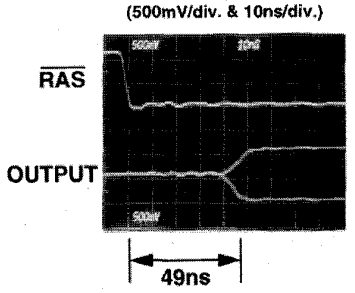


Fig. 13. Output waveform of experimental 16 Mb DRAM at V_{cc} to 1.2 V.

TABLE I
Main Features of Experimental 16 Mb DRAM

Process	**0.4μm Triple-Well CMOS 4-poly/2-Al Single-Drain Tr. (Peri. Logic)**
Memory Cell	**1.35 x 2.8 μm^2 (Stacked Capacitor)**
Chip Size	**7.9 x 16.7 mm^2**
Access Time (tRAC)	**49ns @1.2V, Typ. Condition**
Active Current	**13mA @1.2V, Tcycle=110ns**
Stand-by Current	**5μA @1.2V**

VIII. Conclusion

We have described three circuit technologies for low voltage DRAM's. The CTW sensing is 19% faster than conventional method at 1.2 V and 80°C, because of the suppression of the body effect. The LCL structure achieves 42% faster operation using low-V_{th} and single-drain transistor logic. Furthermore, the LCL structure also realizes a drastic subthreshold leakage current reduction by 3 $\sim$ 4 orders of magnitude in sleep mode, compared with a conventional hierarchical power line structure. The negative-voltage word line technique reduces the subthreshold leakage current of memory cell transistors and contributes to refresh time extension and high reliability. Furthermore, the n-well barrier improves the SER by 2 $\sim$ 3 orders of magnitude using a triple well structure.

Using these technologies and a 0.4 μm CMOS process, an experimental 1.2 V 16 Mb DRAM has been successfully developed. The chip size is 7.9 $\times$ 16.7 mm^2 and a RAS access

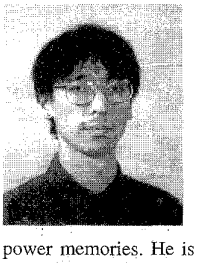
time of 49 ns was obtained. The circuit technologies described above are very useful for implementing low voltage DRAM's for battery operated equipment and low voltage giga-scale DRAM's.

ACKNOWLEDGMENT

The authors wish to thank H. Komiya, T. Yoshihara, M. Yamada, and T. Nishimura for their support and encouragement. They would also like to thank Y. Ohno and T. Eimori for the device fabrication.

REFERENCES

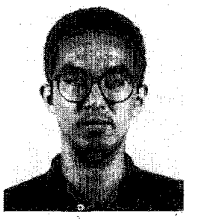
[1] M. Aoki *et al.*, "A 1.5-V DRAM for battery-based applications," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1206–1212, Oct. 1989.
[2] Y. Nakagome *et al.*, "An experimental 1.5-V 64-Mb DRAM," *IEEE J. Solid-State Circuits*, vol. 26, pp. 465–472, Apr. 1991.
[3] H. Yamauchi *et al.*, "A circuit technology for high-speed battery-operated 16-Mb CMOS DRAM's," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1084–1091, Nov. 1993.
[4] D.-C. Choi *et al.*, "Battery operated 16 M DRAM with post package programmable and variable self refresh," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1994, pp. 83–84.
[5] T. Yamagata *et al.*, "Circuit design techniques for low voltage operating and/or giga-scale DRAM's," in *ISSCC Dig. Tech. Papers*, Feb. 1995, pp. 248–249.
[6] T. Ooishi *et al.*, "A well-synchronized sensing/equalizing method for sub-1.0 V operating advanced DRAM's," in *Symp. VLSI Circuits Dig. Tech. Papers*, May 1993, pp. 81–82.
[7] M. Horiguchi *et al.*, "Switched-source-impedance CMOS circuit for low standby subthreshold current giga-scale LSI's," in *Symp. VLSI Circuits Dig. Tech. Papers*, May 1993, pp. 47–48.
[8] D. Takashima *et al.*, "Stand-by/active mode logic for sub-1 V 1 G/4 Gb DRAM's," in *Symp. VLSI Circuits Dig. Tech. Papers*, May 1993, pp. 83–84.
[9] S. Mutoh *et al.*, "1 V high-speed digital circuit technology with 0.5 μm multithreshold CMOS," in *Proc. IEEE ASIC Conf.*, 1993, pp. 186–189.
[10] S. Kohyama, "Semiconductor technology crisis and challenges toward the year 2000," in *Symp. VLSI Technol. Dig. Tech. Papers*, May 1994, pp. 5–8.
[11] M. Asakura *et al.*, "A 34 ns 256 Mb DRAM with boosted sense-ground scheme," in *ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 140–141.



Tadato Yamagata (M'93) was born November 27, 1957, in Osaka, Japan. He received the B.S. and M.S. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1981 and 1983, respectively.

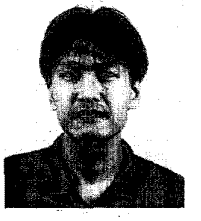
He joined the LSI Research and Development Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo, Japan, in April 1983. Since then he has been engaged in the design of MOS dynamic RAM's, content addressable memories, and MOS static RAM's. His current interest is low-voltage/low-power memories. He is currently with the ULSI Laboratory.

Mr. Yamagata is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



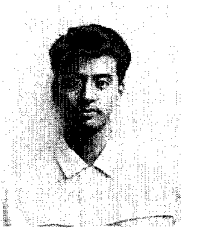
Shigeki Tomishima was born June 3, 1964, in Hyogo, Japan. He received the B.S. and M.S. degrees in solid state physics from Osaka University, Osaka, Japan, in 1988 and 1990, respectively.

In 1990, he joined the ULSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan. Since then he has been engaged in the research and development of ULSI dynamic RAM's. He is currently involved in the development of dynamic RAM at the low voltage condition.



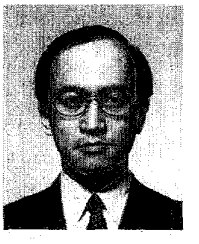
Masaki Tsukude was born December 29, 1961, in Hiroshima, Japan. He received the B.S. and M.S. degrees in electronic engineering from Hiroshima University, Hiroshima, Japan, in 1985 and 1987, respectively.

He joined the ULSI Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo, Japan, in 1987. Since then he has been engaged in the design of ULSI MOS dynamic RAM's.



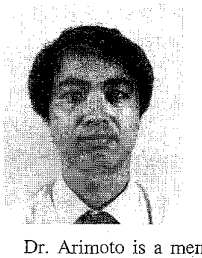
Takahiro Tsuruda was born August 6, 1968, in Fukuoka, Japan. He received the B.S. degree in electronic engineering from Okayama University, Okayama, Japan, in 1991.

He joined Mitsubishi Electric Corporation, Itami, Japan, in 1991. Since then he has engaged in the research and development of ULSI MOS dynamic RAM's at the LSI Laboratory and the ULSI Laboratory.



Yasushi Hashizume was born July 19, 1962, in Tokyo. He received the B.S. degree in electrical engineering from Osaka University, Osaka, Japan, in 1986.

He joined the Kita-Itami works, Mitsubishi Electric Corporation, Hyogo, Japan, in 1986, where he worked on the LPCVD process. In 1990, he transferred to the LSI R&D Laboratory, Mitsubishi Electric Corporation, Hyogo, Japan. He is currently working on the development of the device technology of MOS dynamic memories.



Kazutami Arimoto was born in Wakayama, Japan, in 1957. He received the B.S., M.S., and Dr. degrees in electric engineering from Osaka University, Osaka, Japan, in 1979, 1981, and 1993, respectively.

He joined the ULSI Laboratory, Mitsubishi Electric Corporation, Itami, Hyogo, Japan, in 1981. Since then he has been engaged in the design and development of MOS dynamic RAM's. He is currently interested in multimedia systems, fault tolerant systems, and memory design oriented CAD systems.

Dr. Arimoto is a member of the Institute of Electronics, Information and Communication Engineering of Japan.