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Low-Noise, High-Speed Data Transmission Using a Ringing-Canceling Output Buffer

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Abstract—**The proposed ringing-canceling output buffer transmits a superimposed two-step pulse that almost completely cancels the ringing in the received waveform. Simulation showed that this circuit increases the noise margin by a factor of 2.6 compared to using a conventional circuit in a bus interface at a data rate of 200 MHz. A test circuit was designed and fabricated to experimentally verify the fundamental ringing-canceling effect. Compared with other approaches to reducing ringing, the ringing-canceling output buffer provides a bigger improvement in the noise margin with a smaller signal-delay. This output buffer is promising for improving the data transfer rate of the memory bus.**

I. Introduction

THE clock frequencies of microprocessors and the data rates of synchronous DRAM's now exceed 100 MHz [1] [2]. While there has been a drastic increase in the on-chip circuit operation speed, the off-chip data transfer rate has become a bottleneck because it is difficult to increase the off-chip data transfer rate above 100 MHz, especially in the bus transmission.

DRAM's are mainly used in the bus interconnection system on a printed circuit board to form the main memory. In this system, the I/O pins of many DRAM's are connected to a bus line. Therefore, signal reflections occur at the stubs of the bus or at the parasitic elements of DRAM packages when the frequency of the signal increases, which cause the wavelength of the high-frequency component in the data waveform to approach the bus length. Consequently, ringing appears in the transmitted and received waveform, degrading signal integrity.

The reduced-swing interfaces proposed to achieve high-speed data transfer [3] have a termination resistor at the ends of the transmission line to suppress the signal reflection that occurs there. However, multiple reflections at the stubs and the parasitic elements still occur, so the ringing is not reduced.

Another approach is to use special packages and a transmission line environment for the DRAM [4]. By gathering the pins on one side of the chip to reduce the parasitic capacitance and by limiting the bus length, a high data-transmission rate can be achieved. However, the reduced pin count requires that the address and data be multiplexed, which leads to increased latency. Therefore, it is more preferable to improve the integrity of the signal and to increase the data transmission rate without latency penalty.

This paper proposes and evaluates a new output buffer circuit, a ringing-canceling output buffer (RC buffer), which is introduced for an experimental 1-Gb DRAM [5]. The problems of using a high-speed bus interface are described in Section II. The concept and performance of the RC buffer are described in Section III. Finally, the effectiveness of this buffer and other methods in reducing signal ringing is compared in Section IV.

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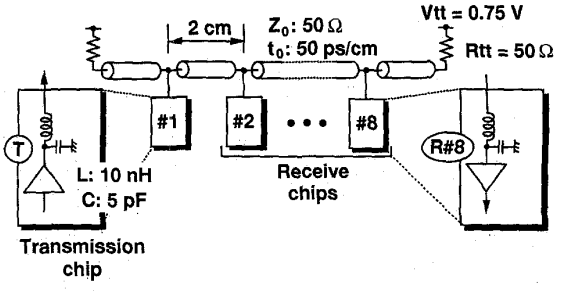


Fig. 1. Model of bus transmission.

II. Signal Integrity on Memory Bus Line

To estimate the response of a bus system to a transmitted signal, we calculated the ac transfer characteristics of the bus by using the bus model in Fig. 1. Eight chips are connected to a transmission line at 2-cm intervals; the line has the characteristic impedance z_0 of 50 Ω and delay t_0 of 50 ps/cm. The line is terminated to a voltage V_{tt} of 0.75 V through termination resistors R_{tt} of 50 Ω at both ends. At the I/O nodes of each chip, a parasitic inductance of 10 nH and a parasitic capacitance of 5 pF are inserted, which are typical values for a conventional DRAM package.

The interface levels are assumed to be the terminated CMOS levels. Power supply voltage V_{dd} is 1.5 V, and the reference voltage and the termination voltage V_{tt} are assumed to be $V_{dd}/2$ (= 0.75 V). A reduced signal amplitude is assumed. The high level is V_{tt}+ 0.4 V (= 1.15 V), and the low level is V_{tt}− 0.4 V (= 0.35 V). To obtain this amplitude for a 25 Ω load, the output impedance of the output buffer is set to 22 Ω.

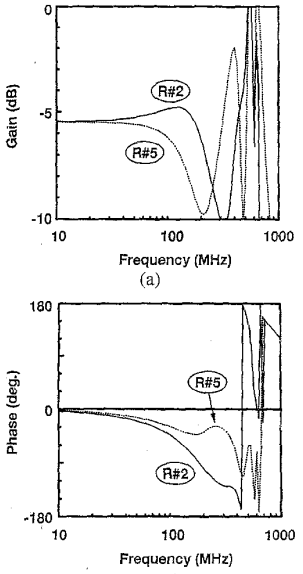


Fig. 2. AC transfer characteristics of the bus. (a) gain. (b) phase.

The calculated ac transfer characteristics from chip #1 to chips #2 and #5 are shown in Fig. 2. Since the signal amplitude is reduced by the output impedance and termination resistance, the gain at lower frequencies is already less than 0 dB. The cut-off frequency of the bus is around 200 MHz. Moreover, gain peaks are observed at 400–600 MHz, caused by resonance on the bus.

Ringing appears in the received waveform if the transmitted waveform contains high-frequency components corresponding to these gain peaks. Undershoots of the waveform caused by ringing at a transition edge from a low to a high level reduce the noise margin of the high-level state. In the same way, overshoots at a transition edge from a high to a low level reduce the noise margin of the low-level state.

The simulated noise margins of the received waveform using the bus model in Fig. 1 are shown in Fig. 3 as a function of data transmission rate f. A step pulse was transmitted from chip #1 by using a voltage source. The rise time of transmitted waveform t_r was assumed to be $1/(10f)$. The noise margin was defined as the ratio of V_m to V_s, as shown in the inset of Fig. 3, where V_m is the difference between the minimum point of the received waveform and the reference voltage, and V_s is the dc signal amplitude (0.4 V). The noise margin drastically decreases as f exceeds 30–40 MHz; it is less than 50% at 100 MHz. It is thus difficult to achieve the data transmission rates above 100 MHz without suppressing the ringing and improving the noise margin.

III. Ringing-Canceling Output Buffer

This section describes a ringing-canceling technique to solve problems pointed out in the previous section. The concept of ringing-canceling technique is first described. The circuit that realizes this concept is shown next. The ringing-canceling effect is verified by simulated and experimental results.

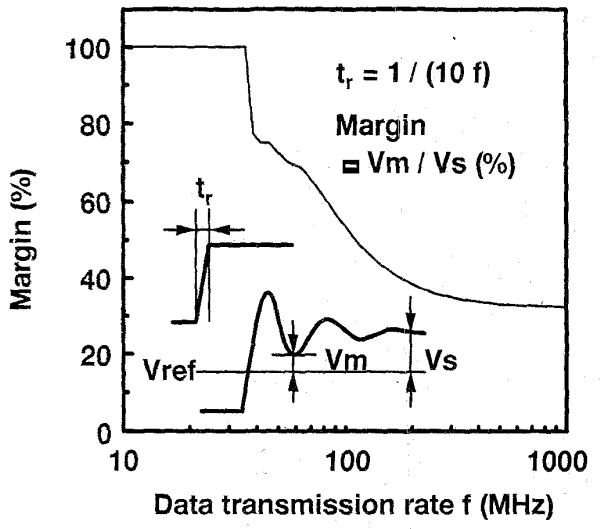


Fig. 3. Noise margin as a function of data transmission rate.

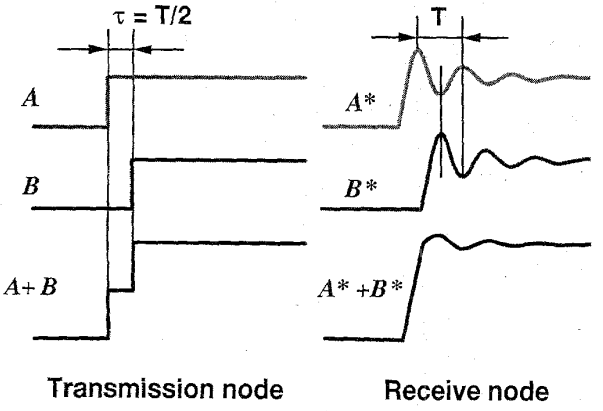


Fig. 4. Concept of ringing cancellation.

A. Concept of Ringing-Cancellation

The proposed ringing-canceling technique is based on the principle of superposition as shown in Fig. 4. When step pulse A is transmitted from a transmission chip on the bus, multiple reflections occur on the bus, and ringing appears in received waveform A^* at the receive chip. The period of this ringing is defined as T. When step pulse B delayed by $T/2$ from A is transmitted, received waveform B^* contains ringing delayed by $T/2$ from that of A^*. The proposed RC buffer transmits a two-step pulse $(A + B)$, the superposition of A and B; the received waveform thus becomes $A^* + B^*$, in which the overshoots and undershoots of the two ringings almost completely cancel each other out.

B. Circuit and Operation

An output buffer circuit to realize the principle is shown in Fig. 5. The size of output stage MOS transistors M_P and M_N in the RC buffer is the same as that in the conventional buffer. This size is sufficient for achieving an output impedance of 22 Ω, which is needed to obtain a suitable signal amplitude in

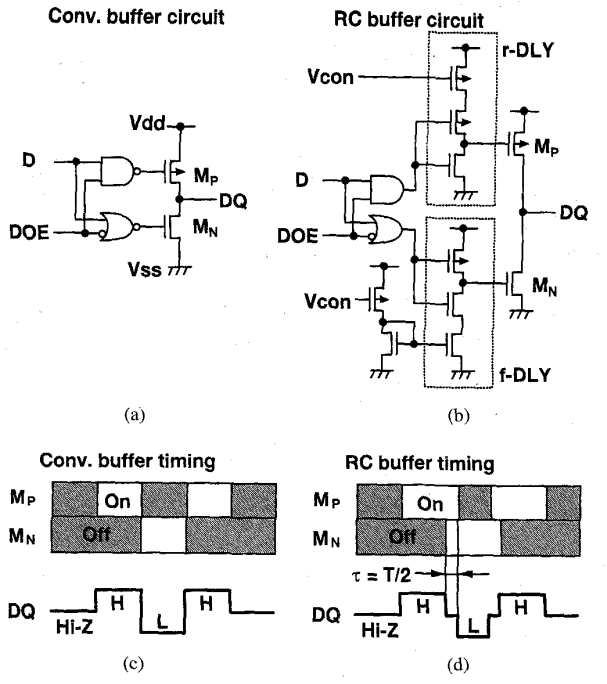


Fig. 5. Circuit and timing diagrams. (a) and (c) conventional buffer. (b) and (d) RC buffer.

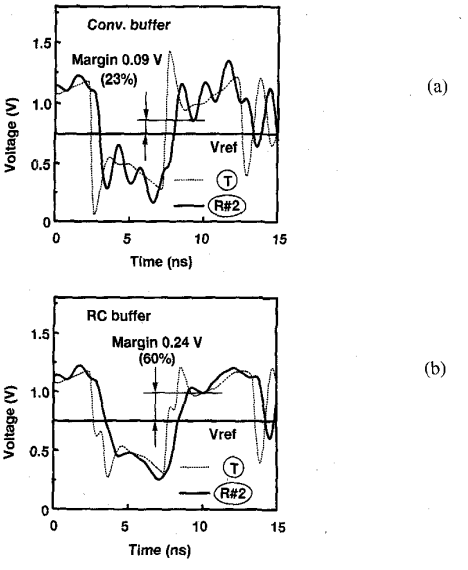


Fig. 6. Transmitted and received waveforms. (a) conventional. (b) ringing-canceling buffer.

the bus shown in Fig. 1. Delay circuit r-DLY is inserted into M_P gate, and another delay circuit, f-DLY, is inserted into the M_N gate; r-DLY delays the rise-edge of the signal for τ, and f-DLY delays the fall-edge of the signal for τ.

As shown by the timing charts in Fig. 5(d), when a output node DQ in the RC buffer transits from a high-level state (H) to a low-level state (L), the cut-off of M_P is delayed; M_P and M_N then conduct at the same time during τ. DQ is thus the intermediate level determined by the ratio of M_P and M_N and a two-step pulse is transmitted. In the same way, when node DQ transits from a low-level state to a high-level state, the cut-off of M_N is delayed, and a two-step pulse is transmitted. During τ, the direct current from V_{dd} to V_{ss} flows through M_P and M_N. However, the power consumption is dominated by the dc current through terminated resistors in the terminated bus system. Therefore, the RC buffer causes no remarkable increase of the power consumption.

In the RC buffer, the two-step-interval of $A + B$ plays an important role; it is defined as τ in Fig. 4. Generally, ringing period T varies due to the configuration of the bus; it is affected by the length of the bus interconnection line, the number of chips connected to the bus, the parasitic inductance and capacitance of the signal pins, etc. Therefore, we can adjust τ to be equal to $T/2$, the optimal value for canceling the ringing. The τ is adjusted by changing the delay of r-DLY and f-DLY by changing dc voltage V_{con}.

C. Simulated Characteristics

To evaluate the proposed RC buffer, we simulated the transmitted and received waveforms using the bus model shown in the Fig. 1. A 200-MHz data signal was transmitted from chip #1 using the buffers shown in Fig. 5 and received at chips #2–8. The waveforms at chip #2, which has the smallest noise margin, are shown in Fig. 6.

With the conventional buffer, a ringing appears in the received waveform. The noise margin is only 0.09 V (23% of the dc signal amplitude, 0.4 V) at the first undershoot. On the other hand, with the RC buffer, the ringing in the received waveform is suppressed; the noise margin increases to 0.24 V (60%).

To investigate the adjustment tolerance of τ in the RC buffer, we calculated the dependence of noise margin on τ by using the bus model shown in Fig. 1. A two-step pulse was transmitted from chip #1 by using a voltage source, varying two-step-interval τ. The rise time of each step was 0.1 ns. The noise margin of the received waveform at chip #2 is shown in Fig. 7. The point where $\tau = 0$ corresponds to using a conventional buffer; in this case, the period of ringing T equals 1.6 ns. Increasing τ suppresses the ringing of the received waveform, increasing the noise margin. At $\tau = T/2 = 0.8$ ns, the ringing-canceling effect is maximized, and the noise margin is maximized. The change in the noise margin is slow at around $\tau = T/2$, so the noise margin can easily be adjusted to be close to the maximum value. Increasing τ further, gradually decreases the noise margin.

The received waveforms may vary between chips because the positions of the chips connected to the bus are different. To investigate the effect of this variation on the ringing-canceling effect, we transmitted data at 200 MHz from chip #1 on the bus shown in Fig. 1. The ringing periods T and the noise margins at chips #2–8 are shown in Fig. 8. With the conventional buffer, T ranges 1.6–2.0 ns, so the distribution is not wide. The noise margin is the smallest at chip #2, (23% and $T =$ 1.6 ns). Using the RC buffer with τ set to 0.8 ns to maximize the ringing-canceling effect at chip #2, the noise margin at chip #2 increased to 60%. Moreover, the noise margins at the other chips also increased.

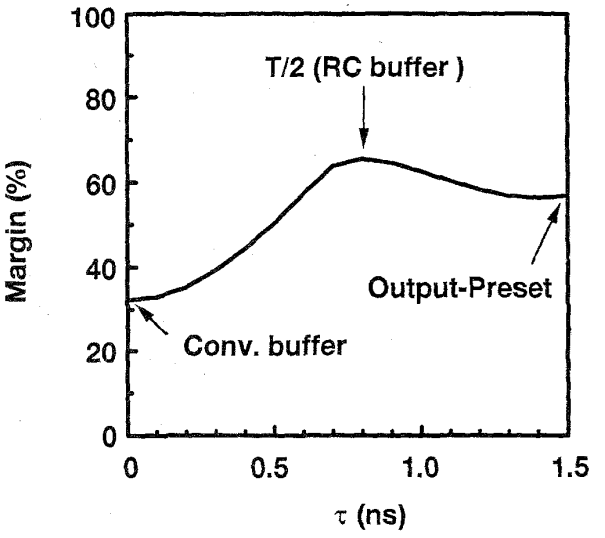


Fig. 7. Dependence of noise margin on two-step-interval τ.

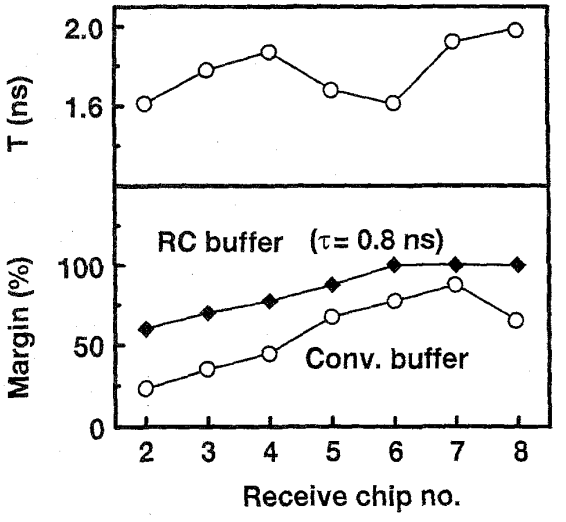


Fig. 8. Distribution of margin and ringing period T on bus.

Preferably, τ should be adjusted to the optimal value for the chip receiving the signal. This is feasible when only one fixed chip in the bus is receiving data, such as output data transmission from one of memory chips to a processor chip; this is impossible when more than one chip in the bus is receiving data at the same time, such as address transmission from a processor chip to memory chips. However, Fig. 8 shows that it is sufficient to adjust τ to the $T/2$ of the chip with the smallest noise margin in this case.

D. Experimental Results

To confirm the effectiveness of the RC buffer experimentally, we fabricated the test circuits shown in Fig. 9. This test circuit chip was assembled in a dual-in-line package. A 10-cm coaxial cable was connected to the output pin; a capacitor of 10-pF was connected to the other end of the cable. Both ends

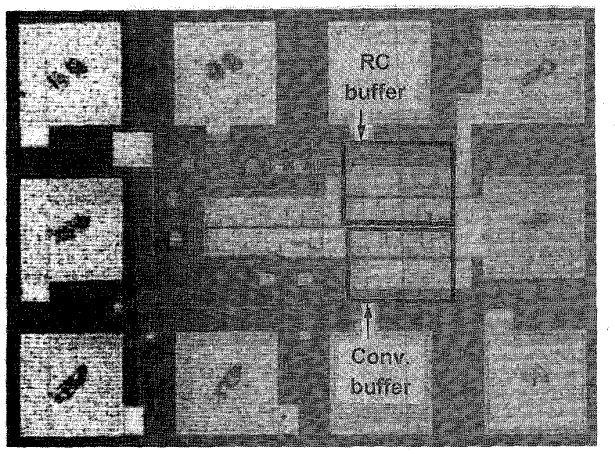
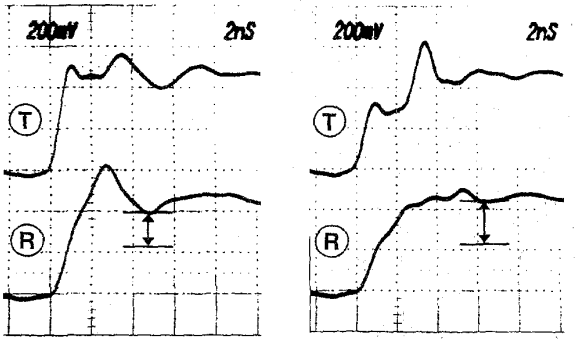


Fig. 9. Photomicrograph of test circuits.



(a) (b)

Fig. 10. Measured waveforms of test circuits. (a) conventional buffer. (b) RC buffer ((T) = transmitted waveform, (R) = received waveform).

of the transmission line were terminated by 50-Ω resistors. Pulses of 50 MHz are transmitted using conventional buffer and RC buffer.

The measured transmitted and received waveforms are shown in Fig. 10. Because the experiment was done in the point-to-point system, the noise margin of received waveform is not so small even using a conventional buffer. However, it is improved slightly using the proposed RC buffer. Fundamental ringing-canceling effect of the proposed RC buffer was verified. In the bus system, the noise margin will be improved as shown in simulation results.

IV. Discussion

Other approaches to reducing ringing in the received waveform include the two-phase drive technique [6]; the output-preset technique, in which an output node is preset to the intermediate level prior to data transmission [7]; and the relaxed-switching-rate technique, in which the rise time and fall time of the transmitted waveform is increased [8]. However, none of these provides sufficient effect because of the following reason.

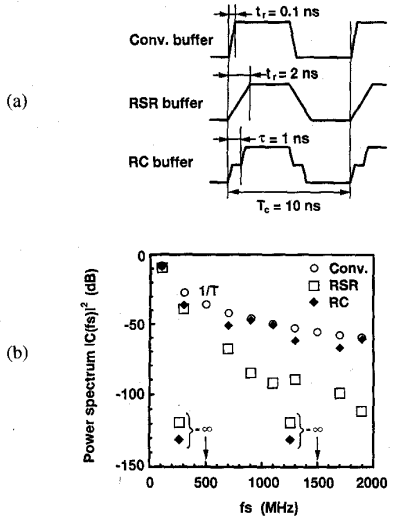


Fig. 11. Comparison of (a) transmitted waveforms. (b) power spectrums $|C(fs)|^2$ ($fs = n \times 100$ MHz).

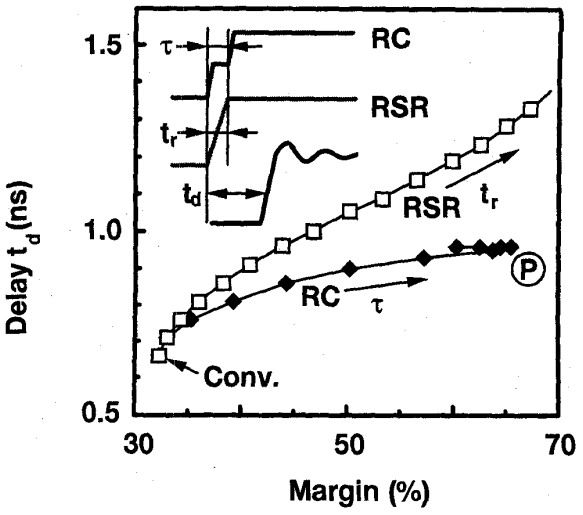


Fig. 12. Comparison of delay with ringing-canceling buffer and relaxed-switching-rate buffer.

In the two-phase drive technique, an output buffer consists of two pull-up transistors and two pull-down transistors placed in parallel. When an output node transits from a low-level state to a high-level state, a delay is introduced between drives of two pull-up transistors. When a output node transits from a high-level state to a low-level state, a delay is introduced between drives of two pull-down transistors. Therefore, a two-step pulse is transmitted. However, in this technique, two-step-interval τ is fixed for each chip—it is not adjusted to $T/2$ when ringing period T changes. Therefore, the noise margin will vary, as shown in Fig. 7, depending on the bus conditions.

In the output-preset technique, the two steps have no correlation at the received node, and the noise margin is only determined by the second step, which starts from an intermediate level. As shown in Fig. 7, as τ is increased, the noise margin approaches a constant value asymptotically. This limit corresponds to the noise margin in this technique.

In the relaxed-switching-rate (RSR) technique, the output buffer transmits a waveform with an increased transition time. This reduces the waveform's high-frequency components, which correspond to the gain peaks of the frequency response in the bus (Fig. 2). However, reducing the high-frequency components means increasing the signal delay on the other hands.

In contrast, the RC buffer reduces the high-frequency components of the bus gain peaks without affecting the other high-frequency components. To clarify this, we calculated the Fourier spectrums of the three waveforms shown in Fig. 11(a).

The nth component of the Fourier spectrum of one-step pulse-wave $C_1(n)$ is

$$C_1(n) = \frac{2T_c}{(n\pi)^2 t_r} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi t_r}{T_c}\right) \quad (1)$$

where T_c is cycle time, and t_r is the signal transition time of the positive and negative edge.

The Fourier spectrum of two-step pulse-wave $C_2(n)$ is

$$C_2(n) = \frac{2T_c}{(n\pi)^2 t_r} \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi t_r}{T_c}\right) \cos\left(\frac{n\pi\tau}{T_c}\right) \quad (2)$$

where τ is the two-step-interval.

The power spectrums of the three waveforms calculated using these equations are shown in Fig. 11(b). The assumptions are as follows: the T_c of these waveforms is 10 ns, and the fundamental frequency of $n = 1$ is 100 MHz; the t_r of the conventional buffer and the RC buffer is 0.1 ns and that of the RSR buffer is 2 ns; the τ of the RC buffer is 1 ns, assuming a ringing frequency of 500 MHz. The power spectrums at 500 MHz and 1500 MHz (Fig. 11) are reduced in the waveforms for both the RC buffer and the RSR buffer compared with that of the conventional buffer. At above 500 MHz, the spectrum of the RSR buffer is smaller than that of the conventional buffer. This leads to a large signal delay. However, the spectrum of the RC buffer is almost as large as that of the conventional buffer at above 500 MHz. This leads to a small signal delay.

We calculated the signal delay and noise margin for these buffers by using a bus model shown in Fig. 1. The t_r was varied for the RSR buffer; the τ was varied for the RC buffer. The waveforms were transmitted from chip #1 by using a voltage source. The relation between the noise margin and the delay t_d of the received waveform at chip #2 is shown in Fig. 12, with t_r and τ as parameters. In the RSR buffer, when t_r is increased, the noise margin and delay increases. In the RC buffer, when τ is increased, the noise margin and delay also increase; the noise margin is maximized at $\tau = T/2$. However, when compared at the same noise margin, the RC buffer delay is smaller than that of the RSR buffer. At the maximum noise margin of the RC buffer (point (P) in Fig. 12), the delay difference is 0.3 ns. Thus, a wider signal strobe window for a certain cycle time is obtained with the RC buffer.

On these delay curves, markers are placed with increase of 0.1 ns of τ and t_r. To set the noise margin around the point

(P) in RC buffer, the adjustment accuracy of τ should be less than ± 0.2 ns. On the other hand, RSR buffer also needs adjustment of t_r to optimize the relation of the delay and the noise margin. The sensitivity of the delay on the t_r of the RSR buffer is larger than that on the τ of the RC buffer. Therefore, the adjustment of the RC buffer is easier than that of the RSR buffer.

V. Conclusion

The ringing-canceling output buffer we propose for low-noise and high-speed data transfer transmits a superimposed two-step pulse that cancels most of the ringing in the received waveform. Simulation results showed that this circuit increases the noise margin in the bus by a factor of 2.6 compared with the conventional circuit at a data rate of 200 MHz. The noise margin is improved even when there is variation in the waveform received by the different chips in the bus. We experimentally verified the fundamental ringing-canceling effect by designing and fabricating a test circuit. The analysis of the Fourier spectrum shows that compared to a reduced-switching-rate output buffer, the ringing-canceling output buffer has a smaller signal delay at the same level of noise margin improvement.

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