An Auto-Ranging Photodiode Preamplifier with 114 dB Dynamic Range

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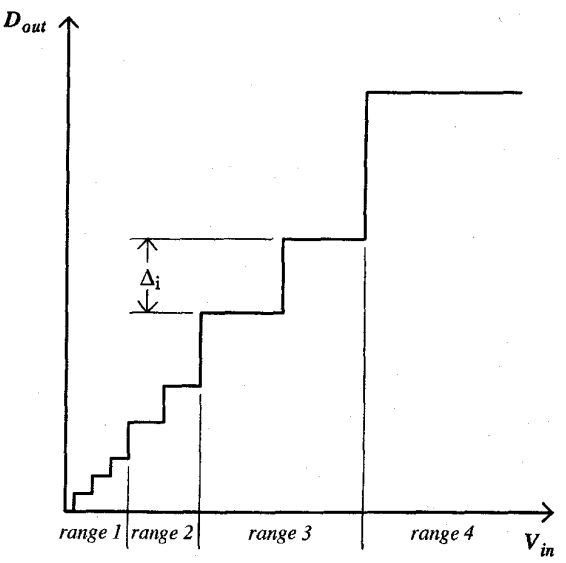
***Abstract*—A low noise photodiode preamplifier integrated circuit with auto-ranging gain capability has been designed, fabricated, and tested. When connected to a 25 pF input capacitance, the four-channel device has an input referred noise below 0.5 fC, which is just 3 dB above the minimum *kTC* noise. The preamp chip is designed to handle a full-scale charge input of 210 pC and has a 114 dB dynamic range. The device achieves a linearity specification of 0.01% of input reading ±0.25 ppm of full scale with a sample period of 1ms. The chip consumes 135 mW and is 5.8 mm × 7.4 mm in size.**

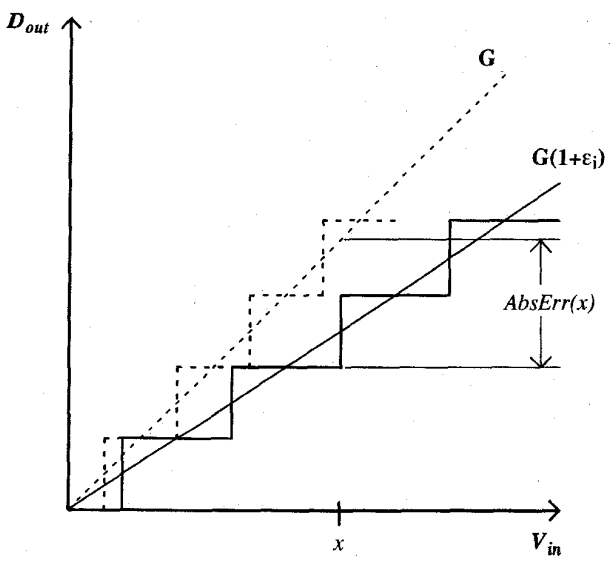
I. Introduction

In many applications, the charge input from a photodiode sensor must be digitized to a high resolution, for example, in x-ray imaging devices. The most common approach is to convert the charge to a voltage using a switched-capacitor integrating preamplifier and then to digitize the signal using a voltage-input analog-to-digital converter (ADC). The addition of an auto-ranging programmable gain amplifier to the preamplifier front-end is useful for obtaining increased dynamic range. A resulting trade-off is that larger quantization steps are provided for larger signals than for small ones. However, this behavior is acceptable in certain applications. Any situation in which an input signal's noise increases with signal level can benefit from autoranging.

X-ray sensor signals, for example, have quantum noise limited characteristics whereby their noise varies in proportion to the square-root of the signal level. Because of this, large x-ray signals can be digitized with larger quantization step-sizes without appreciably increasing the total noise. Previous work has put variable gain in the switched-capacitor integrator by selecting different feedback capacitance values [1], [2]. However, the strength of the signal must be known *a priori* as the gain can not be changed while the signal is being acquired. Holloway [3] has described a charge-to-digital converter which uses a fixed gain preamp followed by an auto-ranging ADC. The drawback of this approach is that it is difficult to obtain a high degree of linearity. The work presented in this paper utilizes an auto-ranging preamp which is followed by a fixed gain ADC. The four channel preamp IC uses a calibration and digital correction technique to obtain a high degree of linearity ($\leq$0.01% of input level) over the entire signal range.



(a)



(b)

Fig. 1. (a) Illustration of a variable step size ADC when used with an auto-ranging preamp and (b) effect of gain error on the ADC transfer characteristic and on the absolute error $AbbsErr$ at point x.

In Section II, the basic circuit architecture is discussed. Section III describes the circuit details and Section IV gives an

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TABLE I
GAIN RANGES AND GAIN ERROR

Bits	Gain Ranges G							Max. ε
14	1	2	4	8	16	32	64	$3.9\text{x}10^{-5}$
15	1	4	16	64				$4.0\text{x}10^{-5}$
	1	2	4	8	16	32	64	$7.0\text{x}10^{-5}$
16	1	8	64					$4.1\text{x}10^{-5}$
	1	4	16	64				$7.0\text{x}10^{-5}$
	1	2	4	8	16	32	64	$8.5\text{x}10^{-5}$

overview of the calibration routine. A detailed noise analysis of the circuits is provided in Section V and experimental results from the implemented chip are given in Section VI.

II. CIRCUIT ARCHITECTURE

In this application, a linearity of 0.01% of input reading ±0.25 ppm of full scale and a dynamic range of 20 bits are required. The use of a low-noise, auto-ranging programmable gain amplifier with a suitable ADC results in small step sizes for low signal levels, where only a small linearity error can be tolerated, and larger step sizes for higher signal levels where larger linearity error is allowed. This concept is illustrated in Fig. 1(a). In addition, the use of variable gain allows the circuit to be optimized for noise performance on the most sensitive high gain setting. The selection of the number of gain ranges and values and the resolution of the ADC will determine the dynamic range and linearity. Analysis has shown that as the number of gain ranges is increased, the amount of tolerable gain mismatch between ranges is relaxed. If the ideal gain is G_i for a given gain range i, then the actual gain can expressed as $G_i(1+\varepsilon_i)$, as shown in Fig. 1(b). In order to meet the linearity specification above, it can be shown (see the Appendix) that the maximum allowed gain error ε_i is given by

$$\varepsilon_i \leq 10^{-4} - \frac{0.5R^{i-1} - \delta}{2^{\text{bits}} \cdot R^{i-2}} \tag{1a}$$

where bits is the ADC resolution and R is the ratio of gains between adjacent ranges. The constant δ represents the 0.25 ppm of full scale factor; its value is a function of bits,R and the number of gain ranges n_R and can be expressed as,

$$\delta(n_R, \text{bits}, R) = R^{n_R-1} \cdot 2^{\text{bits}-22}. \tag{1b}$$

Table I shows the maximum allowed gain error ε_i for several gain combinations when an ADC with a resolution of 14, 15, and 16 bits is used. Based on these calculations, a practical selection of gain ranges that maximizes the allowed gain error ε_i is 1, 2, 4, 8, 16, 32, and 64 when used with a 16-bit ADC.

The overview of the chip architecture in Fig. 2 illustrates how these gains are obtained over two stages. Dividing the gain into two stages simplifies the gain circuitry and allows more accurate calibration to be performed. The preamplifier selects a gain of one or eight depending on the voltage level sensed by the comparator. Then a four-bit flash ADC is used to determine the appropriate gain setting for the programmable gain amplifier (PGA). An off-chip calibration and digital correction routine, described later, is used to correct for offsets and gain mismatches between ranges.

III. CIRCUIT DESIGN

Switched-capacitor circuit techniques are used to implement the preamp, PGA, and sample-and-hold (S/H) stages. The basic principle of operation of the switched-capacitor PGA is similar to the technique used in charge-redistribution ADC's [4] and is illustrated in Fig. 3. During the reset phase, the input current source is disconnected from the amplifier and all the feedback capacitors have one end connected to ground in order to sample the amplifier's offset. In the following integrate phase, the source is connected to the amplifier and the current is integrated across all the capacitors which are now connected in feedback around the amplifier. In the final amplify phase, with the source disconnected, selected feedback capacitors have one end grounded, forcing their charge to be reinjected into the remaining capacitors in feedback across the opamp. The resulting gain is given by

$$v_2 = v_1\left(1 + \frac{C_1}{C_2}\right) \tag{2}$$

where C_1 is the sum of the capacitance switched to ground and C_2 is the total capacitance remaining in feedback. This property can be extended to provide binary weighted gains.

The binary gain PGA is implemented using an array of N binary weighted capacitors ranging in value from C to $2^{N-1}C$, along with an additional unit capacitor as shown in Fig. 4. Adding the extra capacitor makes the total capacitance of the network equal to 2^NC. In Fig. 4(a), all N capacitors are connected to the output of the opamp, and the output is assumed to be at an arbitrary voltage v_1. Then, in Fig. 4(b), capacitors 2^iC through $2^{N-1}C$ are connected to ground and all other capacitors remain in feedback. In this circumstance, the total feedback capacitance is 2^iC and the total capacitance to ground is $(2^N - 2^i)C$. As a result of (2), the resulting gain for Fig. 4(b) is

$$Gain = \frac{v_2}{v_1} = 1 + \frac{2^N - 2^i}{2^i} = 2^{N-i}. \tag{3}$$

Thus, all binary gains from unity to 2^N can be provided by this switched capacitor circuit.

The overall circuit implementation is shown in Fig. 5. Basic circuit operation can be summarized as follows: during phase ϕ_1, the preamp is reset; in the next phase ϕ_2, the PGA is reset with one side of its capacitors switched to ground so that the opamp offset is sampled; the noise and offset of the preamp are sampled on capacitor C_c, with only the small capacitor C_{f1} in feedback around the preamp; this ensures that the noise and offset are optimized for the high gain setting on the preamp. The sampling action of C_c also performs a correlated double sampling (CDS) for reducing the $1/f$ noise of the preamp [5]. During phase ϕ_3, the photodiode is connected to the preamp, and the charge is integrated on the high gain setting (only C_{f1}

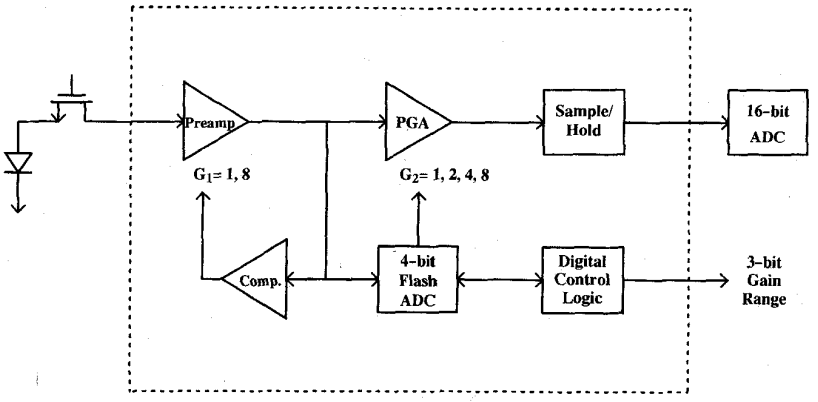


Fig. 2. Overall architecture of the auto-ranging gain preamplifier.

in feedback); the PGA is in unity gain mode with all of its capacitors in feedback. The comparator checks the preamp's output voltage 40 μs into phase ϕ_3; if the output has risen more than halfway past the full-scale value, then capacitor C_{f2} is switched into feedback, which sets the preamp into the low-gain mode. Right before the end of phase ϕ_3, switch M3 disconnects the preamp stage from the PGA stage. This allows the preamp to be reset in the following phase ϕ_1, while the PGA auto-ranges to the correct gain setting. The four-bit flash ADC samples the preamp output in order to determine the correct gain setting for the PGA. This flash converter simply consists of three comparators with a resistor string generating the appropriate reference voltages and some digital logic for decoding the thermometer code output. As described above, the PGA gain is obtained by switching the appropriate number of capacitors to ground. For example, in the unity gain mode, all the capacitors are in feedback around the PGA opamp, and in the gain of eight mode, only a single 4 pF capacitor is in feedback, with the remaining capacitors switched to ground.

The preamp circuit is designed to handle a maximum input charge of 210 pCb per 1 ms integration cycle. The capacitor values and opamps were designed to accommodate a 4 V signal swing for a full-scale input. A folded cascode opamp design was used because of its good stability when driving large capacitive loads and its excellent power supply rejection characteristics. The opamps were powered from $\pm$6 V rails in order to ensure enough headroom for the cascode devices when the opamp outputs swing $\pm$4 V. Shield devices in the cascode, proposed by Laber *et al.* [6], were used to minimize the effects of impact ionization on the cascode devices. The opamp design resembles the one in [6], although it has been optimized for low noise through the appropriate choice of bias currents and device sizes. Most of the power is dissipated in the first opamp (15 mW) since its noise performance is most critical. The PGA and S/H opamps dissipate 6 mW and 2.5 mW respectively.

The effects of charge injection from the switches are a concern since it can be a source of signal and temperature dependent offset. The critical switches are the ones which can inject charge into the summing junction of the opamps when they turn off. Any offset induced by the turning off of switch M2 in the first integrator is cancelled by the CDS

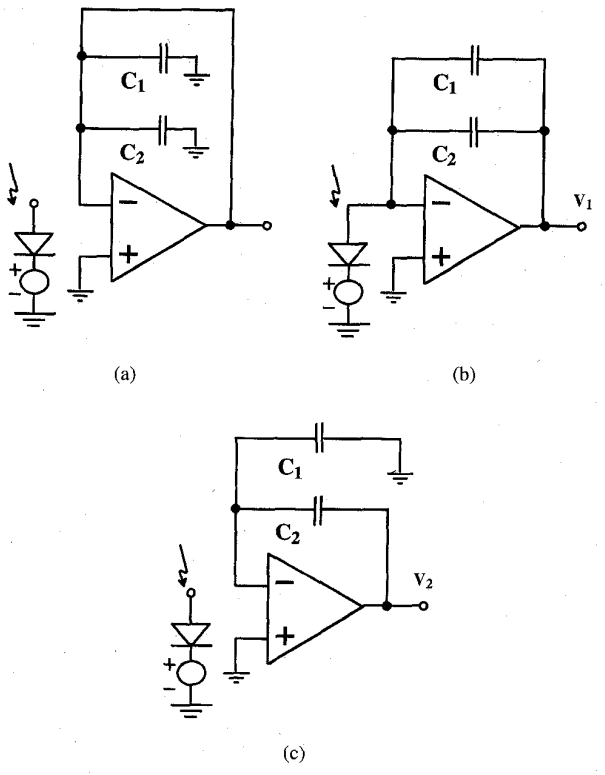


Fig. 3. Basic operation of the programmable gain amplifier: (a) reset phase, (b) integrate phase, and (c) amplify phase with gain $1 + C_1/C_2$.

stage. For the other switches, like M3 and M4, the amount of charge injection is minimized by their small size (W/L = 8 μm/3.5 μm). Also, the switches are composed of equal sized p-type metal-oxide semiconductor (PMOS) and n-type metal-oxide semiconductor (NMOS) devices which ensure that the parasitic clock feedthrough is cancelled to first order. The excellent offset temperature drift results described later (0.1 ppm/°C) validate the effectiveness of this approach.

IV. Calibration

By careful layout of the capacitors, matching to within 0.1% is possible. However, in order to obtain a linearity of

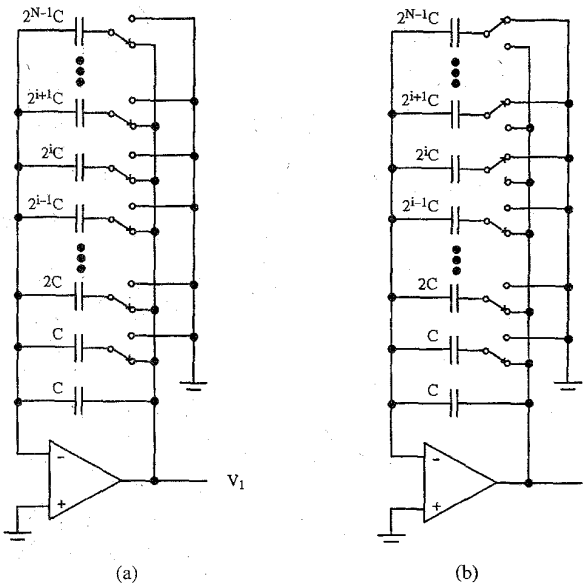


Fig. 4. PGA implementation for obtaining binary weighted programmable gains. (a) PGA acquires signal with all capacitors in feedback. (b) Feedback capacitors switched to obtain gain of 2^{N-i}.

0.01%, the calculations summarized in Table I show that the gains must match between ranges to better than 0.0085%. Off-chip digital correction is used to achieve the required matching. This approach avoids the need of analog calibration circuitry, thus simplifying the design; the correction logic can be combined with the other digital signal conditioning circuitry after the ADC. The nonidealities to be corrected for are the offsets and gain mismatches of the preamp and PGA stages and the offset in the ADC as shown in Fig. 6.

In calibration mode, a reference voltage is input through the V_{ref} pin which charges up the capacitor C_{cal}. By switching C_{cal} from V_{ref} to ground, a constant signal for calibrating the chip is injected into the preamp. The gain range can be set externally during calibration mode. The digital multiplication block ensures that there is a consistent gain of 64 from the input to the digital output D_{out} for all gain settings in the analog preamp chip. The offsets for each gain setting are recorded first; with $V_{\text{ref}} = 0\text{V}$, each gain combination on the Preamp and PGA is set, and the resulting output is digitized to 16 b using the off-chip ADC, and recorded. Next, the gain ranges are calibrated by setting $V_{\text{ref}} = 4\text{V}$ and recording the digitized ADC output after correcting for the previously computed offset. Note that the size of C_{cal} yields gains of $1 - \delta_1$ and $1/8 - \delta_2$ for the preamp stage in calibration mode, where $\delta_i \ll 1$. The added δ_i factor ensures that the preamp will not over-range during calibration due to uncorrected gain errors. Analysis and simulation have shown that in order to achieve the required level of gain matching through the calibration routine, the gain readings must be digitized to 19 bits of resolution; however, the integral linearity is only required to be within two bits at 16 bits of resolution. This can be achieved by sufficiently oversampling the 16-bit ADC during calibration mode. Digital correction terms are calculated by comparing the digitized output values for various gain settings. During auto-ranging operation, each output of the ADC is digitally corrected by subtracting the offset and multiplying by the appropriate gain correction term

$$Dout_{corr} = (D_{out} - offset[range1][range2]) \times G_{1Corr}[range1] \times G_{2Corr}[range2] \quad (4)$$

where $range1$ and $range2$ refer to the particular range selected on the preamp and PGA stage, $offset$ refers to the offset reading and G_{1Corr} and G_{2Corr} refer to the gain correction terms. In our application which involves extensive digital signal processing of the readout data, the added overhead of the calibration routine (one subtraction and two multiplications per data read out) is minimal.

V. Noise Analysis

The noise is most critical on the highest gain range where the input signal is the smallest. The goal of this design is to keep the noise to less than 2 ppm of full-scale when referred to the input on the highest gain range. On the highest gain setting, only the small capacitor $C_{f1} = 7.3$ pF is in feedback and the voltage gain of the PGA is $g_{pga} = 8$. Since the maximum input charge is 210 pCb, the noise must be less than 0.5 fCb input-referred or under 550 μV output-referred. The resistances R_{in}, R_c, R_f, R_h, and R_{h2} have been inserted into the circuit in order to bandlimit the amount of opamp noise sampled on the capacitors. The thermal noise of the resistors does not increase the overall noise of the circuit since the sampled noise on the capacitors remains kT/C, independent of the resistance connected to them.

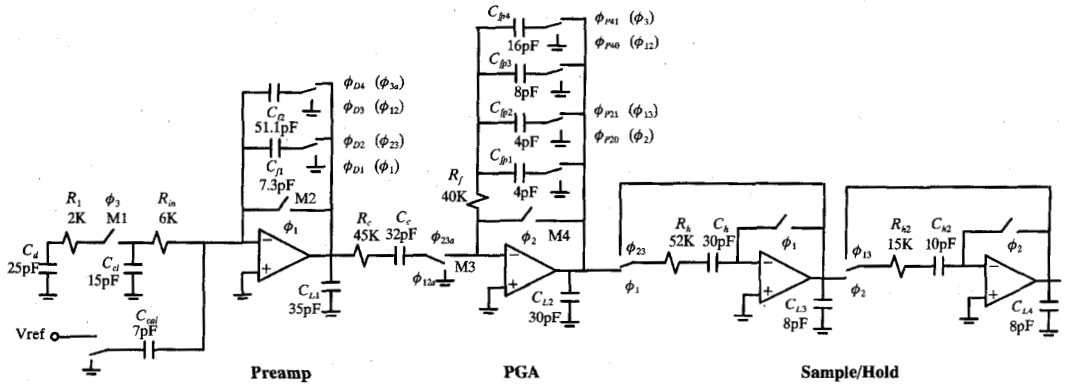
The noise due to resistance of switch M1 (represented by $R1$ in Fig. 5) is given by its thermal noise sampled onto the diode capacitance C_d and by its thermal noise sampled on C_c, bandlimited by its RC low pass filter. Therefore, a reasonable upper bound for the output-referred mean squared voltage for M1 is given as

$$\overline{V}_{M1}^2 = \left[\frac{kT}{C_d} + \frac{kTR_1}{R_cC_c}\right]\left(\frac{C_d}{C_f}\right)^2 \cdot g_{pga}^2. \quad (5)$$

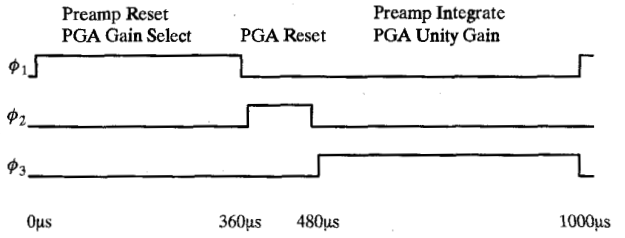
The first term is the noise sampled on the detector capacitance C_d and the second term is the thermal noise due to R_1 sampled on the CDS capacitor C_c. Note, that the first term in the above expression includes noise sampled on C_d due to the resistor R_{in}, so the remaining noise due to R_{in} is given by

$$\overline{V}_{Rin}^2 = \frac{kTR_{in}}{R_cC_c}\left(\frac{C_d + C_{cl}}{C_f}\right)^2 \cdot g_{pga}^2. \quad (6)$$

Although the presence of resistor R_{in} increases the noise by the above expression, it reduces the amount of noise sampled on C_d from the preamp opamp, as seen in the expression below for V_{en1}. The thermal noise due to switch M2 is sampled on the small preamp feedback capacitor C_{f1} and is then canceled by the effect of the correlated double sampling. Note that this noise source is cancelled only in the high gain setting of the preamp, where the noise is most critical. In the CDS circuit, the R_cC_c low pass filter allows most of the noise across C_{f1} to be sampled and cancelled while effectively limiting the amount of opamp noise sampled across C_c. As the noise sampled across



(a)



(b)

Fig. 5. Circuit details and timing diagram for the auto-ranging gain preamplifier.

C_{f1} is cancelled to within 1%, its noise contribution is given by

$$\overline{V}_{Cf}^2 = (0.01)^2 \cdot \frac{kT}{C_{fl}} \cdot g_{pga}^2. \tag{7}$$

The noise sampled on capacitors C_c, C_{fp}, and C_h due to the thermal noise of the switches connected to these capacitors is given by

$$\overline{V}_{Cc}^2 = \frac{kT}{C_c} \cdot g_{pga}^2 \tag{8}$$

$$\overline{V}_{Cfp}^2 = \frac{kT}{C_{fp}} \tag{9}$$

$$\overline{V}_{Ch}^2 = \frac{kT}{C_h}. \tag{10}$$

C_{fp} represents the total capacitance connected in feedback around the PGA opamp. Assuming the opamp has its noise modeled as an input referred noise source at its positive input, the contribution of preamp due to a white noise source with power e_{n1}^2 is

$$\overline{V}_{en1}^2 = \left[\frac{e_{n1}^2}{4R_cC_c}\left(1 + \frac{C_d + C_{cl} + C_{in}}{C_f}\right)^2 + \frac{e_{n1}^2}{4R_cC_C}\left(1 + \frac{C_{cl} + C_{in}}{C_f}\right)^2 + \frac{e_{n1}^2}{4R_{in}(C_d + C_{cl})}\left(\frac{C_d}{C_f}\right)^2 \right] \cdot g_{pga}^2. \tag{11}$$

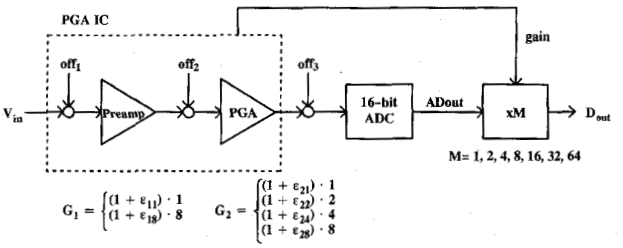


Fig. 6. Offsets and gain-errors that need to be calibrated out of the system.

The first term is the white noise source multiplied by the non-inverting gain factor of the opamp, sampled on the CDS capacitor C_c at the end of clock phase ϕ_3. The second term is due to the noise source sampled on C_c at the end of clock phase ϕ_2; here it is assumed there is no correlation between this sample and the first term is sample. The third term is the opamp noise sampled onto the diode capacitance C_d and referred to the output. Capacitor C_{cl} represents the parasitic line capacitance in the photodiode array and C_{in} includes the input capacitance of the preamp opamp as well as the calibration capacitance C_{cal}, which has one end switched to ground during normal operation. The noise contribution due to the flicker noise at the opamp input was computed using the expression

$$\overline{V}_{1/f1}^2 = g_{pga}^2 \cdot \int_{f_0}^{f_1} \frac{K_{fl}}{f}\left(1 + \frac{C_{cl} + C_{in}}{C_f}\right)^2 4 \cdot \sin^2\left(a_1 \frac{\pi f}{f_s}\right) \cdot \frac{1}{1 + (2\pi f R_c C_c)^2}\, df. \tag{12}$$

TABLE II
PREAMP NOISE

Noise Source	Input Referred (fCb)	Output Referred (μV)
V_{M1}	0.328	365
V_{Rc}	0.167	185
V_{Cf}	0.002	2
V_{Cc}	0.082	91
V_{Cfp}	0.010	11
V_{Ch}	0.010	12
V_{en1}	0.244	271
$V_{1/f1}$	0.064	71
V_{en2}	0.043	48
$V_{1/f2}$	0.026	29
Total	0.463	507

The sin term is due to the CDS [7]; a_1 is the fraction of the clock period between double sampling, f_s is the clock sampling frequency and K_{f1} is the flicker coefficient. The expression was numerically integrated from a lower bound of $f_0 = 1$Hz to the unity-gain bandwidth of the opamp, f_1; the intergrand is attenuated well below the upper bound frequency by the low pass filter provided by R_c and C_c. The noise due to the thermal noise of the PGA opamp is given by

$$\overline{V}_{en2}^2 = \left[\frac{e_{n2}^2}{4R_hC_h} + \frac{e_{n2}^2}{4R_cC_c} + \frac{e_{n2}^2}{4R_fC_{fp}}\right] \cdot g_{pga}^2 \qquad (13)$$

where the first term is the noise sampled on the sample-and-hold stage, the second term is the noise sample on the capacitor C_c and the third term is due to the noise sampled on all the feedback capacitors during the reset phase of the PGA amplifier. Note that resistor R_f is used to limit this noise. The flicker noise due to the PGA amplifier is given by

$$\overline{V}_{1/f2}^2 = g_{pga}^2 \cdot \int_{f_0}^{f_1} \frac{K_{f2}}{f} 4\sin^2\left(a_2\frac{\pi f}{f_s}\right) \cdot \frac{1}{1+(2\pi f R_hC_h)^2}\, df. \qquad (14)$$

The CDS action occurs because the PGA opamp offset and low-frequency noise are sampled on the feedback capacitors C_{fpi} during phase ϕ_2; the constant a_2 represents the fraction of time between the initial sampling of the opamp noise at the end of phase ϕ_2 and the sampling of the PGA output by the sample-and-hold stage at the end of the following phase ϕ_1.

Based on the above equations, it was determined that the noise specification can be met if the preamp and PGA opamps have the following thermal and $1/f$ noise characteristics: $e_{n1} = 6$ nV/$\sqrt{\text{Hz}}$, $K_{f1} = 2.6 \times 10^{-13}$ V^2, $e_{n2} = 8.5$ nV/$\sqrt{\text{Hz}}$ and $K_{f2} = 1 \times 10^{-12}$ V^2. The theoretically calculated noise for each term, referred to both the output and input, is summarized in Table II. Note that the preamp circuits only increase the noise by 3 dB above the minimum noise set by the kTC_d noise of the photodiode capacitance.

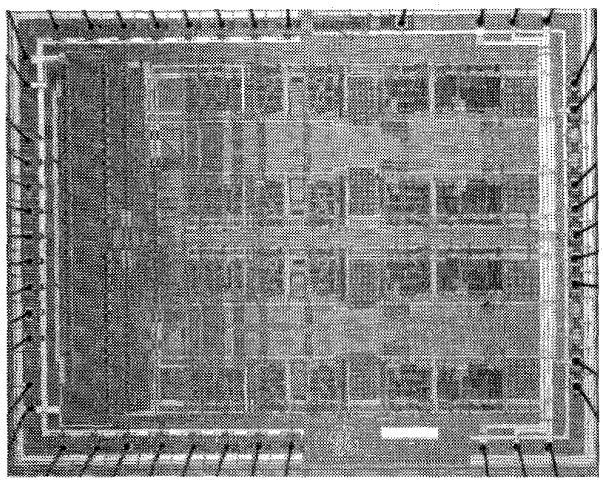


Fig. 7. Microphotograph of the four-channel auto-ranging gain preamplifier die.

VI. EXPERIMENTAL RESULTS

The chips were fabricated in a 1.5 μm double poly CMOS process. There are four channels per chip plus digital logic for generating the clocks and determining the gain settings, as shown in the microphotograph in Fig. 7. The chip was tested using a commercial 16-bit ADC part. The calibration of the data was implemented off-chip. Using a 1ms integration time, the linearity specification of 0.01% of reading $\pm$0.25 ppm of full scale is attained after the chip has been calibrated and the output data digitally corrected. A typical plot showing the measured linearity error after the calibration and digital correction of the output data is shown in Fig. 8. A least-squares fit to the output data is used to obtain the ideal linear fit. The correlation of error with the gain ranges is evident. Without the digital correction, a linearity error of 0.6% of reading is typically measured. The output-referred noise with an unswitched 25 pF capacitor at the input is approximately 440 μV, which is in good agreement with a theoretically predicted value of 400 μV for this case. (The predicted noise value of 507 μV from the previous section represents the intended application for this chip when it is to be used with a switched photodiode input which has a capacitance of 25 pF.) The 5.8 mm $\times$ 7.4 mm die consumes 135 mW of power from $\pm$6 V supplies. The IC was also tested over a temperature range of 0°C to 50°C. The offset drift with temperature was found to be under 0.1 ppm/°C and the gain drift with temperature was 14 ppm/°C. The test results are summarized in Table III.

VII. CONCLUSION

An IC which has a low noise preamplifier for integrating input charge and auto-ranging gain capability has been demonstrated. This sensor preamp interface chip can be used with a 16 bit ADC to digitize the charge input from photodiode sensors to 20 bit resolution. By calibrating the chip and using digital post-processing, linearity better than 0.01% of reading is obtained. In addition, the use of the PGA chip to lower the resolution of the required ADC allows a sufficiently fast

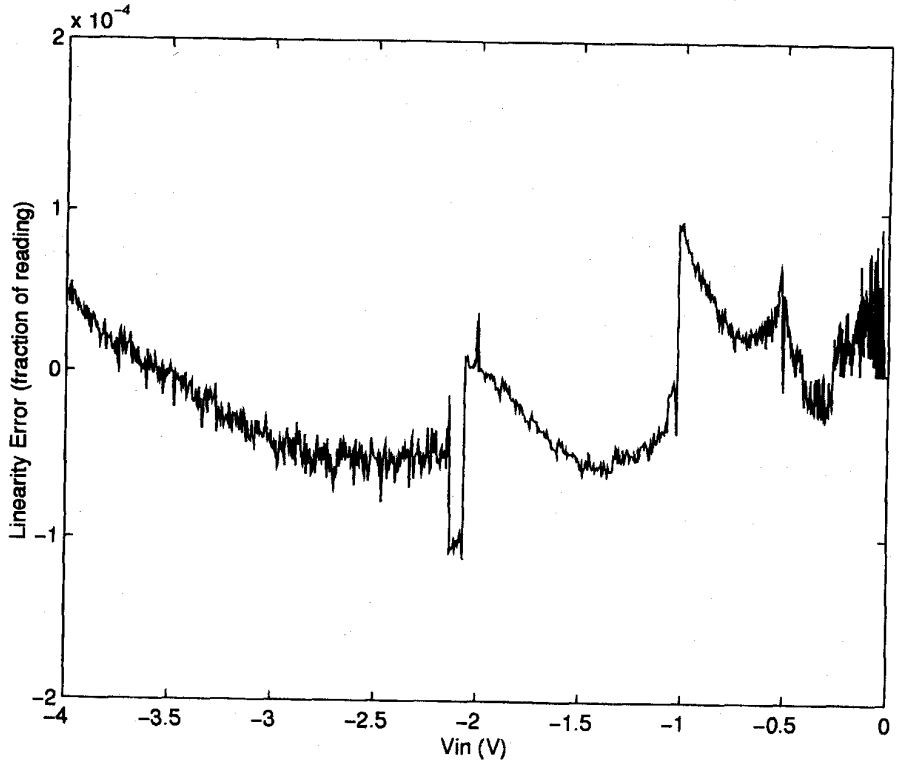


Fig. 8. Plot of the linearity error as a fraction of the input reading after digital correction.

TABLE III
SUMMARY OF THE PGA CHIP

Technology	1.5/3.5 μm CMOS
Die Size	7.4 x 5.8 mm^2
Sample Rate	1 kHz
Full scale input	210pCb
Linearity	0.01% of reading
Noise (input referred)	0.4fCb
Dynamic Range	114dB
Offset Temp. Drift	0.1 ppm/°C
Gain Temp. Drift	14 ppm/°C
Power Dissipation (4 channels)	135 mW

conversion to be obtained to allow several channels to be multiplexed to a single ADC chip.

APPENDIX

The theory behind the selection of the gain ranges is detailed in this appendix. The goal is to find suitable values for the following parameters: the number of gain ranges, n_R; the number of bits in the A/D converter, bits; and the ratio between adjacent gain ranges, R. For example, in the chip described in this work, $n_R = 7, \text{bits} = 16$ and $R = 2$. This yields the gains of 1, 2, 4, 8, 16, 32, and 64. Note that the combined effect of the PGA and A/D results in a full-scale output in counts given as

$$\text{Fullscale in counts} = R^{n_R-1} \cdot 2^{\text{bits}}. \tag{A.1}$$

Thus, it can be seen that the A/D output provides a mantissa with a maximum value of $2^{\text{bits}} - 1$ and the gain selection provides the exponent ranging in value from 1 to $n_R - 1$ with a base of R. The linearity specification for this system can be expressed as

$$\frac{AbsErr - \delta(n_R, \text{bits}, R)}{G_{io} \cdot V_{in}} \leq 10^{-4} \tag{A.2}$$

where $AbsErr$ is the absolute error for any given input expressed in counts, G_{io} is the input to output gain factor which is used to convert the input V_{in} into counts; δ is equal to 0.25 counts for a 20-bit full scale system and therefore its value in counts will vary depending on the actual full-scale of a given system. The δ essentially represents the allowed error for very small inputs, i.e., when 0.01% of reading error is below 0.25 ppm of full scale. Using (A.1), δ can be calculated as

$$\delta(n_R, \text{bits}, R) = R^{n_R-1} \cdot 2^{\text{bits}-22}. \tag{A.3}$$

Let the gain ranges be numbered from $i = 1 \cdots n_R$, where $i = 1$ represents the highest gain and $i = n_R$ is the lowest gain. By definition, the highest gain range will have a step size of one count, the second highest will have a step size of R counts, etc. Thus, the step size in counts in gain range i is given as

$$\Delta_i = R^{i-1}. \tag{A.4}$$

If it is assumed that there are no sources of nonidealities, the maximum absolute error in a given gain range can be approximated as half the converter step size in that gain range.

Since the linearity specification is most difficult to meet for small inputs, i.e., in the gain range $i = 1$, it is desirable to set

$$\frac{\Delta_1}{2} \leq \delta(n_R, \text{bits}, R)$$
$$\therefore \frac{1}{2} \leq R^{n_R-1} \cdot 2^{\text{bits}-22} \quad \text{(A.5)}$$

where the fact that the maximum $AbsErr$ on the highest gain range is half the step size, i.e., $\max[AbsErr1] = \Delta_1/2 = 0.5$ counts. If a gain error ε_i is introduced [see Fig. 1(b)], then the maximum absolute error in a given gain range i is given by

$$\max[AbsErr_i] = \frac{\Delta_i}{2} + \varepsilon_i \cdot V_{in(i)}. \quad \text{(A.6)}$$

$V_{in(i)}$ is the input in gain range i expressed in counts, so that the conversion factor G_{io} used in (A.2) is assumed to be used implicitly, i.e., $V_{in(i)} = G_{io} \cdot V_{in}$. Using (A.2) with (A.6), the linearity specification is satisfied for every gain range i provided

$$V_{in(i)} \geq \frac{\Delta_i/2 - \delta}{10^{-4} - \varepsilon_i} \quad \text{(A.7)}$$

where $\delta = \delta(n_R, \text{bits}, R)$. In order to derive the conditions for the maximum allowed gain error ε_i, note that as ε_i increases in value but remains less than 10^{-4}, the right-hand side of (A.7) increases in value. For a given gain range i, $V_{in(i)}$ is bounded in value by

$$B_{i-1} \leq V_{in(i)} \leq B_i. \quad \text{(A.8)}$$

B_i is defined as the value in counts where the transition from gain range i to $i+1$ is made and can be expressed as

$$B_i = R^{i-1} \cdot 2^{\text{bits}} \quad \text{(A.9)}$$

Therefore, setting $V_{in(i)}$ to its minimum value of B_{i-1} in (A.7) will give the maximum allowed value for ε_i. Combining (A.4), (A.7), and (A.9) yields the condition on the gain error ε_i for gain range i

$$\varepsilon_i \leq 10^{-4} - \frac{0.5R^{i-1} - \delta}{2^{\text{bits}} \cdot R^{i-2}}. \quad \text{(A.10)}$$

Equations (A.5) and (A.10) are used to select the appropriate values for n_R, bits and R in order to satisfy the linearity specifications. For example, in the case with $R = 2$, the equations become

$$n_R + \text{bits} \geq 22$$
$$\varepsilon_i \leq 10^{-4} - 2^{-\text{bits}} + 2^{-21+n_R-i}. \quad \text{(A.11)}$$

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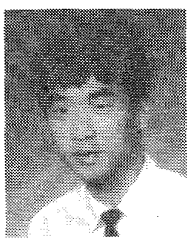

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