A Low-Voltage, Low-Power CMOS Delay Element

Gyudong Kim, Min-Kyu Kim, Byoung-Soo Chang, and Wonchan Kim

Abstract—**A low-voltage, low-power CMOS delay element is proposed. With a unit CMOS inverter load, a delay from 2.6 ns to 76.3 ms is achieved in 0.8 μm CMOS technology. Based on a CMOS thyristor concept, the delay value of the proposed element can be varied over a wide range by a control current. The inherent advantage of CMOS thyristor in low voltage domains enables this delay element to work down to the supply voltage of 1 V while the threshold voltage of the nMOS and pMOS transistors are 840 mV and −770 mV, respectively. The designed delay value is less sensitive to supply voltage and temperature variation than RC-based or CMOS inverter-based delay elements. Temperature compensation and jitter performance in noisy environment are also discussed.**

I. Introduction

DELAY elements are widely used in digital systems and are essential parts for self-timed operation in high speed VLSI and phase modulation such as delay locked loops (DLL's) or phase locked loops (PLL's) [1]–[4].

Inverter chain and RC delay method have been the most common delay elements in those applications. Both of them are simple and easy to design. However, the characteristics of the delay elements are sensitive to environmental conditions such as supply voltage and ambient temperature. Attempts to find a delay element less sensitive to supply voltage and temperature variations have been made [1], [2].

A differential stage chain provides stable characteristics but consumes static power, requires a complex biasing circuitry for delay variation, and, in general, is not feasible to implement a large delay value with differential stages. Biasing techniques with feedback mechanism can enhance the figure of sensitivity. But such approaches cannot compensate such high frequency perturbation as the power line noise, which causes metastability in synchronous systems [5].

In this paper, a delay element is proposed which is suitable for low-voltage operation. The proposed delay element is less sensitive to environmental conditions such as supply voltage and temperature than RC or inverter-chain based delay elements since the major component of the delay is controlled by the current source. This delay element does not consume static power and the power consumption decreases with the increasing delay value. In Section II, a CMOS circuit equivalent of thyristor is introduced and the concept of the delay element based on the CMOS thyristor is proposed. In Section III, the full circuit schematics and detailed operation principle of this delay element are explained. In Section IV, the simulated characteristics of this delay element are provided and compared to those of other delay elements.

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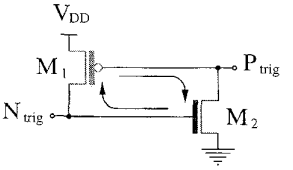

Fig. 1. Concept of the CMOS thyristor.

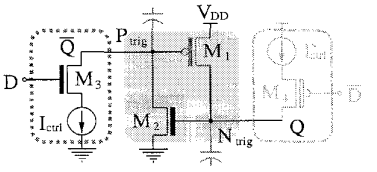

Fig. 2. Concept of the delay element based on the CMOS thyristor.

II. Concept of the Delay Element

Fig. 1 is a conceptual circuit which acts as if it is a thyristor [6]. When $P_{\rm trig}$ is precharged to V_{DD} and $N_{\rm trig}$ is predischarged to ground, the thyristor is turned off. The thyristor can be triggered with the potential of either $P_{\rm trig}$ or $N_{\rm trig}$. Without loss of generality, $P_{\rm trig}$ is assumed as the triggering node. Until $P_{\rm trig}$ is discharged down to $V_{DD} - V_{Tp}$, M_1 conducts at most the subthreshold current. This feature provides negligible power consumption before the turn-on of the thyristor. Once M_1 is turned on, M_1 charges $N_{\rm trig}$ and M_2 discharges $P_{\rm trig}$ in turn. The positive feedback mechanism in this turn-on operation provides a quick flipping of the state and reduces the dynamic power consumption. Note that no current flows directly from V_{DD} to ground. Since there are no stacked structures which require more voltage margin, this CMOS thyristor can operate with a low supply voltage. This allows the low voltage operation of the delay element.

A delay element can be built with this CMOS thyristor and a control current source for triggering the thyristor. Fig. 2 is a delay element based on the CMOS thyristor. The shaded part with transistor M_3 is for triggering on the rising edge of signal D and that with transistor M_4 is for triggering on the falling edge. M_3 detects the rising edge of D and starts to discharge $\overline{Q}$ with $I_{\rm ctrl}$. Once M_1 is turned on, the positive feedback mechanism of the CMOS thyristor causes the delayed rising edge of the input signal to arrive at node Q. The same triggering can be done with M_4 in the complementary manner.

Fig. 3 shows the simulated waveforms and the supply current of the proposed delay element with 3 V supply. The

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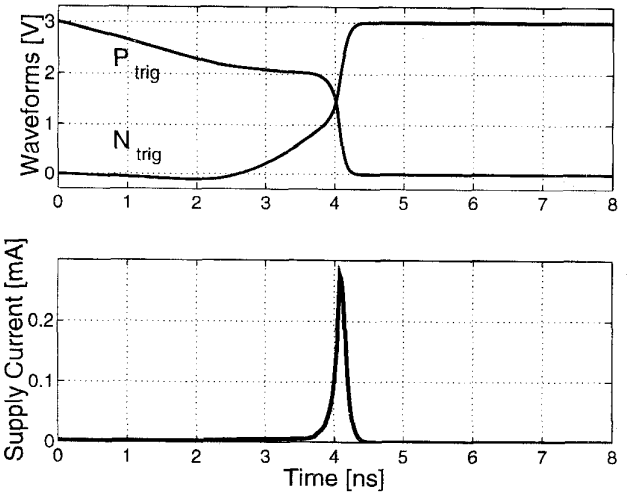


Fig. 3. Simulated waveforms and supply current of the delay element.

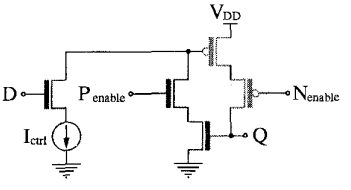


Fig. 4. Half-circuit of the delay element.

TABLE I
SUMMARY OF A QUALITATIVE COMPARISON OF THE VARIOUS DELAY ELEMENTS

Circuit	Inverter Chain	RC Delay	Differential Pair	Proposed one
Static Power	no	no	yes	no
Energy/Toggle	$\propto t_d$	$\propto t_d$	$\not\propto t_d$	$\not\propto t_d$
Supply Sensi.	high	medium	low	low
Temp. Sensi.	high	medium	low	very low

proposed delay element does not conduct noticeable amount of current until the CMOS thyristor is triggered. Once the CMOS thyristor is triggered, the element is instantly flipped and does not consume the static power any more.

With a simple analysis, the delay value of the proposed element calculated as

$$t_d = \frac{C_1 V_{T1}}{I_{\text{ctrl}}} + \sqrt[3]{\frac{6C_2C_1^2}{\kappa_1 I_{\text{ctrl}}^2}} V_{T2} + \delta t \qquad (1)$$

where the subscript 1 is for the driving transistor and 2 is for the driven transistor in a CMOS thyristor, and δt is the time for the regeneration at the CMOS thyristor which is a minor component of the delay value but sensitive to the supply voltage. Since the major components of the delay value are insensitive to the supply voltage, the characteristics of this delay element is less sensitive to the variation of the supply voltage. Hence, with smaller I_{ctrl}, i.e., larger delay value, the delay element gets less sensitive to the supply voltage variation. From (1), the delay value is determined by the control current, I_{ctrl}. The second term shows the dependency of the delay value to the temperature variation with κ.

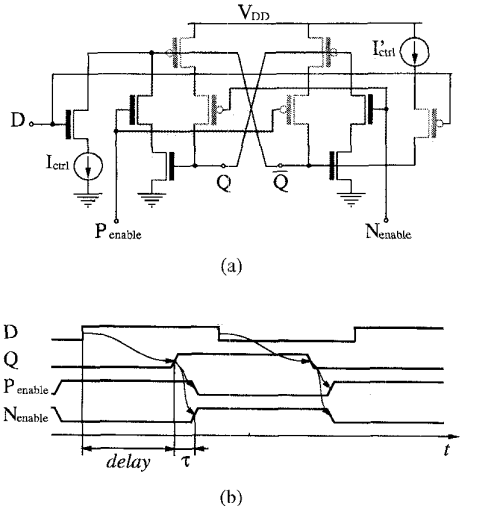


Fig. 5. Proposed delay element with dynamic triggering. (a) Circuit schematic. (b) Timing diagram.

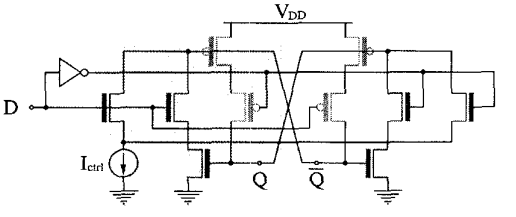


Fig. 6. Proposed delay element with static triggering.

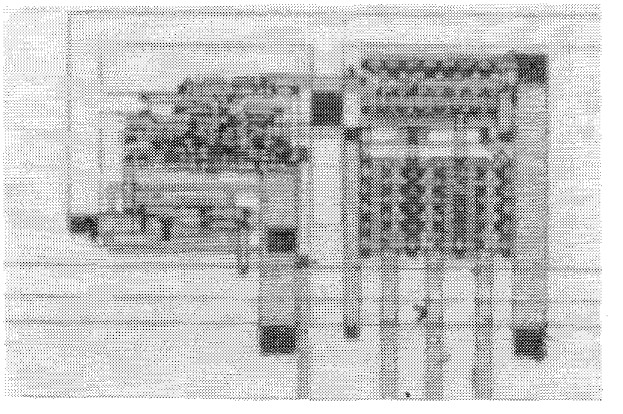


Fig. 7. Microphotograph of the prototype with 0.8 μm CMOS technology. Active area is 42 μm $\times$ 28 μm without input–output buffers.

Qualitative comparisons of the various delay elements are summarized in Table I.

III. CIRCUIT DESCRIPTION

The circuit in Fig. 2 is not complete, as it will operate once only. Once the state of the circuit is flipped over, the CMOS thyristor should be turned off and precharged before the next transition. Fig. 4 is the half-circuit with the switch-transistors which are in the shaded area.

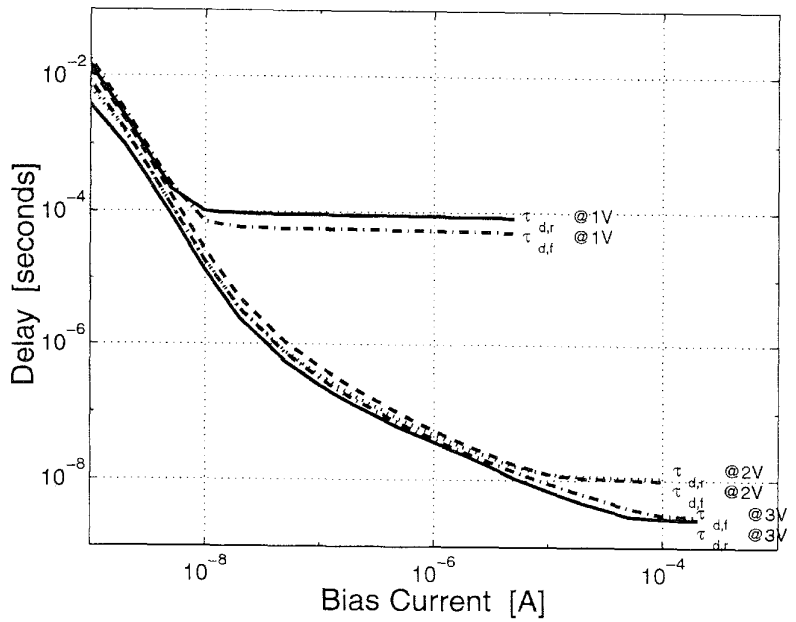


Fig. 8. Measured delay characteristics of the proposed delay element to I_{ctrl} and V_{DD}.

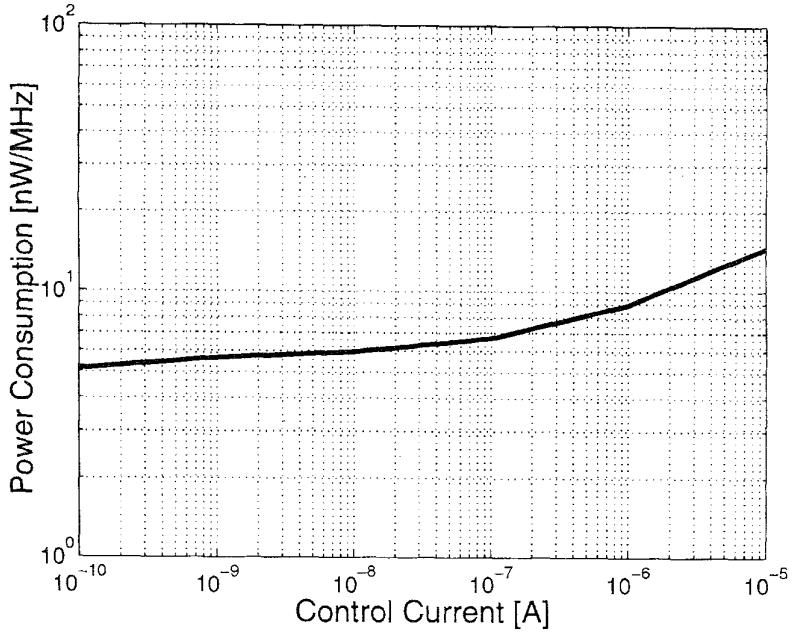


Fig. 9. Simulated power consumption of the proposed delay element to I_{ctrl}.

Full implementation of the delay element uses two of the half circuits, activated at different edges of the input signal. Additional precharge circuitry is not required as each half-circuit functions as the other's precharge circuit. Fig. 5 is the circuit schematic of the delay elements with dynamic triggering. The shaded part is for the selective enable of each half circuit for the expected switching of input signal D. The left half is for the rising edge, and the right half is for the falling edge.

Dynamic triggering prevents shunt current which would cause higher power consumption and spike noise on the power line, but requires an internal delay element τ for dynamic timing generation. The delay τ is required for the flipping of the signal Q in dynamic triggering. Since flipping is a characteristic of the feedback mechanism of the CMOS thyristor, the required delay τ is quite small (less than 1 ns in a 0.8 μm CMOS technology with minimum transistor sizes) and can be easily implemented with conventional delay elements. The variation of the characteristics of the delay element for τ does not cause variation in the delay characteristics of the proposed delay element. Since the required delay τ is small, the impact on the power consumption from the assistant delay element is not so important for a target delay value larger than 2 ns.

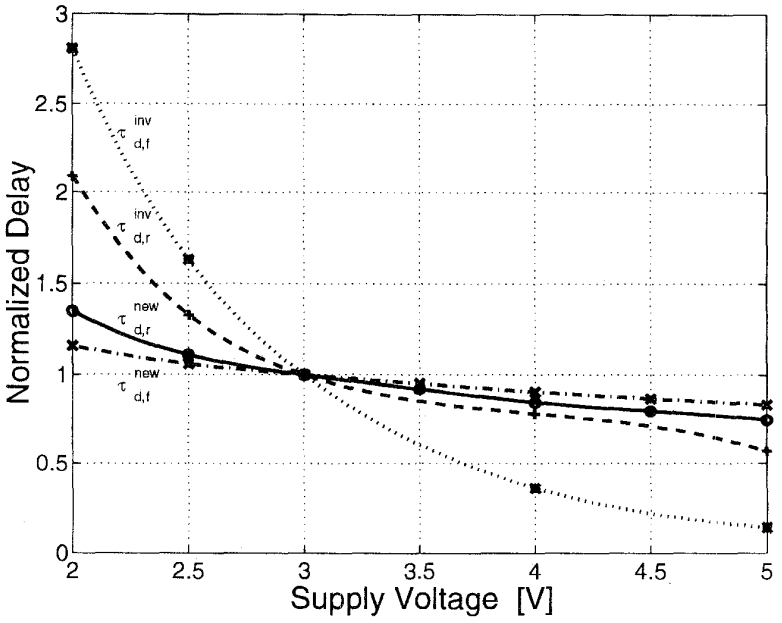


Fig. 10. Measured sensitivity to the supply voltage variation. The proposed delay element shows smaller sensitivity to V_{DD} in low voltage regime than inverter chain.

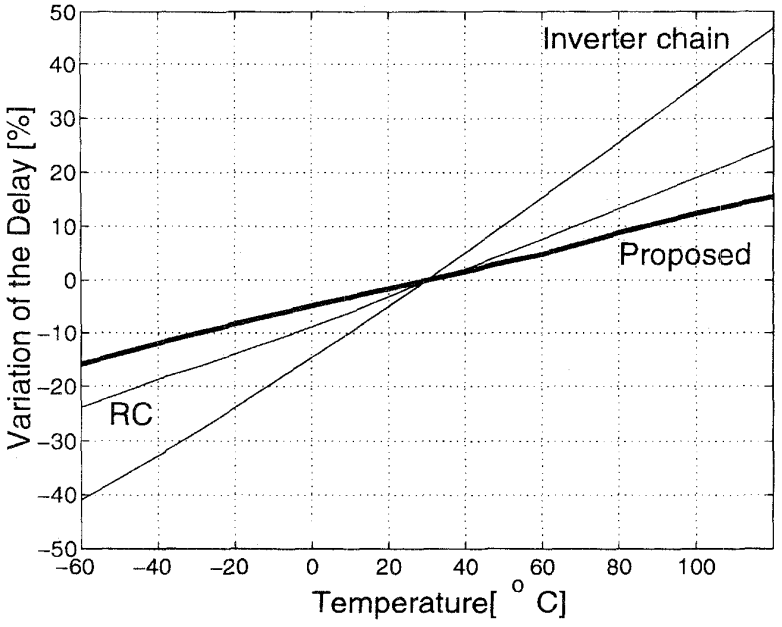


Fig. 11. Sensitivity to the temperature variation. Nominal $t_d \approx 3.3$ ns at 3 V, 30°C.

The proposed concept can be implemented with static triggering as in Fig. 6. Static triggering is simpler and has a wider control range as it doesn't require the internal delay element used in dynamic triggering, however, this is at the cost of the possible shunt current at the beginning of each switching.

There are two ways of controlling the delay value. When the required delay values are different at the rising edge and the falling edge of the input signal, two different current sources can be used as in Fig. 5. When the two delay values are identical, a current source is shared as in Fig. 6. These design methods can be used with both dynamic and static triggering methods.

The proposed delay element produces a sharp pulse from the positive feedback operation of the CMOS thyristor. However, this element cannot transfer a pulse whose duration is shorter

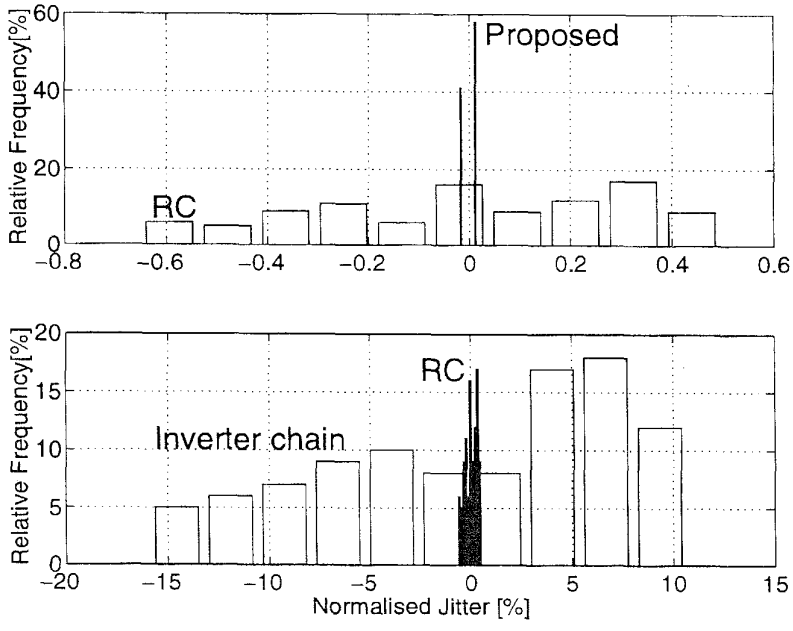
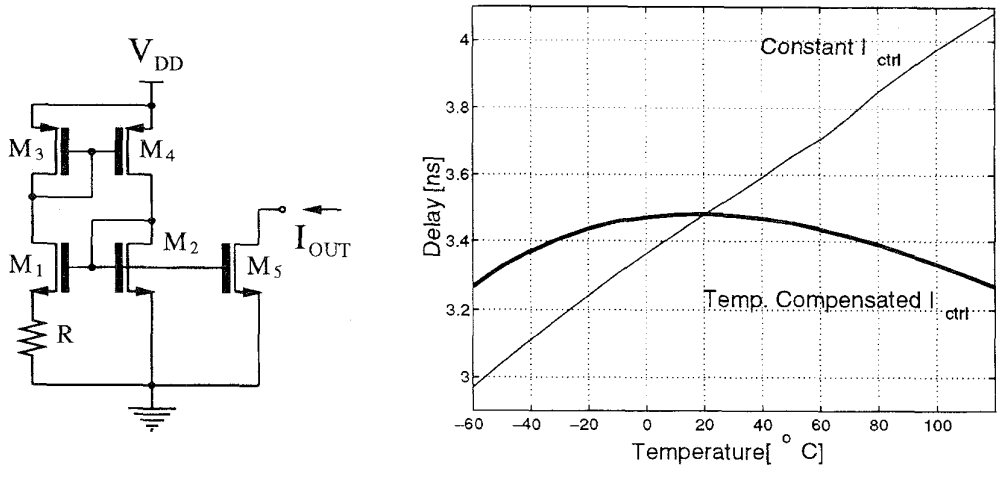


Fig. 12. Jitter histograms under power-line noise. Nominal $t_d \approx 3.2$ ns at 2 V, 27°C.



(a) (b)

Fig. 13. Current source with a designed temperature coefficient. (a) Circuit Schematic. (b) Delay Response at $V_{DD} = 3$ V.

than the delay time. This restriction on the operation also applies to the RC-delay elements.

IV. Results and Performance Analyses

In a real application, this delay element operates in an integrated circuit, that is, the circuit don't have any off-chip interface. But for the test circuit, the delay element is interfaced through a TTL-to-CMOS converter and a output driver. To compensate the delay of the input–output buffers, a dummy buffer is implemented in parallel with the proposed delay element. For the performance comparison, a CMOS inverter chain is also implemented. Static triggering scheme is used in the fabricated prototype. Fig. 7 is the microphotograph of the prototype.

Fig. 8 is the measured delay characteristics of the proposed delay element to the control current $I_{\rm ctrl}$. The obtained delay is inversely proportional to the control current $I_{\rm ctrl}$. By controlling $I_{\rm ctrl}$, 2.6 ns $\sim$ 76.3 ms of delay is obtained in 0.8 μm CMOS technology. Fig. 9 is the power consumption of the proposed delay element versus the control current $I_{\rm ctrl}$. The power consumption of the fabricated prototype could not be measured since the power current is negligible to that of input–output buffers.

The sensitivity to variation in supply voltage is compared to other delay elements in Fig. 10, and the sensitivity to temperature variation is shown in Fig. 11. The proposed delay element shows less sensitivity to supply voltage and temperature variations than inverter chains and RC delay elements.

The noise on the power line causes jitter in a delay element. Since the proposed delay element is less sensitive to the supply voltage than the other elements, it shows better jitter performance. Fig. 12 shows jitter histograms when the power-line noise is present. The noise is generated with a ring oscillator which operates in an asynchronous manner with the delay elements. The inductance of the bonding wire is 0.3 nH. The percent jitters of each delay element are 7.2% for inverter chain, 0.3% for RC delay element, and 0.015% for the proposed delay element. With the same amount of power-line noise, the proposed delay element shows smaller jitter than the other delay elements.

The temperature characteristics can be further enhanced by using a current source with a designed temperature coefficient as in Fig. 13. With a constant current source, proposed delay element shows a temperature coefficient of 1750 ppm/°C, while temperature coefficient of an RC-based delay element is 2500 ppm/°C, and that of an inverter chain is 4700 ppm/°C. Using the current source in Fig. 13, the temperature coefficient of the proposed delay element is 340 ppm/°C.

V. Conclusion

In this paper, a low-power CMOS delay element is proposed. The proposed delay element dissipates less power, and the delay value is less sensitive to the temperature and supply voltage variation than inverter chains or RC delay elements for a delay longer than 2.6 ns with a unit inverter load. The delay value can be varied with the control of the current source in a wide range and shows little jitter with a noisy power supply.

The power consumption of the proposed delay element is a decreasing function of the delay value. The proposed delay element is suitable for low-voltage operation from the inherent advantage of the CMOS thyristor and the fabricated prototype works down to 1 V supply while the technology is designed for 5 V applications.

Temperature compensation of the delay value is demonstrated by using a current source with a designed temperature coefficient.

This delay element will make DLL's and PLL's less sensitive to variation in the environment and provide a stable reference for the self-timed sub-blocks in a high speed VLSI.

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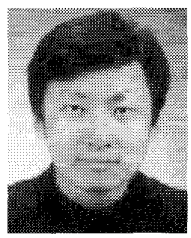

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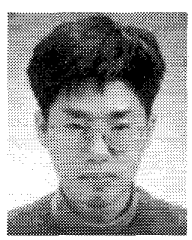

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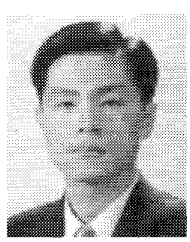

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