A High Resolution Frequency Multiplier for Clock Signal Generation

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Abstract— **This paper presents a high resolution frequency multiplier (FMUL) with the ability to multiply frequency with a programmable high multiplication factor, in the order of 10^2–10^4 and of the form N/M. It was designed for chip-sets that use a real time clock (32768 Hz) for power-save operation, and an additional high-frequency oscillator, in the range of 40–60 MHz, for regular operation. Using the FMUL spares the need for the additional high-frequency oscillator.**

The FMUL's frequency resolution is 100 ppm, and its jitter is less than 200 ps. The circuit is designed to work with 2–5 V supply voltage. It is implemented in a standard 0.8 μm N-well CMOS process, and its area is 0.48 mm^2.

I. Introduction

IN chips that use two separate clock systems, and where one is a low-frequency and the other a high-frequency [1], it may be desirable to have only one oscillator. One of the two ways is available to solve the problem.

a) Use only the high-frequency oscillator and generate the low-frequency by dividing it. In this configuration, a special high-frequency oscillator is used [2] to meet the power consumption specification at power save mode.
b) Use only the low-frequency oscillator and generate the high-frequency by multiplying it. Currently, most implementations of this configuration use a PLL [3], however, in most chips there is no demand to correlate the phase between the two frequencies. In addition, when a high multiplication factor is needed, the use of charge-pumped PLL [4] or similar implementation, requires special circuit techniques, and external components for the loop's filter.

The frequency multiplier (FMUL) presented here, is an alternative implementation of the latter configuration. It generates a high-frequency clock by means of digitally controlled current controlled oscillator (CCO). This approach does not use a phase-detector, and enables the control of the frequency by discrete steps. The FMUL consists of two modules, one is the CCO and the other is the digital logic that controls it. Its stability is guaranteed since it is a first order loop.

II. Digitally Controlled Frequency Multiplier

The high resolution of the frequency multiplier presented here is achieved by using 14 binary weighted current sources at the CCO that operates similarly to a 14-b DAC. In the FMUL, as opposed to a digital-to-analog converter (DAC), we do not have to guarantee linearity nor monotony of the high order bits, as will be shown later.

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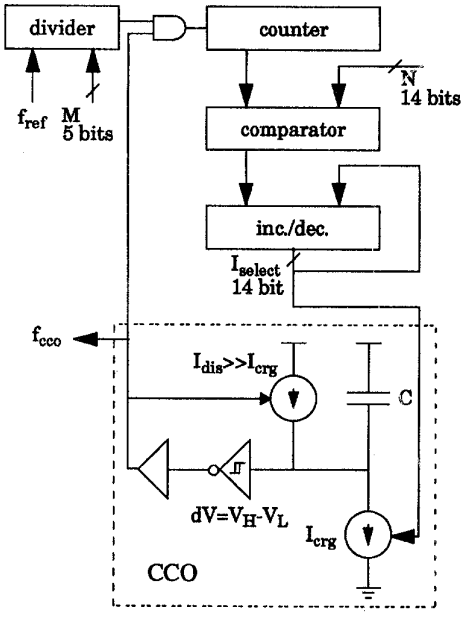

Fig. 1. FMUL's block diagram.

The frequency locking is done in two phases, the first is coarse tuning, and the second is fine tuning. During the coarse tuning, a binary search algorithm is implemented in a similar way to a successive approximation DAC, and during the fine tuning the frequency is incremented/decremented by small constant steps. The coarse tuning is done only once, during the chip's reset cycle. The FMUL's complete block diagram is presented in Fig. 1.

A. Current Controlled Oscillator

The CCO consists of a controlled charge current, a Schmidt trigger that defines the voltage window of the oscillations, and a constant discharge current that is enabled by the Schmidt's output.

The capacitor C is charged by current $I_{\rm crg}$, whose value is determined by the digital control logic. This continues until its voltage reaches V_L—the Schmidt's lower threshold. At this voltage the Schmidt changes state to "1," and the discharge current source is activated. The capacitor is discharged by the constant current $I_{\rm dis}$ until its voltage reaches the upper threshold of the Schmidt-V_H, $I_{\rm dis}$ is disabled, and the cycle repeats.

The oscillation frequency and its resolution are defined by (1) and (2), where S is the value of the charge current control bits—$I_{\rm select}$, i_0 is the single charge current step (LSB), dV is the Schmidt's voltage window, $T_{\rm cco}$ is the oscillation time

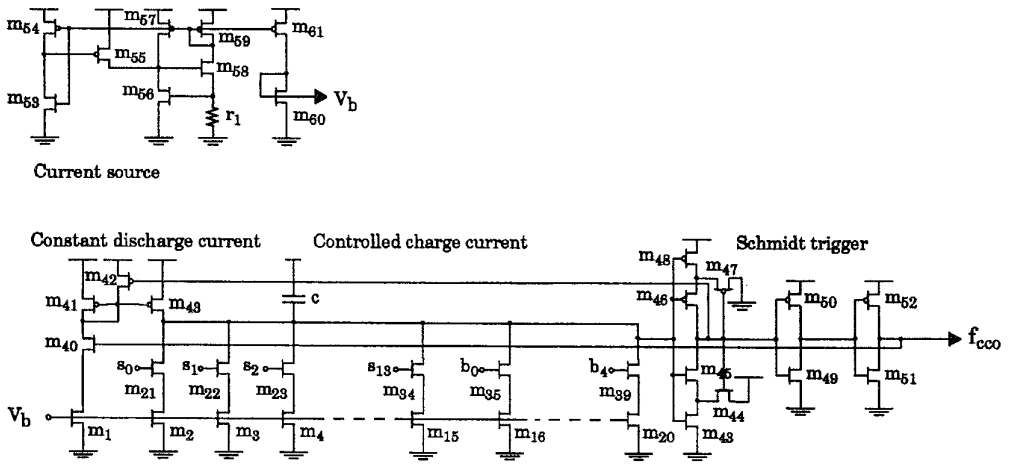

Fig. 2. Digitally controlled CCO.

cycle, and C is the value of the capacitor. It is assumed that the discharge time is negligible compared to the charge time

$$S \cdot i_0 = C \cdot (dV)/T_{\text{cco}} \tag{1}$$

$$(S+1) \cdot i_0 = C \cdot (dV)/(T_{\text{cco}} - dT). \tag{2}$$

The detailed CCO's circuit is shown in Fig. 2. The V_T-referenced current source [5], transistors m_{53}–m_{61}, is used as the basic current for mirroring and producing the $2^n * i_0$ binary weighted currents.

The constant discharging current source is implemented by transistors m_1 and m_{40}–m_{43}. Discharging is enabled by the signal at the gate of m_{40}. We added m_{42} for two reasons, the first is for faster shut-off of the discharging current, and the second is to prevent a steady-state where the discharge current equal the charge current, and no oscillations would occur. For the same reason, it is vital to enable the discharging only after the Schmidt has completed its turnover. Transistors m_2–m_{15} are the binary weighted charge current mirrors, and m_{21}–m_{34} are their switches that are controlled by I_{select}.

The current mirroring accuracy is guaranteed only up to 8 b by the process used [6] (when using adequate layout techniques). This may cause "holes" in the f-I curve of the CCO which would degrade the FMUL's frequency resolution. To solve this problem we have implemented a controlled bias current in parallel to the controlled charge current-transistors m_{16}–m_{20}.

Whenever more than 7 b are simultaneously changed from "1" to "0" in the I_{select}, during fine tuning (e.g., when the previous I_{select} was S = '01110011111111' and the present one is S = '01110100000000'), then the bias charging current will be incremented by one "bias step" which is $-8 * i_0$ (this is in addition to the "normal step" of $-1 * i_0$ by m_2–m_{15}). This technique is a very simple method to move away from the possible "holes" in the f-I curve of the CCO, and impose the value of the control word—I_{select}, to be lower than the multiple simultaneous bits change value (since I_{crg} is now $(S+8) * i_0$, I_{select} will change to $S_{\text{new}} = S_{\text{old}} - 8$, '01110011110111' in our example). Transistors m_{16}–m_{20} are the binary weighted bias mirrors, and m_{35}–m_{39} are their switches, respectively.

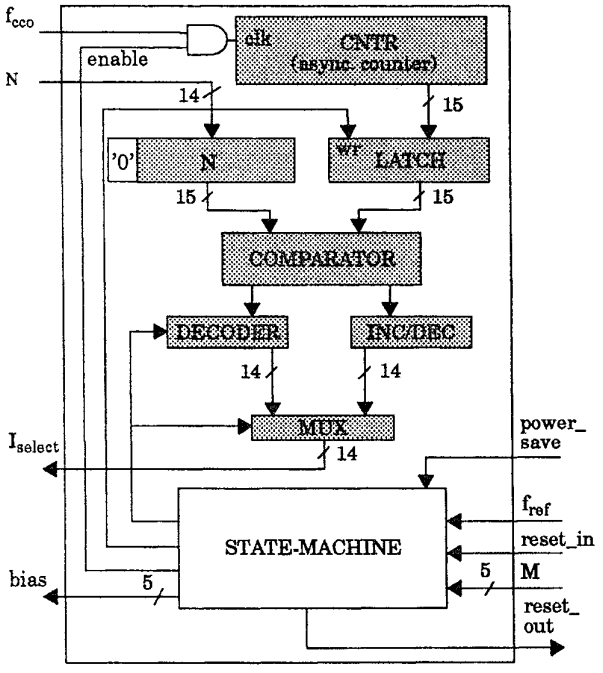

Fig. 3. Digital control of the CCO.

The Schmidt trigger is composed of transistors m_{43}–m_{48}. The two inverters at its output, m_{49}–m_{52}, are used to delay the discharging current turn-on.

B. Digital Control Logic

The CCO's digital control logic is shown in Fig. 3. It consists of the following blocks.

- *Asynchronous counter* (CNTR)—counts the number of f_{cco} cycles in a given time frame, that is defined by M cycles of the reference clock f_{ref}. The goal is to reach the relation $f_{\text{cco}} = (N/M) f_{\text{ref}}$.

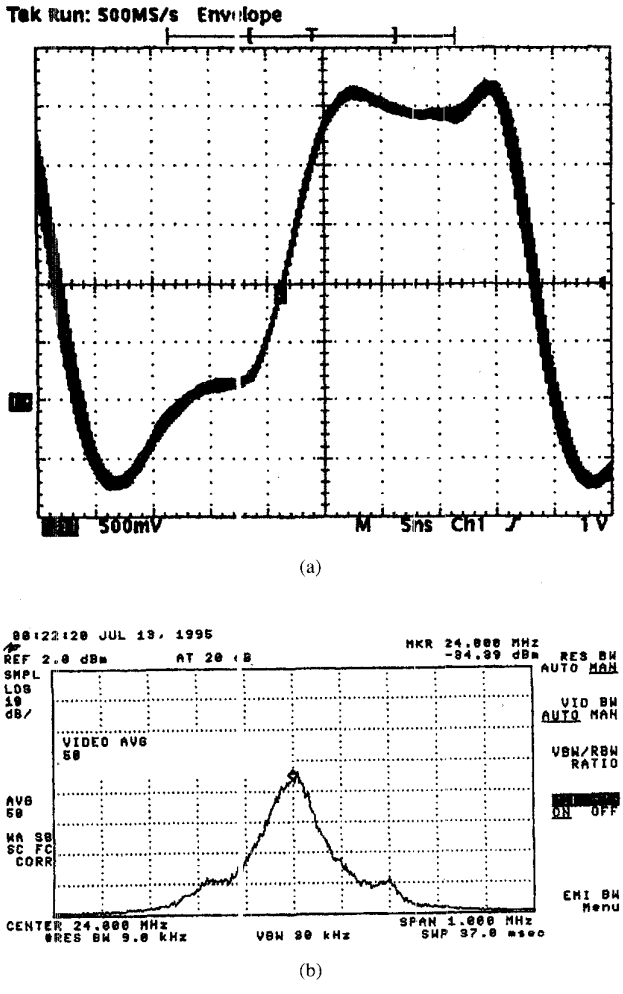

Fig. 4. (a) Infinite samples of the output clock. (b) Spectrum of the output clock.

TABLE I
JITTER AS A FUNCTION OF V_{cc}

Supply voltage	Jitter
2.5v	190ps
3.0v	180ps
3.5v	170ps
4.0v	150ps
4.5v	120ps
5.0v	100ps

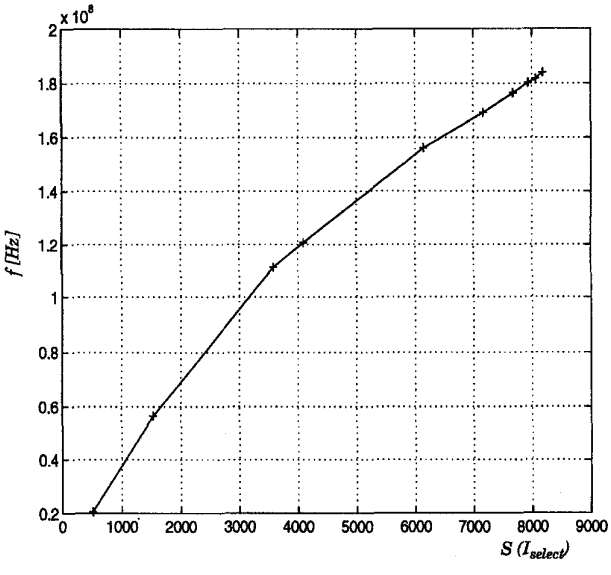

Fig. 5. f-I curve of the CCO.

- *15 b comparator*—compares the asynchronous counter's output to N.
- *14 b incrementor/decrementor*—increments and decrements the value of I_{select}, by one step, during fine tuning.
- *Decoder*—defines the value of the I_{select} bits during the coarse tuning.
- *Synchronous finite-state-machine* (FSM)—controls the functions of all blocks that were mentioned above according to the convergence algorithm.

As was mentioned previously, the convergence algorithm has two phases, coarse and fine. After **reset_in**, the FMUL enters the coarse tuning phase, I_{select} is imposed to $S =$ '10000000000000' which is the FMUL's center frequency, and the value of CNTR after M reference cycles is compared to N. The decoder determines accordingly, whether the next state will be $S =$ '$11X$' or $S =$ '$01X$' (binary search algorithm). This is repeated for all I_{select} bits (S_{13} to S_0).

At the end of the coarse tuning phase, the end-of-conversion is indicated by the **reset_out** signal. This indication means that the rest of the chip may use the f_{cco} clock.

From this point, the FMUL enters the fine tuning phase, during which the value of I_{select} will be incremented/decremented by single count, every M reference cycles, according to the comparison with N. The special bias control bits that are used to move the operating point away from the possible "holes" in the f-I curve of the CCO are activated only during the fine tuning phase.

Recovering from power-save mode to regular operation mode is performed immediately, after **power_save** signal is disabled, due to the fact that the CCO is controlled digitally and I_{select} keeps its value during power-save.

III. RESULTS

The FMUL was used to generate a clock at the frequency of 48 MHz, with a reference clock of 32 768 Hz. The demand was that the 48 MHz clock will have 50% duty-cycle, and thus we generated f_{cco} at 96 MHz, $N/M = 8789/3$, and divided it by two.

The circuit's current consumption for $f_{\text{cco}} = 96$ MHz @ $V_{\text{cc}} = 5$ V is 5.6 mA.

Fig. 4 shows the 24 MHz output clock (divided 48 MHz). Fig. 4(a) shows infinite scope samples one on top of the other

(jitter is less than 200 ps). The frequency as measured with a spectrum analyzer is shown in Fig. 4(b), the 3 dB width is 6 kHz, implying a standard deviation of 106 ppm. Table I presents jitter results as a function of the supply voltage. Jitter is restricted to less than 200 ps over all the dynamic range of the supply voltage. As can be seen, the jitter is lower for higher supply voltages. This is explained by a combination of several facts: i) the reference clock f_{ref} is more stable at higher supply voltage, ii) the frequency correction step is larger for lower supply voltage since i_0/dV is higher, iii) the Schmidt is more susceptible to substrate coupling noises at lower supply voltage. Frequency resolution remains in the 100 ppm range for all supply voltages since the frequency control is done digitally (N/M is fixed) and the correction steps are kept small enough.

Fig. 5 is the CCO's f-I curve, it shows that the FMUL is capable of working with f_{cco} up to 180 MHz.

The FMUL's simplicity, small area, and its low sensitivity to process variations and supply voltage make it very attractive for use in every chip that requires more than one oscillator. It is especially useful for low-power systems due to its fast recovery time from power-save mode.

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