A Wide Dynamic Range Continuously Adjustable CMOS Current Mirror

A. K. Gupta, J. W. Haslett, and F. N. Trofimenkoff

Abstract—**A novel circuit realization of a CMOS current mirror with wide input dynamic range and continuously adjustable gain is presented. The proposed current mirror is linear with respect to signal current in the strong inversion as well as in the subthreshold region of MOSFET operation. The gain is controlled by the same control signal in both regions. The circuit is analyzed using a numerical unified MOSFET model which covers both operating regions. The implemented current mirror is adjustable over more than eight decades of signal current.**

I. Introduction

CURRENT mirrors with continuously adjustable gain [1]–[8] are used in applications such as auto-zeroed amplifiers, tunable analog filters, self calibrating sensor arrays, etc. In some cases, the signals are unipolar but have a logarithmic variation, for example in optical sensor systems [9]. In such applications, a current mirror which is linear and adjustable over four or five decades of signal current, say 100 pA–10 μA, is needed.

Several bipolar junction transistor (BJT) adjustable current mirrors (ACM) based on the *log-antilog* or *translinear* property of the BJT have been developed [1]–[4]. The translinear property of the BJT makes it possible to achieve an adjustable current mirror in a convenient fashion. In contrast to BJT ACM's, it is difficult to construct a MOSFET ACM because MOSFET current versus voltage characteristics vary with channel current. In the strong inversion region, which is the most useful region of operation, the MOSFET has a square law characteristic which is not as convenient as the translinear characteristic of the BJT for producing an ACM. MOS current gain cells with variable gain and constant bandwidth have been described [5] using source injected control signals to achieve linear controlled gain over a signal current range of several hundred microamperes. Attempts have also been made to develop a CMOS adjustable current mirror by degenerating the source terminal of the mirror transistor using a variable active resistor [6], [7], where a single MOSFET biased in the triode region was used as the variable active resistor. There are two main drawbacks to this type of current mirror: a) it has very poor linearity in the strong inversion region, and b) it cannot be controlled in the subthreshold region because a small signal current does not cause any significant voltage drop across the variable resistor. In the subthreshold region, the MOSFET has translinear characteristics similar to those of a BJT and therefore topologies exploiting the translinear property of the device can be used [1]. Large chip area and low speed are the main disadvantages of using the MOSFET current mirror only in the subthreshold region. When this type of current mirror is operated at high signal currents such that the current mirror MOSFET's enter the strong inversion region, a significant amount of nonlinearity is introduced. A similar type of current mirror [8] also faces the same problem.

In this paper, a unique topology [9] which achieves linear characteristics for the devices which have either translinear or square-law characteristics is presented. The current gain in both subthreshold and strong inversion regions is controlled by the same control signal and there is no switching involved. However, the current gains for the same control signal are not exactly the same for the two operating regions, and the current gains are not constant in the transition region.

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II. CMOS Adjustable Current Mirror

Fig. 1 shows the circuit realization of the proposed adjustable current mirror in which MOSFET's M_1 and M_2 carry duplicated input currents. MOSFET's M_4 and M_5 are used as buffer transistors. The gate-to-source voltages of MOSFET's M_1 and M_2, V_{GS1} and V_{GS2}, are set by the drain currents of M_1 and M_2. The potentiometer generates a gate voltage, V_{GS3}, for MOSFET M_3 which is a weighted sum of V_{GS1} and V_{GS2}. The ratios of $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ are chosen to be $M:1:M$ where M is the maximum achievable gain. For a moderate value of M, say 2–10, the voltage difference of V_{GS1} and V_{GS2} will be relatively small and therefore a variable active resistor with a small linear range would be adequate. For extreme settings of the potentiometer, the gate of M_3 will be either connected to the gate of M_1 or M_2 and the resulting circuit will be similar to a scaled current mirror. Any arbitrary setting of the potentiometer is expected to provide a current gain between 1 and M.

The choice of transistor geometries was driven by the fact that large devices reduce random gain variations in the subthreshold region when small random changes occur in V_T. Long channel devices were used in place of cascode circuits to reduce output conductance while retaining maximum dynamic range.

III. Analysis

Let I_D be the large signal channel current in a MOSFET and V_{DS}, V_{GS} be the large signal drain-source and gate-source potentials, respectively. If channel length modulation is ignored, the drain current in the subthreshold region can be

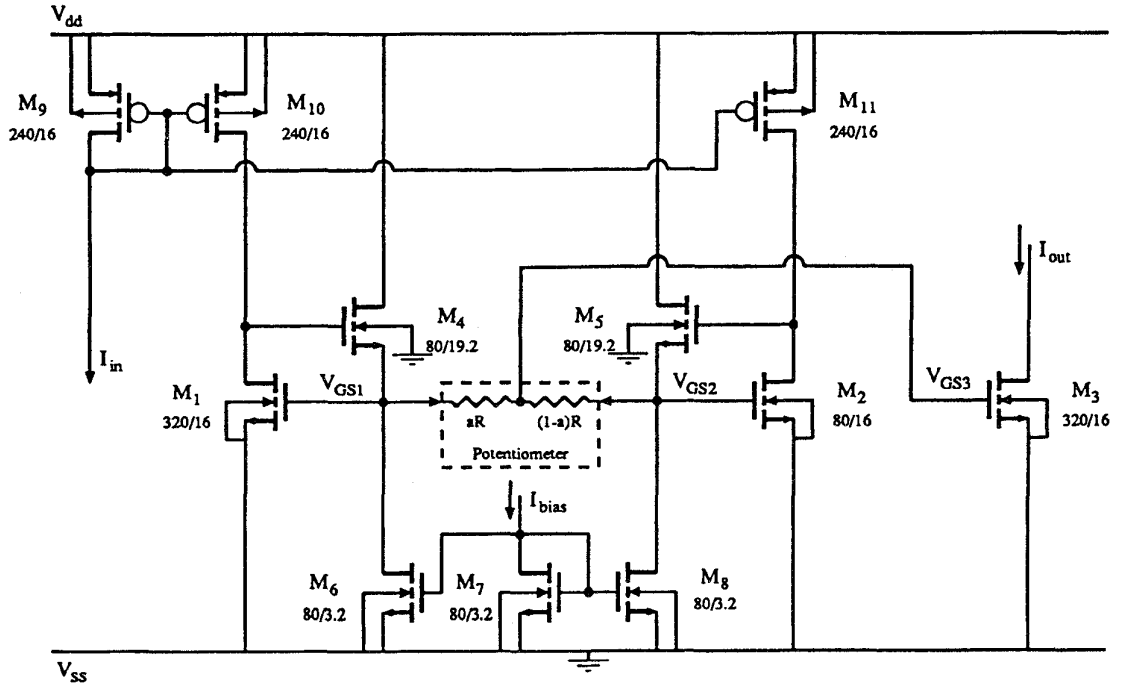

Fig. 1. CMOS adjustable current mirror.

written as [10]

$$I_D = K_x \frac{W}{L} e^{V_{GS}/\eta V_T}(1 - e^{-V_{DS}/V_T}) \tag{1}$$

where K_x depends on the process parameters, $V_T = kT/q$ and $\eta \approx 1.5$. For $V_{DS} \gg V_T$, I_D can be approximated by

$$I_D = K_x \frac{W}{L} e^{V_{GS}/\eta V_T}. \tag{2}$$

If channel length modulation is ignored, the drain current in the strong inversion saturation region can be written as

$$I_D = K_y \frac{W}{L}(V_{GS} - V_{TO})^2 \tag{3}$$

where K_y depends on the process parameters and V_{TO} is the threshold voltage of the MOSFET.

At low signal current levels, M_1, M_2, and M_3 (see Fig. 1) will be biased in the subthreshold region. In this case, V_{GS1} and V_{GS2} can be written as

$$V_{GS1} = \eta V_T \ln\left(\frac{I_{\text{in}}}{K_x(W/L)_1}\right) \tag{4}$$

and

$$V_{GS2} = \eta V_T \ln\left(\frac{I_{\text{in}}}{K_x(W/L)_2}\right). \tag{5}$$

V_{GS3}, which is generated by the potentiometer, will be given by

$$V_{GS3} = (1-a)V_{GS1} + aV_{GS2} \tag{6}$$

where a is the gain setting parameter of the potentiometer. Using (2), (4), (5), and (6), the current gain at low current levels can be written as

$$G_{\text{sub}} = \frac{I_{\text{out}}}{I_{\text{in}}} = M^a. \tag{7}$$

At high signal current levels, M_1, M_2, and M_3 will be biased in the strong inversion region. In this case, V_{GS1} and V_{GS2} can be written as

$$V_{GS1} = V_{TO} + \sqrt{\frac{I_{\text{in}}}{K_y(W/L)_1}} \tag{8}$$

and

$$V_{GS2} = V_{TO} + \sqrt{\frac{I_{\text{in}}}{K_y(W/L)_2}}. \tag{9}$$

Using (3), (6), (8), and (9), the current gain in the strong inversion region will be given by

$$G_{\text{str}} = \frac{I_{\text{out}}}{I_{\text{in}}} = M\left(a + \frac{1-a}{\sqrt{M}}\right)^2. \tag{10}$$

The current gain in both regions is, to first order, independent of the signal current which indicates that the circuit will be linear in both regions. Gain variation from G_{sub} to G_{str} is expected in the transition region. A MOSFET model developed by Barron [11] is used to predict the circuit behavior in the transition region. For a MOSFET with source and bulk connected to ground, the source current is given by

$$I_S = \frac{qWD_n n_i L_D}{L} \int_0^{V_{DS}/V_T} \int_0^{U_s} \frac{e^{U-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi \tag{11}$$

where

D_n electron diffusion coefficient;

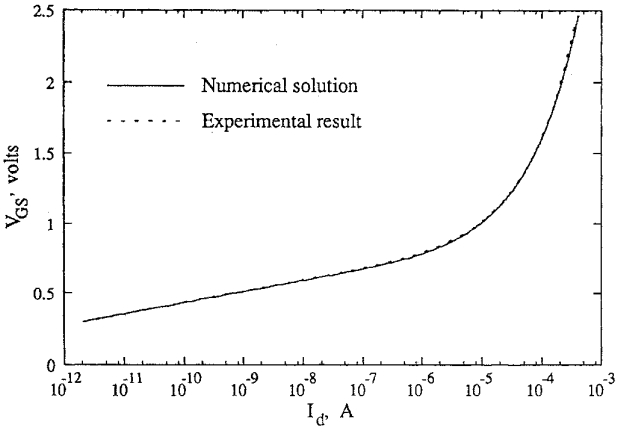

Fig. 2. MOSFET characteristics.

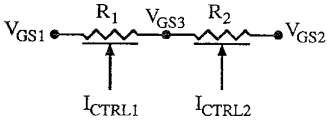

Fig. 3. Schematic diagram of the electronically tunable potentiometer.

n_i	intrinsic carrier density;
L_D	$\sqrt{kT\epsilon_s/2q^2n_i}$;
ϵ_s	permittivity of Si;
N_a	acceptor density;
U	normalized potential;
U_s	normalized surface potential;
U_F	$\sinh^{-1}(N_a/2n_i)$;
ξ	normalized electron quasi-Fermi potential;
$F(U,U_F,\xi)$	$(e^{U_F-U} + e^{U-U_F-\xi} + (U-1)e^{U_F} - (U+e^{-\xi})e^{-U_F})^{1/2}$.

In the moderate subthreshold region, the generation currents in the drain and channel depletion region will be much smaller than the channel current and therefore I_D can be approximated by I_S. The lower limit of the first integral can be changed to two to save computation time. The resulting error will be small because the value of the integral between zero to two is relatively small [11] and I_D can be written as

$$I_D = \frac{qWD_n n_i L_D}{L} \int_0^{V_{DS}/V_T} \int_2^{U_s} \frac{e^{U-U_F-\xi}}{F(U,U_F,\xi)}\, dU\, d\xi. \tag{12}$$

The surface potential, U_s, is calculated from the implicit equation

$$\frac{q(V_{GS}+\psi_{\text{msco}}+\psi_Q)}{kT} = \frac{\epsilon_s}{C_{\text{ox}}L_D}F(U_s,U_F,\xi)+U_s \tag{13}$$

where

ψ_{msco}	metal semiconductor work function;
ψ_Q	modification of the metal semiconductor work function due to bound charges in the oxide;
C_{ox}	oxide capacitance per unit area.

Approximations such as $2U_f > U_s$ cannot be used for the unified model so that a closed form analytical solution for I_D as a function of V_{DS} and V_{GS} cannot be found. To analyze the circuit, I_D is obtained numerically for various V_{GS} ignoring channel length modulation and using $V_{DS} = 1$ V. The I_D versus V_{GS} characteristics of a diode-connected polysilicon gate MOSFET were measured to verify the unified model presented in (12). Process parameters were manipulated in order to compare the measured and the modeled characteristics as shown in Fig. 2. Matching of analytical and measured characteristics was found to be very good. The modeled I_D versus V_{GS} characteristics were used in conjunction with (6) to predict the gain of the current mirror.

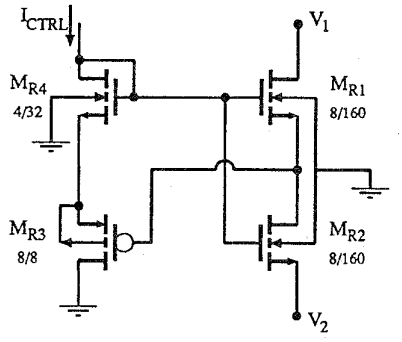

Fig. 4. Circuit diagram of the variable active resistor.

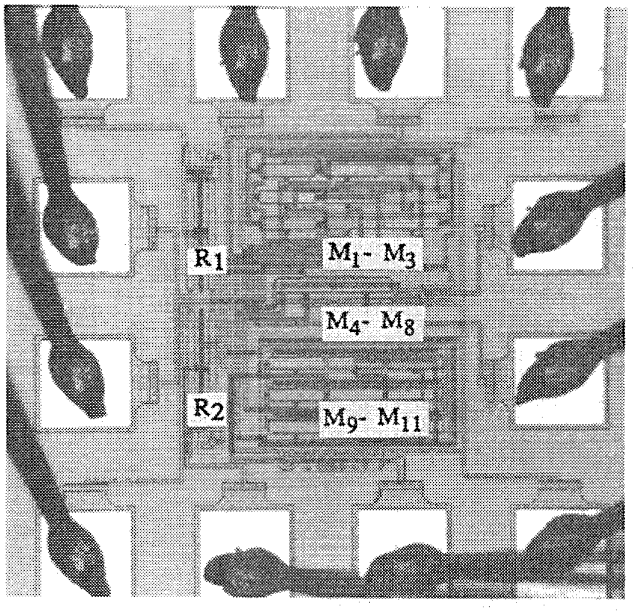

Fig. 5. Photomicrograph of the wide dynamic range CMOS ACM IC.

IV. Electronically Tunable Potentiometer

For electronic control of the ACM, an electronically tunable potentiometer (ETP) can be used. Two series connected variable active resistors (VAR's) can be used to realize an ETP as shown in Fig. 3.

The VAR's to be used in this particular application should have the following properties.

Biasing Robustness: The integrated circuit should not go into improper biasing of the source-body junction of MOSFET's which can trigger latchup of the chip. Some circuits

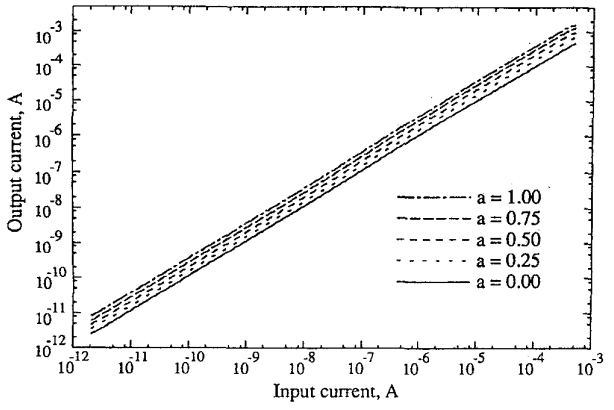

Fig. 6. Measured characteristics of CMOS current mirror.

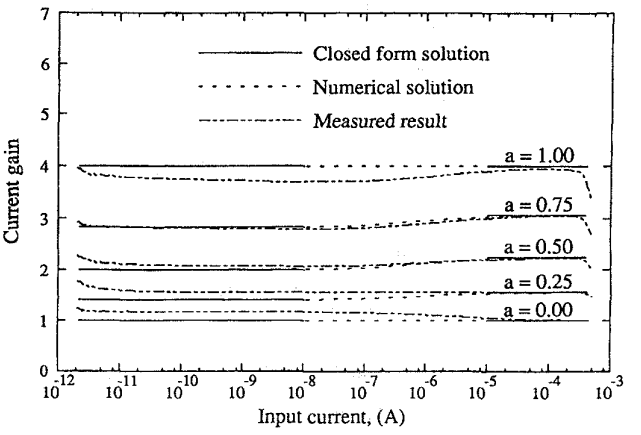

Fig. 7. Current gain of CMOS current mirror.

which involve separate biasing of the body and the gate of the resistive MOSFET may not be robust in this regard.

Large Common-Mode Voltage Range: The control circuit for the active resistor should be such that the circuit will be properly biased for large common-mode terminal voltages extending to one of the power supply voltages.

Common-Mode Voltage Independence: The resistive value of a variable resistor should not depend on the common-mode voltage of the resistor terminals, otherwise it will introduce nonlinearity. In MOSFET resistors, the *body effect* is the main reason for this distortion.

No Offset Current/Voltage: The variable resistor should not have any offset current or voltage, otherwise an exact weighted sum cannot be achieved. This constraint is not generally fulfilled in circuits which rely on the use of matched transistors.

A series-type VAR developed by VanPeteghem and Rice [12] was modified to increase the common-mode voltage range extending to the negative power supply at the expense of slight common-mode voltage dependence of the resistor. There is a significant reduction in the circuit complexity. Moreover, only one control signal current source is required instead of two matched complementary control signal current sources. The circuit diagram of the modified VAR is shown in Fig. 4. The current in the VAR can approximately be given by [9]

$$I_{1-2} = \frac{K_{nr}}{2}(V_1 - V_2)V_c\sqrt{1 - \frac{(1+\delta)^2(V_1 - V_2)^2}{4V_c^2}} \quad (14)$$

where

K_{nr}	$K_{n1} = K_{n2}$;
V_c	$V_{CTRL_0} - V_{T_n}$;
V_{CTRL_0}	$(-V_{TO_p} + \sqrt{2I_{CTRL}/K_{p3}})(1+\delta) + V_{T_n} + \sqrt{2(1+\delta)I_{CTRL}/K_{n4}}$;
K_n	$\mu_n C_{\text{ox}} W/L$;
K_p	$\mu_p C_{\text{ox}} W/L$;
δ	$\gamma/(2\sqrt{\phi_B - V_B})$;
γ	$(1/C_{\text{ox}})\sqrt{2qN_A\epsilon_s}$;
V_{T_n}	$V_{TO_n} - \gamma\sqrt{\phi_B} + \gamma\sqrt{\phi_B - V_B}$;
ϕ_B	surface inversion potential;
V_{TO_n}, V_{TO_p}	zero V_{BS} threshold voltages of the NMOS and PMOS transistors.

In an n-well process, the p-substrate is the body of all the NMOS transistors, which should be connected to the most negative power supply, thus $V_B = 0$ V.

The I/V characteristics are linear for $V_c^2 \gg (V_1 - V_2)^2$. This variable resistor fulfills all the desired characteristics sufficiently well.

V. Integrated Circuit Implementation

The circuit was implemented in a commercial 1.2 μm n-well CMOS process made available to us through the Canadian Microelectronics Corporation. The photomicrograph of the integrated circuit is shown in Fig. 5. The die area of the IC excluding bonding pads is approximately 400 μm $\times$ 480 μm. A common centroid technique was used to reduce the threshold voltage variation. The maximum achievable gain, M, was chosen to be four. The ETP was fabricated on the same chip, but the internal connections were taken out to package pins so that the current mirror could also be tested with an external potentiometer.

VI. Comparison of Analytical and Test Results

The input current was varied from 2 pA to 500 μA to cover the desired range of signals. The circuit was tested using the external potentiometer for $a = 0.00$, 0.25, 0.50, 0.75, and 1.00. The measured input and output currents are shown in Fig. 6. It is evident that the current mirror is adjustable over the entire range. In Fig. 7, the gains of the current mirrors are plotted. The closed form solution [(7) and (10)], the numerical solution, and the measured results are in reasonably good agreement. The deviation of the measured gain from the analytical gain was due to the variation in the threshold voltages of MOSFET's M_1, M_2, and M_3. Random threshold voltage variation could be traded off against speed of the current mirror by choosing large device geometries. Five chips were tested to measure the gain variation among chips at $a = 0.5$. The % normalized variation defined as $100 \times (\max(\text{gain}) - \min(\text{gain}))/\text{average}(\text{gain})$ of chips was less than 4% over more than seven decades of signal current (see Fig. 8).

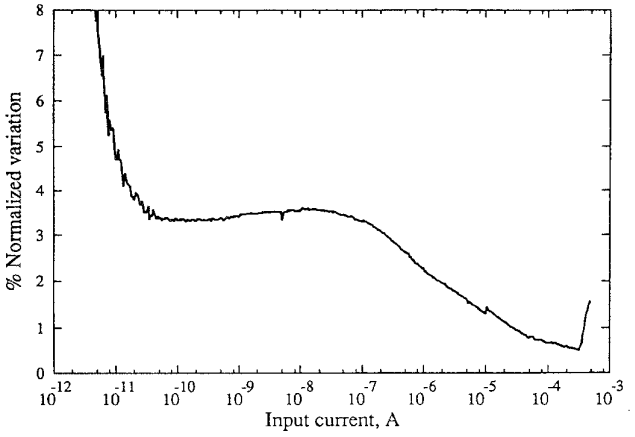

Fig. 8. Normalized gain variation among different IC's at $a = 0.5$.

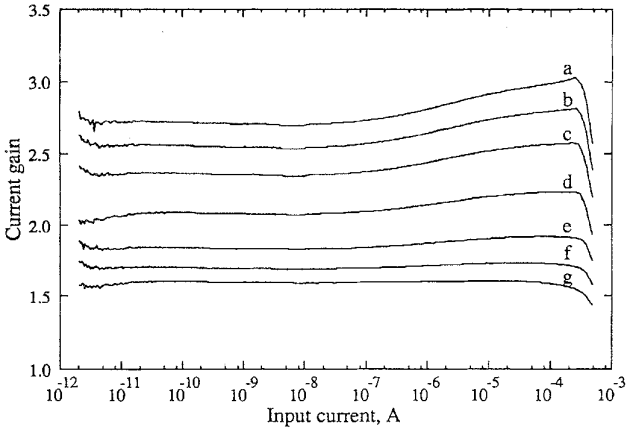

Fig. 9. Current gain of the CMOS current mirror using the integrated ETP. Curves a–g correspond to $(I_{CTRL1}, I_{CTRL2}) = (10^{-9}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-8}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-7}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-7}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-8}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-9}\,\mathrm{A})$, respectively.

The current mirror was also tested using an ETP integrated on the same chip. Different gain parameters were set by varying I_{CTRL1} and I_{CTRL2}. Fig. 9 shows current gains at $(I_{CTRL1}, I_{CTRL2}) = (10^{-9}\,\mathrm{A}, 10^{-6}\,\mathrm{A}), (10^{-8}\,\mathrm{A}, 10^{-6}\,\mathrm{A}), (10^{-7}\,\mathrm{A}, 10^{-6}\,\mathrm{A}), (10^{-6}\,\mathrm{A}, 10^{-6}\,\mathrm{A}), (10^{-6}\,\mathrm{A}, 10^{-7}\,\mathrm{A}), (10^{-6}\,\mathrm{A}, 10^{-8}\,\mathrm{A}), (10^{-6}\,\mathrm{A}, 10^{-9}\,\mathrm{A})$. The % normalized gain error defined as $100 \times (\text{gain} - \text{gain}\,(1\,\mu\mathrm{A}))/\text{gain}\,(1\,\mu\mathrm{A})$ is plotted in Fig. 10. The nonuniformity in the curves is due to switching of signal ranges in the measuring instrument. The current mirror is linear within ±4% for a gain variation of 1.62–2.81 over more than six decades of signal current.

VII. Gain Range and Gain Variation

The proposed circuit can be designed for a gain range (1 to M) which is set by the device geometries. An electronically controlled potentiometer will have a swing in gain parameter, a, less than one, and this would result in a decrease in the current gain range.

The variation between the current gain of the current mirror in the subthreshold region and the strong inversion region depends on the gain parameter a and the maximum current

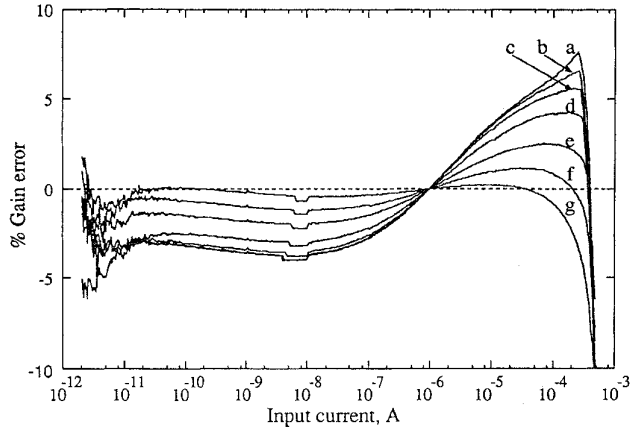

Fig. 10. Percent normalized gain error of the CMOS ACM using the ETP. Curves a–g correspond to $(I_{CTRL1}, I_{CTRL2}) = (10^{-9}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-8}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-7}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-6}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-7}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-8}\,\mathrm{A})$, $(10^{-6}\,\mathrm{A}, 10^{-9}\,\mathrm{A})$, respectively.

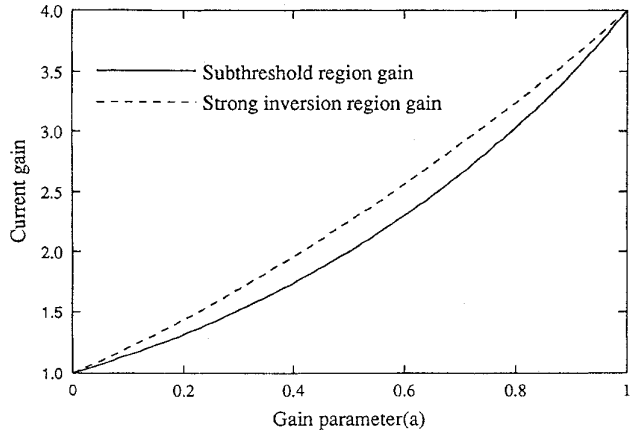

Fig. 11. Theoretical current gain as a function of gain parameter (a), for $M = 4$.

gain M. The variation in the current gain is maximum near $a = 0.5$ and the variation increases with increase in M. Fig. 11 shows the current gains G_{sub} (7) and G_{str} (10) for $M = 4$ and varying a. Fig. 12 shows the current gains G_{sub} and G_{str} for $a = 0.5$ and varying M. There is obviously a tradeoff between the gain variation and the gain range.

VIII. Bandwidth Characteristics

The bandwidth characteristics of the circuit are of interest, and although complicated by the wide range of bias and signal current levels involved, some observations can be made as follows.

At high signal current levels, the bandwidth is determined by the pole formed by the resistive poentiometer and the gate-source capacitance of M_3. At low signal current levels, the bandwidth is determined by the poles formed by the small-signal transconductances of (M_1, M_4) and (M_2, M_5) and the associated gate-source capacitances.

To maximize the circuit bandwidth, low valued resistors (VAR's) should be used. However, when there is a relatively

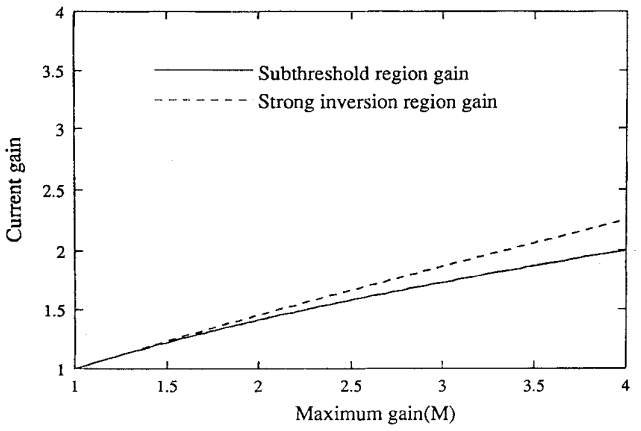

Fig. 12. Theoretical current gain as a function of maximum gain (M), for $a = 0.5$.

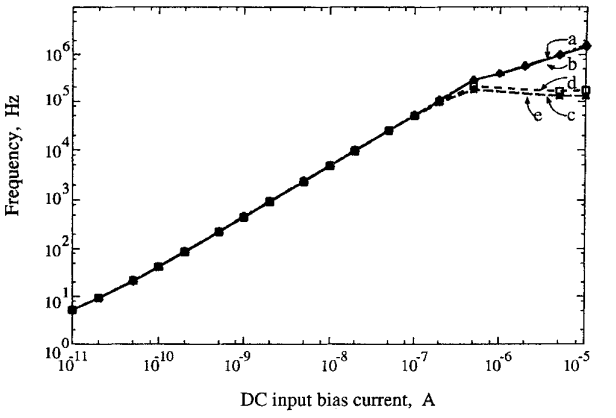

Fig. 13. Bandwidth of the CMOS ACM as a function of dc input current. Curve a corresponds to the gate of M_3 shorted to the gate of M_2. Curve b corresponds to the gate of M_3 shorted to the gate of M_1. Curves c, d, and e correspond to $(I_{ctrl1}, I_{ctrl2}) = (10^{-8}\,\text{A}, 10^{-6}\,\text{A}), (10^{-6}\,\text{A}, 10^{-6}\,\text{A})$, and $(10^{-6}\,\text{A}, 10^{-8}\,\text{A})$, respectively.

large voltage difference between V_{GS1} and V_{GS2}, a larger current will flow through the VAR's. To bias M_4 and M_5 properly, the biasing currents in M_6 and M_8 must be larger than the currents in the VAR's. These requirements result in larger power consumption when low valued VAR's are used, and a tradeoff between bandwidth and power consumption must be made.

In order to develop a low power circuit in this work, high valued VAR's were used. The SPICE simulated bandwidth characteristics of the circuit are shown in Fig. 13 for a wide range of currents and with gain setting as a parameter. In the low current range, the 3 dB bandwidth is roughly proportional to current and is independent of gain setting, and at higher current levels, it becomes less sensitive to current when VAR's are used to vary the gain as indicated by curves c, d, and e. Curves a and b correspond to the situation where the gate of M_3 is shorted to either the gate of M_2 or M_1, respectively. In the latter case, the resistance of the VAR's does not contribute to the VAR-C_{GS3} pole, resulting in a bandwidth that increases somewhat in the high current region with increasing signal current.

IX. Conclusion

A circuit realization of a novel CMOS adjustable current mirror which is linear with signal current in both operating regions of the MOSFET, i.e., subthreshold and strong inversion, has been presented. The transition between the two regions is smooth and does not require any switching. The implemented current mirror was controllable over more than eight decades of signal current. The ACM with an electronically tunable potentiometer exhibited a linear input–output relationship to within ±4% for a gain variation of 1.62 to 2.81 over more than six decades of signal current.

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