A Rail-to-Rail Ping-Pong Op-Amp

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Abstract—**A rail-to-rail ping-pong op-amp achieves offset cancellation and $1/f$ noise reduction without folding of the input spectrum. The clocking scheme minimizes the clock feedthrough and the residual offset due to charge injection. With a clock frequency of 100 KHz, the residual offset is less than 100 μV, and the input referred noise is about 225 nV/Hz$^{1/2}$. The rail-to-rail distortion at 1 kHz is lower than −71 dB. The total silicon area is 610 × 420 μm^2, and the circuit dissipates 1.5 mW from a single 5 V supply.**

I. Introduction

OFFSET cancellation and $1/f$ noise reduction in CMOS op-amps can be achieved with chopper amplifiers or auto-zero techniques [1]. A ping-pong architecture [2] can achieve 100% duty cycle and continuous time operation. The main advantage of this approach is that the input spectrum is not folded by sampling or modulation, therefore, the clock frequency can be lower than the usable bandwidth.

On the other hand, the rail-to-rail operation requires complementary input pairs. The difference in random offset voltages of these input pairs translates into a global offset with nonlinear variation over the common mode input range. This nonlinear offset is one of the main causes of large signal distortion in rail-to-rail circuits.

This paper presents a ping-pong design with rail-to-rail capability. Very low distortion is obtained by separately auto-zeroing semicircuits that have complementary input pairs.

II. Circuit Description

The block diagram of the circuit is shown in Fig. 1. A four phase clock controls the CMOS switches according to the timing diagram of Fig. 2. The nonoverlapping phases Φ_1 and Φ_2 represent the auto-zero and the amplify phase of transconductance amplifiers A_1 and A_2 with complementary input pairs. During Φ_1, the inputs are shorted together to a common input reference voltage $V_{ref_{in}}$, and the feedback loops for offset cancellation are closed. The offsets are stored on capacitors C_1 and C_2, respectively.

During the auto-zero phase of A_1 and A_2, phase Φ_3 is also active, thus the A_3 and A_4 transconductance amplifiers are connected in the signal path. During the auto-zero phase of A_3 and A_4, the roles are reversed, and A_1 and A_2 are connected in the signal path.

The schematic diagram of the transconductance amplifiers A_1 and A_3 (nMOS inputs) is shown in Fig. 3. This is a folded cascode design with an input active pair M_{13}–M_{14}, the cascode transistors M_{23}–M_{24}, and cascode current mirror M_{25}–M_{28}. A secondary pMOS pair M_{15}–M_{16} is used for offset cancellation. Its transconductance is only 20% of that of the main active pair M_{13}–M_{14} to minimize the residual input referred offset due to charge injection on the offset capacitors.

Another nMOS input pair, M_{11}–M_{12} is used to control the current through the offset cancellation pair M_{15}–M_{16} and the output current sources M_{21}–M_{22}. For a common mode input close to ground, the input pair M_{13}–M_{14} is collapsed, and its output current is essentially zero. Transistors M_{11}–M_{12} also cut off the bias current for the M_{20}–M_{22} current sources, so that the total output current is null. Without this control scheme, when the M_{13}–M_{14} pair collapses for a low input common mode voltage, the total output current would be nonzero due to mismatches in the M_{21}–M_{24} current sources and the M_{25}–M_{28} cascode current mirror. A similar design has been used for the amplifiers A_2 and A_4, with pMOS input transistors.

The four clock phases are generated on chip with an interlocked logic design. This approach guaranties the correct phase sequencing and nonoverlapping intervals between phases on the order of two gate delays. The charge injection on the offset capacitors and the clock feedthrough have been minimized by reducing the skew between the pMOS and the nMOS command signals for the CMOS switches.

The pseudodifferential circuit in Fig. 4 was used as the switch driver. The relatively large skew, about 0.8 μs, after the first inverter M_1–M_2 is subsequently reduced in two pseudo-differential stages M_{11}–M_{18} and M_{21}–M_{28}. Simulations of this circuit indicate less than 200 ps output skew, worst case. This figure represents at least a factor of three to four improvement compared to the skew of an extra inverter in a conventional approach. Dummy switches could be used to further reduce the charge injection.

The output buffer is an adaptive biasing complementary circuit [3], Fig. 5. This stage has relatively good linearity due to its class AB operation, with good control of the quiescent current in the output branch, insensitivity to the input pairs M_1–M_2 and M_{11}–M_{12} mismatches, and large output

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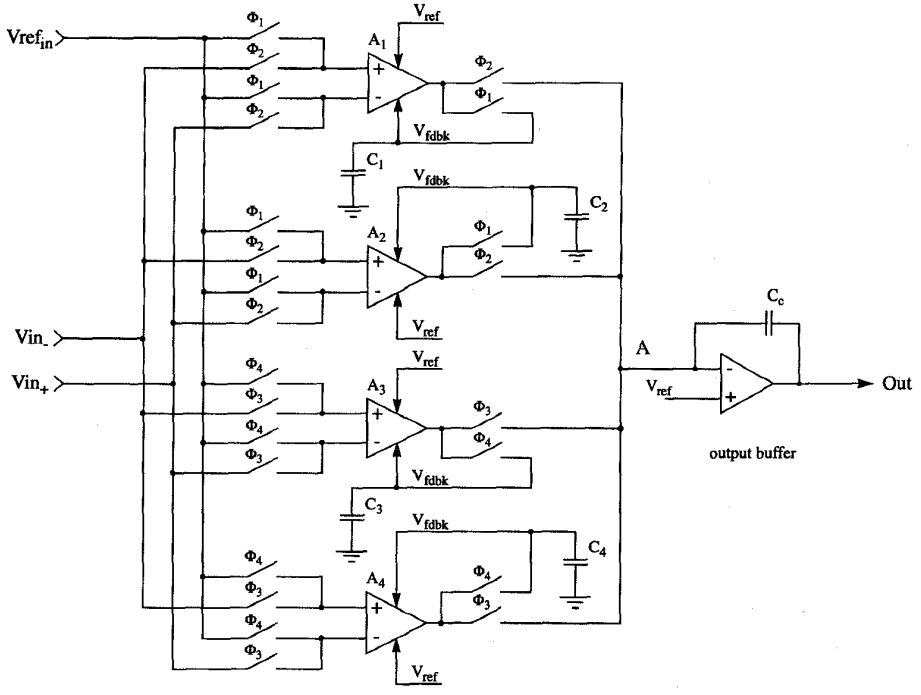

Fig. 1. Block diagram of the rail-to-rail ping-pong op-amp.

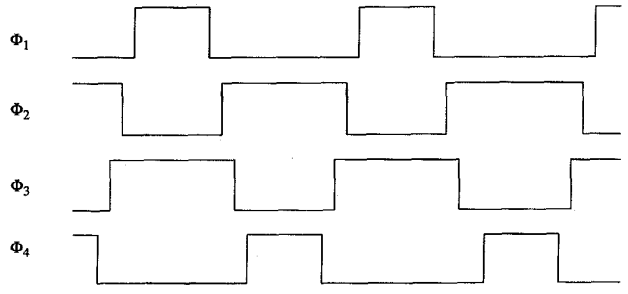

Fig. 2. Timing diagram.

current capability. The output current multiplication factor, given by the ratio of the geometric factors of transistors M_7–M_3 and M_{17}–M_{13}, is ten. The adaptive biasing is obtained with positive feedback loops with transistors M_2–M_6 and M_{12}–M_{16}. The stability is ensured by a feedback loop gain always less than unity [3].

III. Experimental Results

An experimental prototype was fabricated using the ORBIT, double poly, 2-μm CMOS process. The total active area, including the multiphase clock generator and drivers, is 610 $\times$ 420 μm^2, Fig. 6.

The overall frequency compensation of the op-amp is ensured by the Miller capacitor $C_c = 2.5$ pF (Fig. 1) across the output stage. With an 8 μA bias current in the input pairs of each transconductance amplifier A_1–A_4, the slew rate of the overall op-amp is limited to about 7 V/μs, and the small signal unity gain bandwidth is 5 MHz, decreasing to half this value near the supply or ground rails. The output buffer can drive a 2 kΩ load within 0.2 V of each rail and 100 pF capacitive load with a 62 degree phase margin.

The offset capacitors, C_1–C_4, are 5 pF each. This value represents a compromise between size, settling speed during the auto-zero phase, and sampled noise and charge injection effects. The offset cancellation feedback closed loop bandwidth is approximately 1 MHz (simulated), determined essentially by the transconductance of the offset cancelling transistors (M_{15}–M_{16} in Fig. 3) and the offset storage capacitor. At higher clock frequencies, the closed loop for offset cancellation does

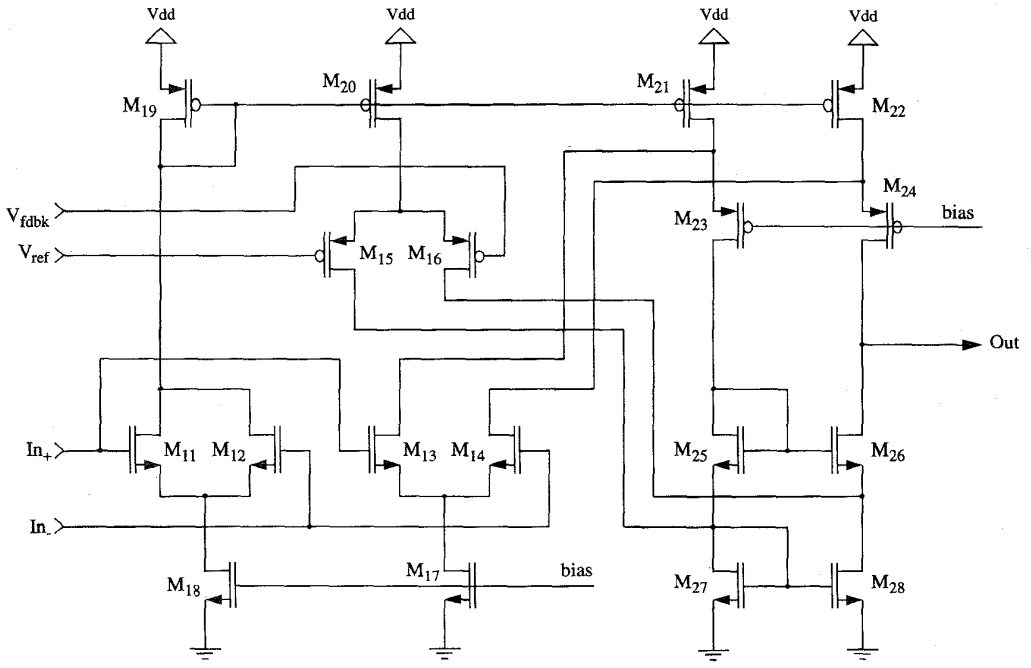

Fig. 3. Circuit schematic of the transconductance amplifier (nMOS inputs).

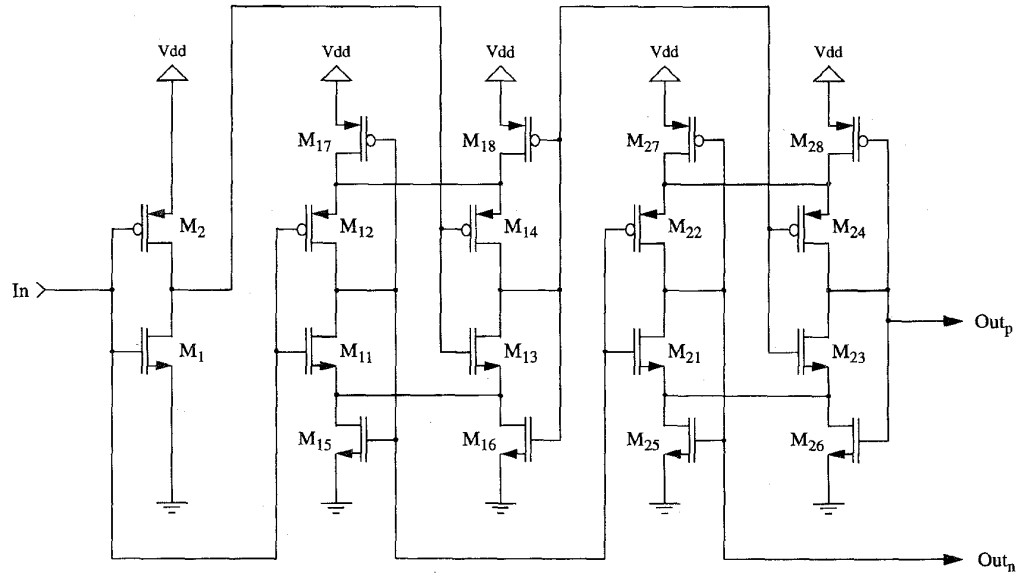

Fig. 4. Pseudodifferential CMOS switch driver.

not have enough time to settle, and a clear offset degradation was observed for clock frequencies above 200 kHz, Fig. 7.

The input referred noise has a constant power density. This noise power density, however, is dependent on the clock frequency and follows essentially the $1/f$ dependence of the original amplifier, Fig. 8. Due to the small input device sizes (12/4 nMOS and 32/4 pMOS), the $1/f$ noise corner is around 200 kHz. At this frequency, the clock feedthrough measured at the output was about 135 μV_{rms}, and the residual input referred offset at mid-supply was less than 100 μV for all the four fabricated samples. Any offset difference in the two op-amp paths will show up as a frequency component at the clock frequency and could not be separated from the real clock feedthrough. Thus, a clock frequency between 50 kHz

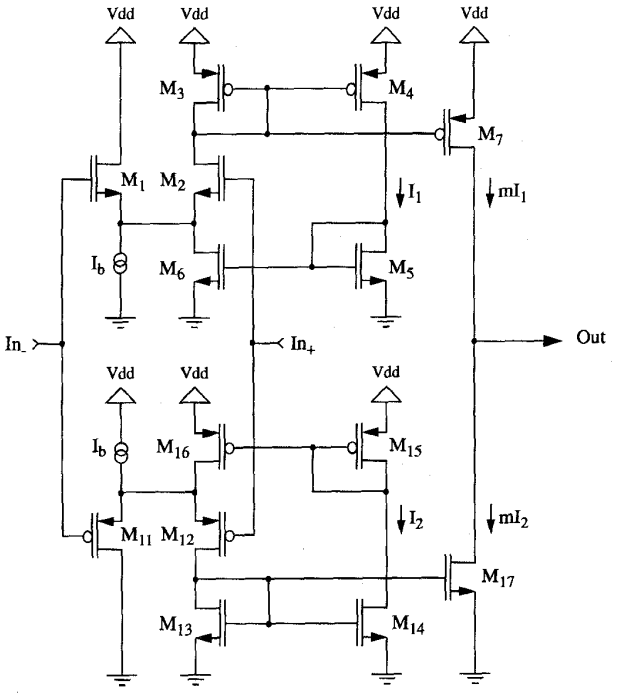

Fig. 5. Schematic diagram of the output buffer.

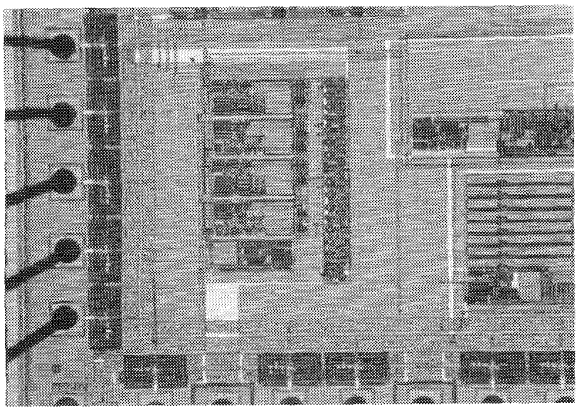

Fig. 6. Photomicrograph of the ping-pong op-amp.

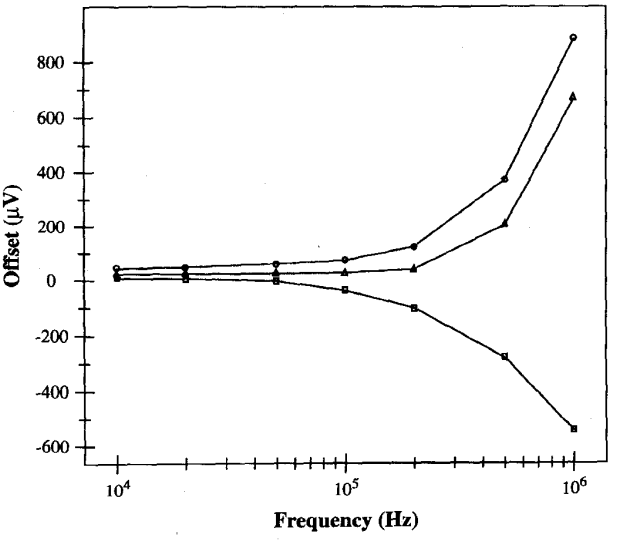

Fig. 7. Offset dependence on the clock frequency.

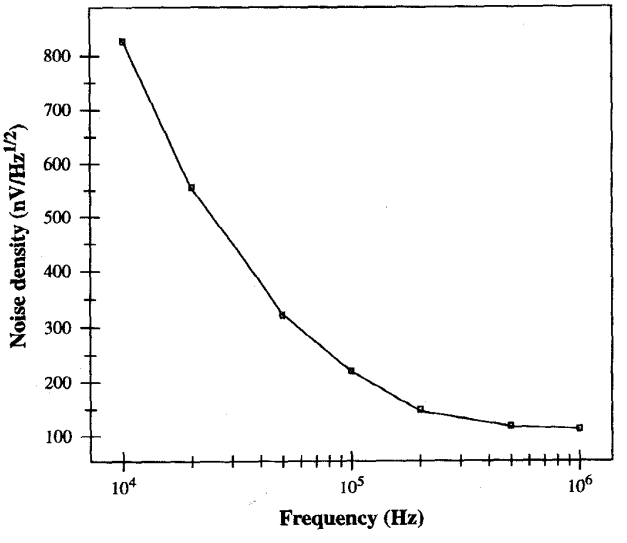

Fig. 8. Input referred noise floor versus clock frequency.

and 200 kHz represents a good compromise for this design between the clock feedthrough, residual offset, and the $1/f$ input referred noise [1].

Very good offset cancellation over the whole rail-to-rail input range was achieved. A typical offset variation with the common mode voltage is shown in Fig. 9. The offset behavior in the 0.6–1.2 V input common mode range was observed for all fabricated samples and it is attributed to a layout problem, probably increased clock feedthrough for input levels near the nMOS threshold. To minimize the effect of the input common mode voltage on the bias current sources, the offset cancellation reference input $V_{ref_{in}}$ has been connected to V_{in_+}, Fig. 1. This variation can also be greatly reduced by using cascode current sources for the bias of the input pairs. In a unity gain configuration with a 10 kΩ load, the distortion for a 4.9 $V_{\rm pp}/1$ kHz input signal was less than -71 dB. The corresponding output spectrum is shown in Fig. 10. This distortion is limited primarily by the offset variation with the input common mode. Without the ping-pong control, the expected 5–10 mV of offset mismatch between the pMOS and nMOS input pairs in a conventional rail-to-rail op-amp would limit the rail-to-rail distortion to above approximately -55 dB

IV. Conclusion

A rail-to-rail op-amp with a ping-pong offset cancellation scheme has been described. This technique avoids both alias-

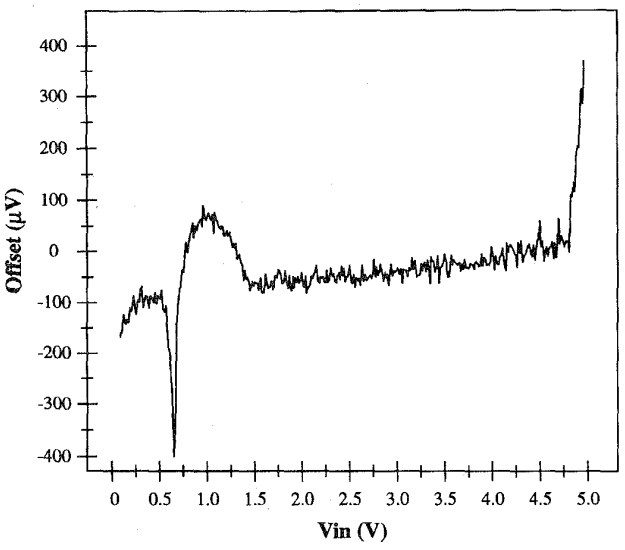

Fig. 9. Offset dependence on the input common mode voltage.

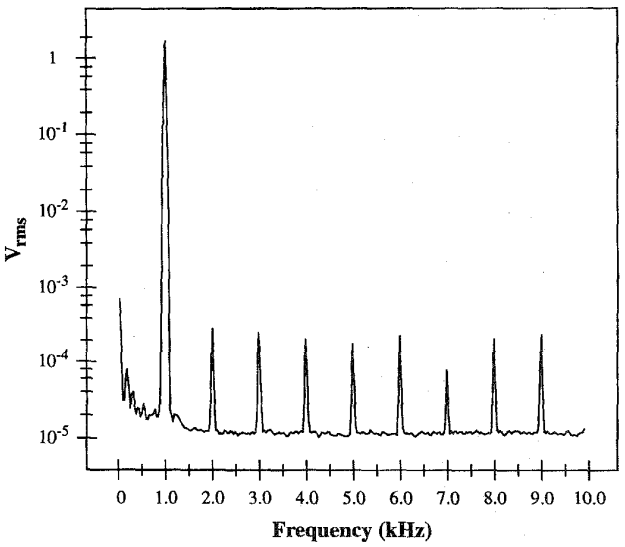

Fig. 10. Output spectrum for a 4.9 V_{pp}/1 kHz sine input.

ing of the amplifier broad band noise and folding of the input spectrum. Therefore, it can be used in applications requiring a signal bandwidth larger than the clock frequency. The chosen clock frequency of 100 KHz represents a compromise between the clock feedthrough, residual offset, and the $1/f$ input referred noise. The experimental prototype achieved an input referred noise of about 225 nV/Hz$^{1/2}$ and an offset less than 100 μV, while having very low distortion for rail-to-rail input signals.

REFERENCES

[1] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE J. Solid-State Circuits,* vol. SC-22, no. 3, pp. 335–342, 1987.

[2] C.-G. Yu and R. L. Geiger, "An automatic offset compensation scheme with ping-pong control for CMOS operational amplifiers," *IEEE J. Solid-State Circuits,* vol. 29, no. 5, pp. 601–610, 1994.

[3] M. G. Degrawe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits,* vol. SC-17, no. 3, pp. 522–528, 1982.