A Tiny, High-Speed, Wide-Band, Voltage-Feedback Amplifier Stable with All Capacitive Load

Farhood Moraveji

Abstract—**A tiny, high-speed, wide-band, voltage-feedback operational amplifier capable of driving unlimited capacitive load is described. A class AB input stage is combined with a modified dynamic Witch-Hazel current mirror to provide high slew rate and wide bandwidth with a small die area and small idle current. An RC network couples part of the capacitive load into the high-impedance node, therefore lowering the dominant pole and increasing stability as a function of capacitive load. The part was fabricated on a 3 GHz, 40 V complementary bipolar process. The quiescent current of the chip is 4.5 mA with 1500 V/μm slew rate and a −3 dB bandwidth of 235 MHz. The part is operational from ±2.5 V to ±18 V supply range. Die size is 38 mils by 46 mils and it fits into a tiny surface outline transistor (SOT) package.**

I. Introduction

IN high-performance systems, integration of high-frequency analog is not easily achievable. One possible alternative is to use very small packages for the versatile signal conditioning blocks without sacrificing the performance. This puts stringent constraints on the die size and demands new circuit techniques which provide higher performance with fewer transistors. This paper describes a wide-band, high slew rate amplifier capable of driving any size capacitive load with a small die size designed to fit in the tiny surface outline transistor (SOT) package.

In order to achieve higher slew rate together with wide bandwidth, low input offset voltage, high open-loop gain, lower power, and smaller die size, this circuit required a new design for the signal current mirror and biasing scheme. Smaller package size puts a severe constraint on the use of additional transistors for better performance and limits the amount of power dissipation because of the relatively high thermal resistance of SOT package which is about 325°C/W.

Traditionally, external components such as snubber-resistors are used to maintain stability while driving large capacitive loads. However, this technique works for well-defined capacitive loads and comes at the expense of current drive, voltage swing, and external components. In the design of this amplifier, the output stage is modified in such a way that the part can handle any size capacitive load while maintaining its stability. In Section II, general amplifier architecture is described. In Section III, pros and cons of current mirrors are reviewed and the modified Witch-Hazel current mirror together with the input offset cancellation scheme are examined. Section IV concludes with some experimental results and depicts the amplifier performance.

Manuscript received February 15, 1996; revised June 24, 1996.

The author was with National Semiconductor Corporation, Santa Clara, CA, USA. He is now with S3 Inc., Santa Clara, CA 95052-8058 USA.

Publisher Item Identifier S 0018-9200(96)07325-8.

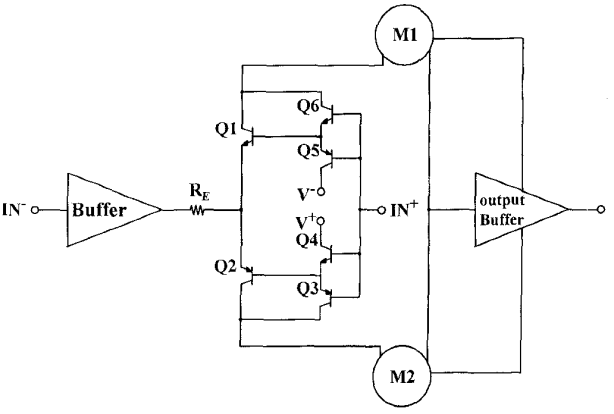
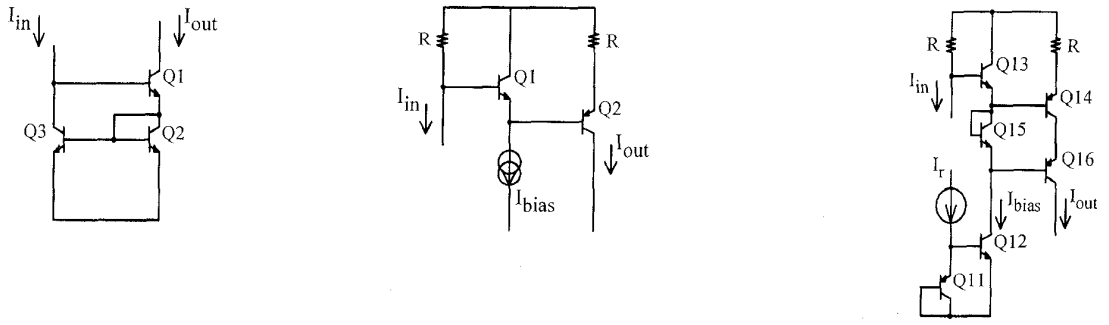


Fig. 1. Simplified amplifier block diagram.

II. Amplifier Architecture

Fig. 1 shows the basic amplifier architecture used in this design. Complementary emitter followers Q1–Q4 form the noninverting input of the amplifier driving the degeneration resistor RE while the other side of this resistor is connected to inverting input via a buffer. This is basically a class AB input stage with very symmetrical characteristics [1]. The collector signal currents of transistors Q1 and Q2 are turned around and summed through mirror M1 and M2, respectively. This signal current multiplied by the impedance seen at the high-impedance point (input of the output buffer) sets the open-loop gain of the amplifier. As one can see from this simplified block diagram, the ac performance and dc accuracy of current mirrors M1 and M2 greatly influence the overall operation of the amplifier. Any dc mismatch of current generated by these mirrors appear as a systematic dc offset voltage where feedback is coupled around the op-amp. Also, how fast these current mirrors can turn around the signal current as a function of frequency will set a limit on the speed of the amplifier. Needless to say, the output impedance of the mirrors directly affects the gain of the amplifier. So, the overall performance of these current mirrors plays a crucial rule in the circuit behavior and care must be taken in selecting the proper mirrors based on the specific requirements of the design.

The voltage obtained at high-impedance node is isolated from the output via the output buffer. In order to improve the speed of the output buffer for fast signals, the idling current



(a) (b) (c)

Fig. 2. Schematic diagram of different types of current mirrors. (a) Wilson current mirror. (b) Witch-Hazel current mirror. (c) Modified Witch-Hazel current mirror.

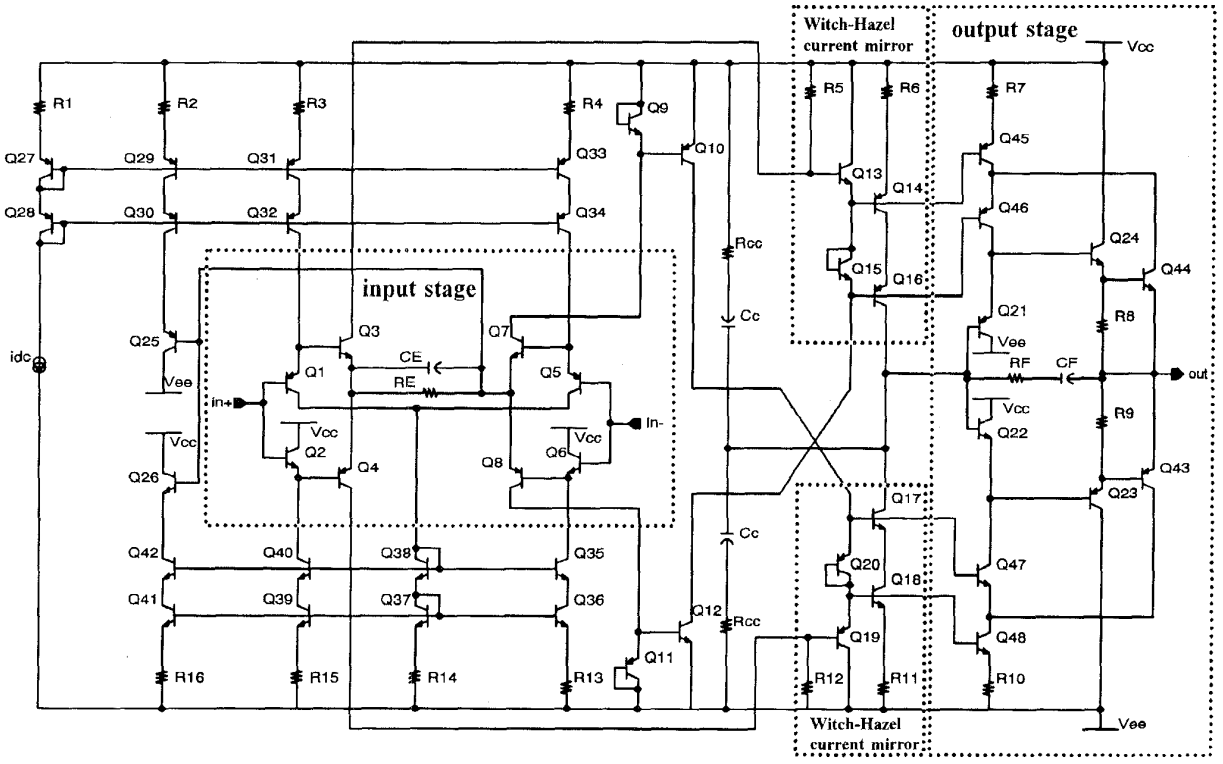


Fig. 3. Simplified schematic diagram of the amplifier.

of the buffer is dynamically adjusted through mirrors M1 and M2 while sinking or sourcing the current into the load.

III. Current Mirrors and Amplifier Circuit

A. Current Mirrors

In the design of this amplifier, the goal was to choose a fast current mirror with relatively high output impedance which doesn't suffer from dc inaccuracy. To fulfill this task, several current mirrors were examined both from dc and ac points of view and the results are tabulated as follows [2].

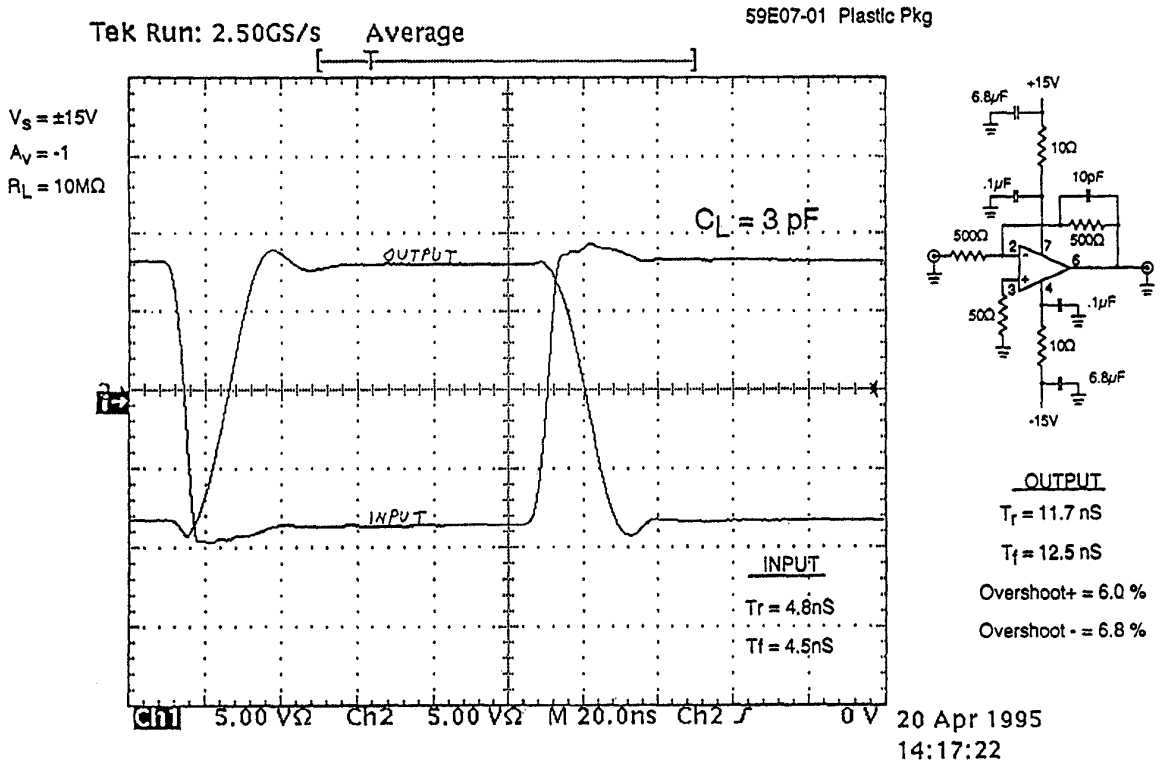
1) Wilson Mirror: Fig. 2(a) shows the basic schematic diagram of Wilson current mirror. For this mirror the output impedance is equal to

$$R_o \cong \beta\left(\frac{r_{o1}}{2}\right) \tag{1}$$

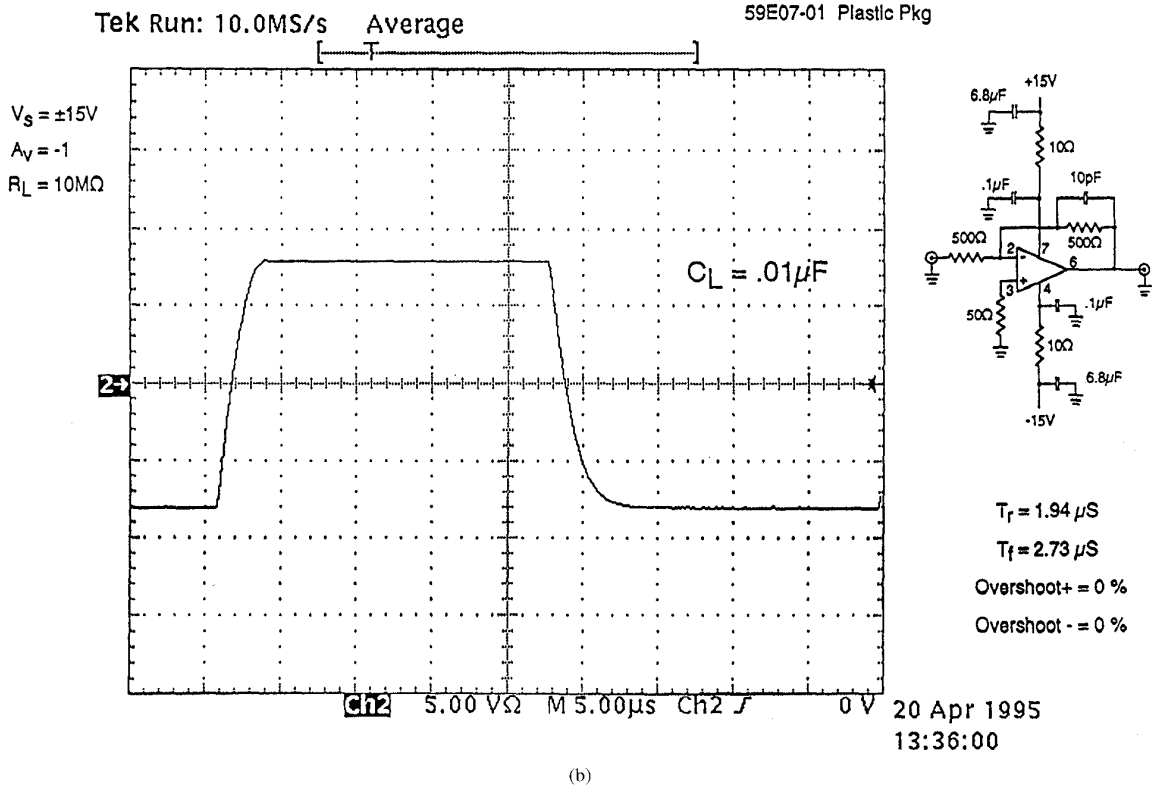
where β is the dc current gain and r_{o1} is the output resistance of transistor Q1. Also, the transfer function of the current in the frequency domain is

$$\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{\beta_o(\beta_o+2)}{\beta_o^2+2\beta_o+2}\,\frac{1+2Sr_eC\pi}{1+2Sr_eC\pi+2S^2(r_eC\pi)^2}. \tag{2}$$

As one can see from these equations, the Wilson current mirror has high output impedance together with good dc accuracy. However, due to poles and zeros, it suffers from

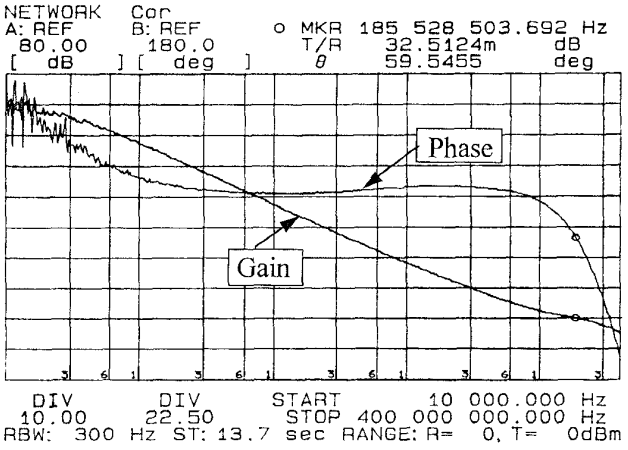


(a)



(b)

Fig. 4. (a) Large signal pulse response of the amplifier driving 3 pF of capacitive load (slew rate is 1500 V/μs). (b) Large signal pulse response of amplifier driving 0.01 μF capacitive load.



BW = 185 MHz PM = 59 degrees

Fig. 5. Open-loop gain and phase of the amplifier, $V_s = \pm 15$ V, $R_L = 1$ kΩ.

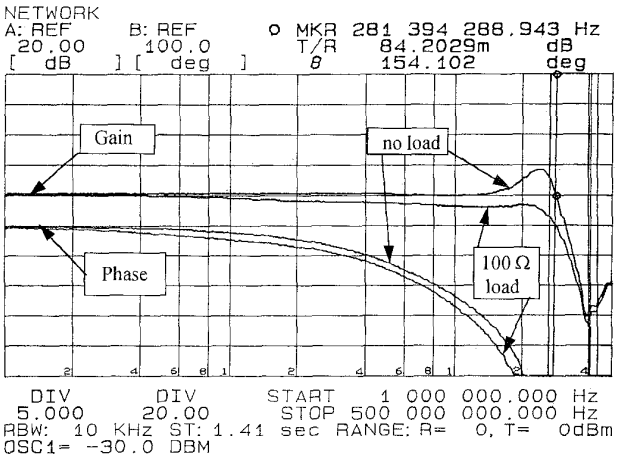


Fig. 6. Closed-loop frequency response of the amplifier with no load and 100 Ω load conditions.

high frequency peaking and it was not a good candidate from a speed point of view.

2) Witch-Hazel Mirror: A simplified schematic diagram of the Witch-Hazel current mirror is depicted in Fig. 2(b). Here, the relationship between the input and output currents can be written as

$$I_{\text{out}} = \frac{V_T}{R} \ln\left[\left(\frac{I_{\text{bias}}}{I_{\text{out}}}\right)\left(\frac{I_{\text{sp}}}{I_{\text{sn}}}\right)\right] + I_{\text{in}} \tag{3}$$

$$\Delta I = I_{\text{out}} - I_{\text{in}} = \frac{V_T}{R} \ln\left[\left(\frac{I_{\text{bias}}}{I_{\text{out}}}\right)\left(\frac{I_{\text{sp}}}{I_{\text{sn}}}\right)\right] \tag{4}$$

and the output resistance of this mirror is

$$R_o \cong r_o(1 + g_m R). \tag{5}$$

This type of mirror is usually very fast due to the fact that input signal current is driving a relatively low base impedance (resistor R from base of transistor Q1 to supply). Also, the mirror is not prone to saturation. Although the mirror is superior in terms of speed, it suffers from low output resistance and poor dc accuracy. Equation (4) shows that this has an uncontrollable dc error which is mainly due to the V_{be} mismatch of Q1 and Q2. This error is process dependent and can create a systematic input offset voltage.

3) Modified Witch-Hazel Mirror: Fig. 2(c) shows the simplified schematic diagram of the modified Witch-Hazel mirror. Addition of transistors Q15 and Q16 increases the output resistance of the mirror significantly. Equation (4) showed that the inherent dc error of Witch-Hazel mirror is dependent on the ratio of reverse saturation currents of PNP and NPN as well as "I_{bias}" which sets the mirror bias current.

In the modified mirror version which is shown in Fig. 2(c), the bias current "I_{bias}" is made proportional to the ratio of reverse saturation currents of a *npn* over that of a *pnp*. By examining the mirror formed by Q11–Q12 and equating their V_{be}, we can write

$$I_{\text{bias}} = I_r\left(\frac{I_{\text{sn}}}{I_{\text{sp}}}\right). \tag{6}$$

By substituting (6) into (4), we get

$$\Delta I = \frac{V_T}{R} \ln\left(\frac{I_r}{I_{\text{out}}}\right). \tag{7}$$

Equation (7) shows that the dc error terms depend on the logarithmic ratio of the reference current I_r and output current I_{out}. If these currents are made equal, the dc error term becomes zero. One important point to remember is that I_{out} should dynamically follow I_r to result into zero error, therefore, I_r must be signal driven. This is the key point in the design of this tiny amplifier. A differential input stage has been designed in such a way that it makes I_r and I_{out} equal as a function of input signal, therefore reducing the error.

TABLE I
TYPICAL MEASURED PERFORMANCE DATA

PARAMETER	VALUE
SUPPLY CURRENT	4.5 mA
GAIN	75 dB
INPUT BIAS CURRENT	2 uA
OFFSET VOLTAGE	1 mV
CMRR	75 dB
PSRR	95 dB
GBW	185 MHz
PM	59 degrees
SLEW RATE	1500 V/usec
SUPPLY VOLTAGE	+/- 2.5V to +/- 18V
OUTPUT SWING @ 30V	26.5 Vpp

B. Amplifier Circuit

Fig. 3 shows the simplified schematic diagram of the amplifier which utilizes the modified Witch-Hazel current mirrors

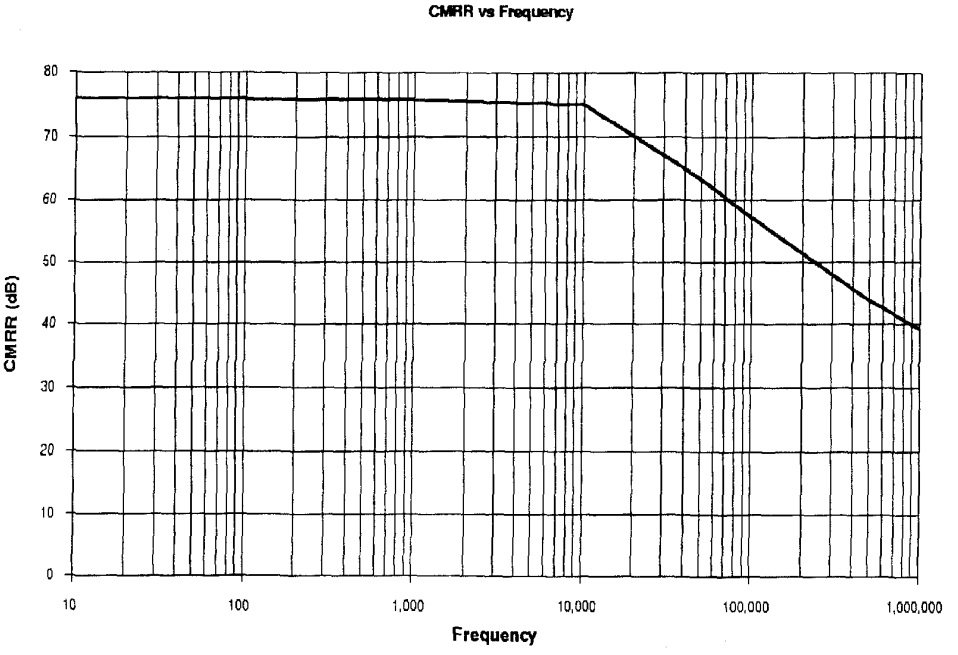


Fig. 7. CMRR frequency response of the amplifier, $R_L = 10$ kΩ.

together with input offset cancellation scheme. Here, Q1–Q4 form the equivalent of the current-feedback input buffer, RE the equivalent of a feedback resistor which sets the transconductance of the input stage, and Q5–Q8 buffer the inverting input. The quiescent current of the input stage is set by cascoded mirrors Q31–Q34 in the top-side mirror and Q35–Q40 in the bottom-side mirror [3].

A differential input voltage, ΔV, is applied to the input of this amplifier and creates a differential current ΔI that appears at the collectors of Q3–Q4 in one side and Q7–Q8 at the other side [4]. Remember that from the signal point of view, the collector currents of Q3 and Q8 as well as the collector currents of Q4 and Q7 follow each other. Collector currents of Q3 and Q4 are mirrored and summed via the modified Witch-Hazel mirror Q13–Q16 in the top side and Q17–Q20 in the bottom side. This signal current multiplied by the impedance seen at the high-impedance node (collectors of Q16 and Q17), sets the open-loop gain and the dominant pole of the amplifier. To compensate for the $V_{\rm be}$ mismatch of these mirrors, the collector currents of transistors Q7 and Q8 are turned around via the mirror Q9–Q10 in the top-side and Q11–Q12 in the bottom-side and then set the bias currents of the Witch-Hazel mirrors, respectively. Since the bias current through these mirrors is proportional to the ratio of reverse saturation current of a NPN over a PNP, they compensate for the $V_{\rm be}$ mismatch of the Witch-Hazel mirror and its reflected input offset voltage.

The RF-CF network between the high-impedance node and output serves as a frequency compensation adjuster which effectively increases the overall compensation as a function of capacitive load [1], [6]. When there is no capacitive load or its value is very small, this network is fully bootstrapped through the output stage and has minor effect on the bandwidth. However, for heavy capacitive loads, RF-CF is partially bootstrapped and effectively reflects part of the capacitive load to high-impedance node, therefore improving the phase margin by reducing the bandwidth and enhancing the stability. The capacitor CE in parallel with RE extends the bandwidth at high frequency [1]. The network $R_{cc} - C_c$ sets the dominant pole of the amplifier.

The simple class AB output stage consists of transistors Q21–Q24. Dynamic current sources Q45–Q46 in the top side and Q47–Q48 in the bottom side set the current through this stage.

IV. Performance and Conclusion

This amplifier has been fabricated on a high-frequency complementary bipolar process and the dimensions of the die are 36 mils by 48 mils [5]. The amplifier has been fully characterized and the typical measured performance data is shown in Table I. Fig. 4(a) and (b) shows the large signal pulse response of the amplifier driving 3 pF and 0.01 μF capacitive load respectively. Diving 3 pF of capacitive load with slew rate of 1500 V/μs, the overshoot is about 6.8%. The open-loop gain and phase of the amplifier is depicted in Fig. 5. The graph shows that the unity gain-bandwidth of the amplifier is 185 MHz with 59 degrees of the phase margin. In Fig. 6, the closed-loop frequency response of the part under no-load and 100 Ω load conditions is shown. Fig. 7 shows the CMRR as a function of frequency.

In conclusion, a tiny, low-power, high-speed, and high slew-rate voltage-feedback amplifier has been described. Die-size constraint together with demand for higher speed and lower power limited the number of transistors available to the circuit design. In the design of this amplifier, the modified Witch-Hazel current mirror and its associated biasing scheme provided good AC performance and DC accuracy.

The collector currents of the class AB input differential pair were used not only to drive the high-impedance node but also to bias the amplifier. The relatively large collector-to-Nwell parasitic capacitances on the PNP signal path transistors were bootstrapped to minimize their effect and improve the bandwidth [4]. The amplifier is operational from ± 2.5 V to ± 18 V supply range and can handle unlimited capacitive load.

REFERENCES

[1] F. Moraveji, "A low-power, high-speed, voltage-feedback operational amplifier on a low-cost 40 V complementary bipolar technology," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 1994, pp. 19–22.

[2] J. Davidse, *Analog Electronic Circuit Design*. Englewood Cliffs, NJ: Prentice-Hall, pp. 166–170, 1991.

[3] D. Smith, M. Koen, and A. F. Witulski, "Evolution of high-speed operational amplifier architectures," *IEEE J. Solid-State Circuits*, vol. 29, no. 10, pp. 1166–1179, Oct. 1994.

[4] F. Moraveji, "A wide-band, low-power, high slew rate voltage-feedback operational amplifier," *IEEE J. Solid-State Circuits*, vol. 31, no. 1, pp. 10–16, Jan. 1996.

[5] R. Bashir *et al.*, "A 40 Volt silicon complementary bipolar technology for high-precision and high-frequency analog circuits," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 1994, pp. 225–228.

[6] Analog Devices AD847 and AD817 datasheets.