A PLL-Based Frequency Synthesizer for 160-MHz Double-Sampled SC Filters

F. Rezzi, F. Montecchi, and R. Castello

Abstract—**This paper describes a clock generator for a double-sampled switched capacitor (SC) filtering system. The circuit is based on a fast charge-pump phase-locked loop (PLL) system that multiplies an external reference clock signal by a factor of eight and also ensures a high precision and stability of two internal nonoverlapped clock phases up to 80 MHz. This allows the driving of double-sampled SC filters up to 160 MHz sampling rate. The PLL is a third-order system with a bandwidth of 100 kHz and a lock-in time of 15 μs. The output clock jitter is 170 ps rms. The total power consumption at 160 MHz is 25 mW and the total chip area is about 1 mm^2.**

I. Introduction

DOUBLE-SAMPLED switched capacitor (SC) systems require two nonoverlapping clocks. These signals can be viewed as two clock waveforms precisely separated by 180°, each with a duty-cycle of less than 50% [1]. Since these two clocks drive analog MOS switches, their shapes must be well defined, with a rail-to-rail voltage swing and sharp edges in order to define the sampling instants accurately. Another important property is that the phase noise (jitter) must be as low as possible to avoid a random phase-modulation of the sampled signals.

One advantage of using a double-sampling strategy is that the frequency of each clock signal is half the sampling rate. On-chip frequency synthesizers often generate first a clock at the sampling frequency by means of an internal VCO and divide it by two [2]. In this way, a precise 50% duty-cycle can be obtained, and the sampling instants are defined on both the rising and falling edges. A simple digital network based on the delay of logic gates allows recovery of the two nonoverlapping phases starting from this signal. The key point of the system here presented is that the oscillation frequency of the VCO is the same as that of the clock phases, which relaxes the speed requirements of the VCO by a factor of two. The accuracy in the generation of the timing signals is, in this case, inherently guaranteed by the circuit characteristics.

This paper describes an integrated phase-locked loop (PLL) based frequency synthesizer capable of locking on to an external frequency up to 10 MHz, multiplying it by a factor of eight and generating, by means of an internal VCO, two nonoverlapping clock signals which can drive a double-sampled SC filter with a sampling rate up to 160 MHz.

The VCO and the nonoverlapping circuits are described in Section II. Section III discusses the PLL system with the phase frequency detector (PFD) and the charge-pump circuit.

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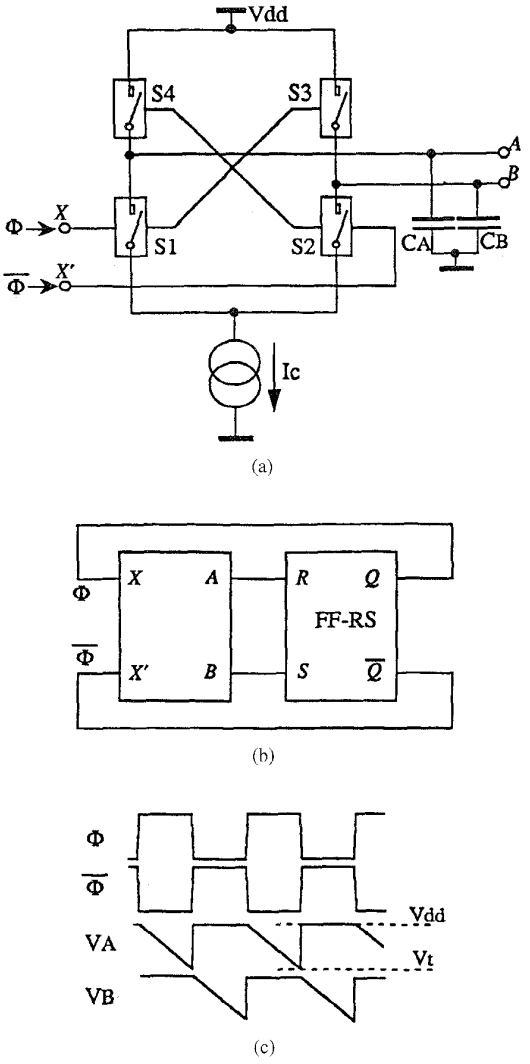

Fig. 1. (a) Ideal schematic of the ramp generation circuit. (b) Structure of the VCO. (c) Corresponding output waveforms.

In Section IV experimental results from a test prototype circuit integrated in a 1.2-μm BiCMOS technology are presented.

II. VCO Circuit

As mentioned before, in this design the generation of the two nonoverlapping phases is obtained avoiding frequency division. The proper phase relation between the two clocks is guaranteed by the structure of the VCO and the phase generators which are realized from a single core element called a ramp generator.

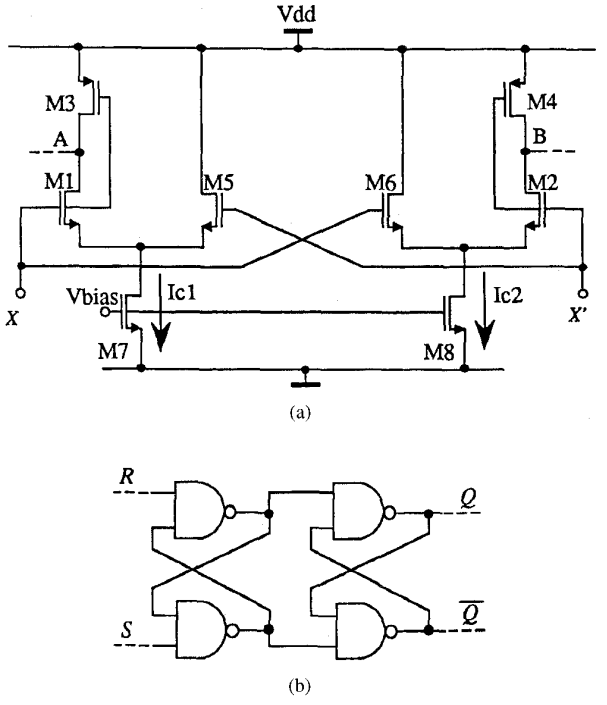

Fig. 2. Circuit implementation of (a) the ramp generator and (b) the feedback circuit.

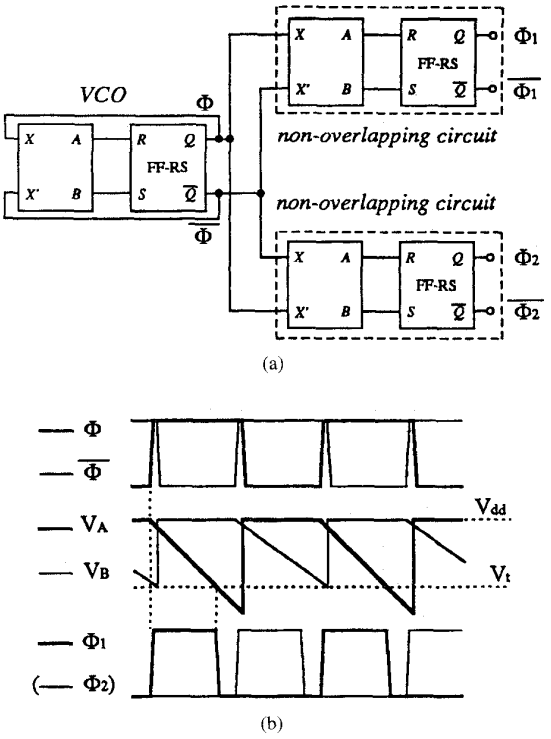

Fig. 3. (a) Overall block structure for the generation of the two nonoverlapping waveforms. (b) Corresponding voltage waveform V_A and Φ_1 (V_B and Φ_2 in thin lines).

A. Oscillator Description

The conceptual schematic of the ramp generator presented here is shown in Fig. 1(a) where Φ and $\overline{\Phi}$ indicate two complementary digital control signals [3]. When Φ is high ($\overline{\Phi}$ low) S1 and S3 are closed and C_A is discharged via the current I_c with a negative slope equal to I_c/C_A while C_B is shorted to the positive supply voltage V_{dd}. When Φ is low ($\overline{\Phi}$ high) the circuit operation is reversed, exchanging S1 (S3) with S2 (S4) and C_A with C_B. This ramp generator, with the help of proper feedback elements, can be used to implement a relaxation oscillator. This is represented in Fig. 1(b) in which the feedback element is a set-reset flip-flop (FF-SR). In this way, the discharging of the capacitors is interrupted each time the voltage at node A or B reaches the high-to-low switching threshold of the FF-SR. If C_A and C_B have the same value C, the voltage waveforms at nodes A and B (V_A, V_B) as a function of time are as shown in Fig 1(c). The circuit oscillates at a frequency f_o equal to

$$f_o = \frac{1}{2}\frac{1}{\frac{C(V_{dd}-V_t)}{I_c} + t_d}$$

where t_d is the propagation delay of the FF-SR. The frequency of the oscillator can be changed through the value of the tail current I_c in Fig. 1(a). The theoretical limit of f_o for $I_c \to \infty$ is $1/(2t_d)$.

The proposed implementations of the ramp generator and of the feedback FF-SR circuit are as shown in Fig 2(a) and (b). In Fig. 2(a), two distinct current generators I_{c1} and I_{c2} are used as opposed to the single one of Fig. 1(a). In this way, it is possible to independently control the discharging slope of the

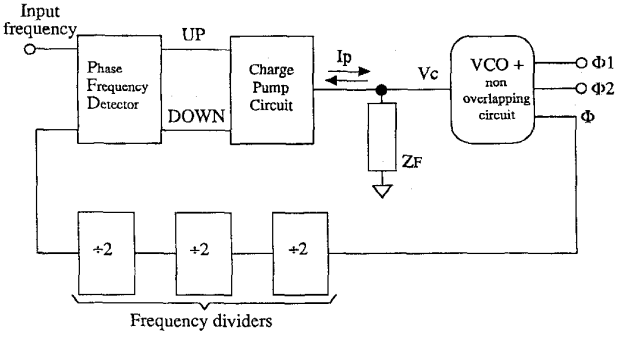

Fig. 4. Block schematic of the PLL.

voltages at node A and B during the two semi-periods of the output waveforms. This additional flexibility will be profitably used in the nonoverlapping circuits to be described later. The additional pass-transistors M5 and M6 switch the currents to V_{dd} when not used.

This structure shows an additional advantage. In fact, due to the delay t_d in the feedback circuit, the voltage at the common source of the n-MOS switches M1, M5 (M6, M2) tends to fall below the threshold voltage V_t [indicated in Fig. 1(c)] of the feedback FF-SR. This phenomenon (more apparent when the length of each semi-period is comparable with t_d) may force the current generator M7 (M8) in the triode region of operation. In the presence of this wrong bias condition, the discharging time would differ from the expected value if the current has to be immediately used to control the following

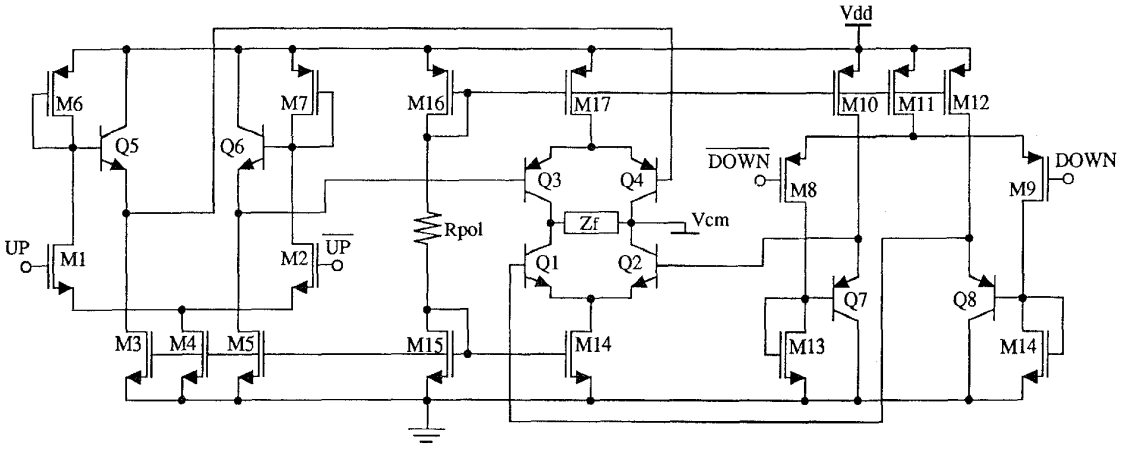

Fig. 5. Charge-pump circuit schematic.

discharging phase [as in the case of Fig. 1(a)]. In Fig. 2(a) transistor M5 (M6) brings M7 (M8) into the saturation during the inactive time allowing the current to recover its nominal value before the beginning of the next discharging period.

Capacitors C_A and C_B are the parasitic capacitances at the respective nodes. Good matching between these two capacitances is achieved by using a large input gate capacitance of the FF-SR circuit connected at these nodes and by carefully controlling the symmetry of the layout.

The FF-SR circuit shown in Fig. 2(b) consists of a series of two latches implemented with NAND gates. Even though the second latch increases the total feedback delay t_d, it acts as buffer improving the slope of the switching edges of the signals Φ and $\overline{\Phi}$.

Since the clocks are the output signals of an SR latch, a NAND delay time exists between the switching instants of Φ and those of its complementary phase $\overline{\Phi}$. As a consequence, the duty-cycle of the waveforms slightly differs from 50%. However, the two waveforms maintain the feature of being exactly 180° out of phase with each other. This is the key for proper operation.

B. Nonoverlapping Circuits

Each of the two nonoverlapping phase generators (one for phase Φ_1 and one for phase Φ_2) consists of the ramp generator of Fig. 2(a) followed by the FF-SR of Fig. 2(b). The ramp generator is driven by the two phases Φ and $\overline{\Phi}$ generated by the VCO as shown in Fig. 3(a). The structure of the nonoverlapping circuits is the same as that of the oscillator with the exception of the currents I_{c1} and I_{c2} that, in this case, are chosen to be $I_{c1} = 1.5I_{c2}$. In this way, I_{c1} speeds up the discharging ramp during one semi-period of the input signal Φ, thus reducing the duty-cycle of the output signal while maintaining the same overall period (i.e., that of signals Φ).

To properly generate the two phases Φ_1 and Φ_2, the two nonoverlapping circuits are driven with opposite phase from the outputs of the VCO. The timing diagram for the waveforms is shown in Fig. 3(b).

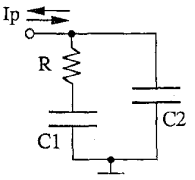

Fig. 6. Implementation of the loop impedance.

Since the VCO and the nonoverlapping circuits are identical, they can be laid out in the same way, allowing an excellent matching for the parasitics at the critical nodes.

III. Overall System Description

The whole system is shown in the block diagram of Fig. 4. The PLL uses a PFD to drive a charge-pump circuit whose schematic is presented in Fig. 5.

The charge-pump circuit is preceded by two voltage-swing converters which transform the two full-swing CMOS signals UP and DOWN into low-swing logic signals (and their complements). These low-swing signals drive two high-speed bipolar current switches (each implemented with a PNP and an NPN transistor pair) that deliver $\pm I_p$. The reduced swing of the UP and DOWN signals limits the total amount of charge injection and increases the switching speed by avoiding the saturation of the bipolar devices.

Maximizing the speed or equivalently the bandwidth of the PLL is important to obtain good noise filtering and, therefore, a low jitter in the output clock when the main source of noise is the internal circuits. The reason for this is that, provided that a jitter-free input reference signal is available, the PLL is able to reject the noise spectral components up to its bandwidth. Therefore, the higher the bandwidth, the more the amount of noise rejected [4], [5]. On the other hand, a loop impedance as that of Fig. 6 gives rise to a third-order loop which is potentially unstable. As a consequence, the increasing of the PLL bandwidth can affect the stability of the loop as well as reduce the lock-in range [6].

The influence on the stability and on the lock-in range of the PLL of parameters such as the voltage-to-frequency

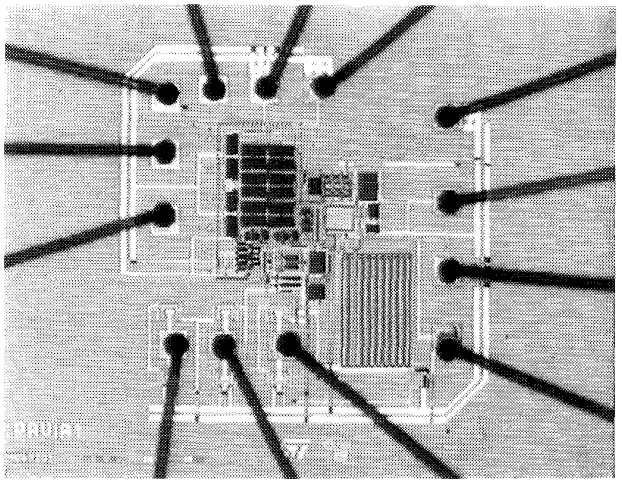

Fig. 7. Chip photograph.

characteristic of the VCO, the charge-pump current I_p, and the value of the components in the loop-impedance have been investigated using a PC program written for that purpose. The program simulates the time evolution of the output frequency of the VCO in response to a frequency step at the input. In this way, the loop impedance which gives the best tradeoff between level of stability, maximum lock-in range, and speed of response has been chosen.

The passive components that make up the loop-impedance have been chosen to have the following values: $C_1 = 80$ pF, $C_2 = 20$ pF and $R = 4$ kΩ. They have been completely integrated so that no external components are required for the PLL. The nominal value of the reference current in the charge-pump circuit is 200 μA.

The system uses a cascade of three frequency dividers allowing the multiplication of the input frequency by a factor of eight. In this way, three additional clock signals at binary scaled frequencies are available. The combination of these clocks with the main high frequency nonoverlapping waveforms could potentially allow the generation of more sophisticated clock sequences [7].

IV. Experimental Results

An experimental prototype of the PLL-based clock generator has been built using a technology named HF3CMOS from SGS-Thomson. This technology offers 1.2-μm minimum channel CMOS transistors and 7-GHz NPN bipolar devices together with an optional 3-GHz vertically isolated PNP. The chip microphotograph is shown in Fig. 7. The total active area is about 1 mm^2.

Fig. 8 shows the plots of the 40 MHz and 80 MHz output waveforms. The fraction of the total period in which neither clock is high depends on the rising and falling time of the waveforms and, therefore, on the total capacitive load. In our case, the circuit has been designed with output buffers capable of driving a capacitive load up to 1.2 pF per phase.

To suppress any replica of the filter frequency response at one half the effective sampling frequency (ghosts), the

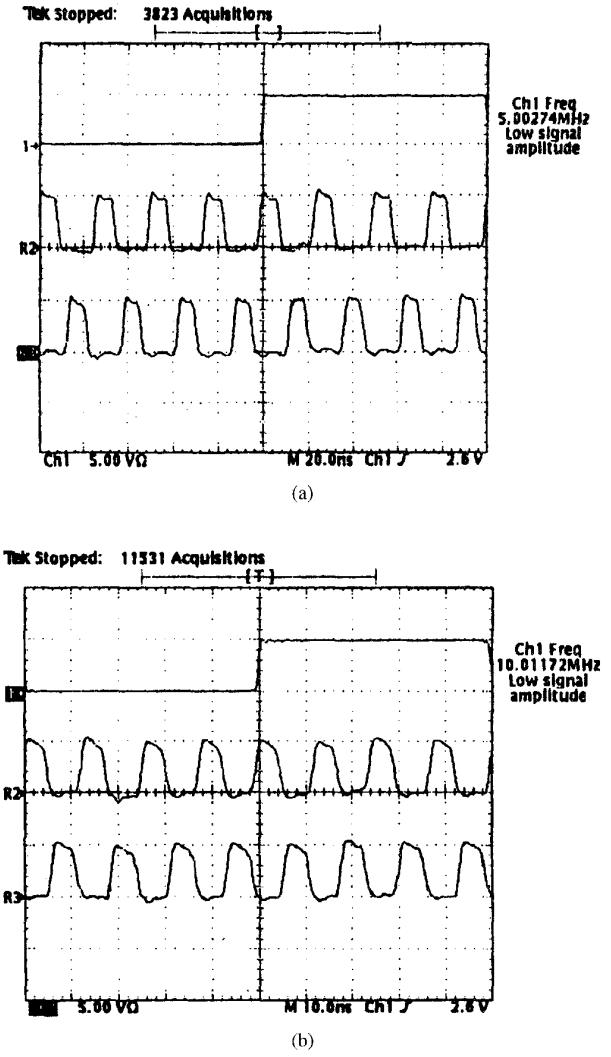

Fig. 8. Output clock waveforms corresponding to (a) 5 MHz and (b) 10 MHz. The sampling rate is 80 and 160 MHz, respectively.

sampling period should be exactly constant. This fundamental specification has been checked by acquiring a sample of more than 50 clock periods and computing the times at which the falling edges of the two clocks cross a fixed reference voltage (that simulates the threshold at which the n-MOS switches close). The time intervals between successive sampling instants has shown a maximum deviation of 0.5% on an average value of 6.147 ns (i.e., $\approx$162 MHz of sampling rate). This measure gives evidence of the good matching properties of the VCO and, in general, of the feasibility of the proposed technique.

The above analysis has been performed on clock waveforms which are the result of an averaging of more than 1000 acquisitions in order to eliminate the random variation of the sampling period due to the jitter. The jitter has been measured to be of about 170 ps rms.

The lock-in time and the bandwidth of the PLL have also been measured to test their dynamic behavior. The lock-in range result is about 15 μs and the bandwidth 100 kHz.

TABLE I
RESULTS SUMMARY

Max. Sampling rate	160 MHz
Voltage Supply	5 V $\pm$ 10%
Power consumption	25 mW (full rate,full load)
Jitter	170 ps rms
Sampling period max. deviation	0.5%
Chip Area	1 mm^2
Technology	1.2 μm BiCMOS
Max. load per phase	1.2 pF
PLL acquisition time	15 μs
PLL bandwidth	100 kHz

V. CONCLUSIONS

A clock generator for a double-sampled SC filter has been presented. The system is based on a PLL circuit that multiplies an external reference clock by a factor of eight. A key feature of this design is that the running frequency of the VCO is the same as that of each nonoverlapping clocking phase. Experimental results testify that a constant sampling period can be obtained thanks to the proposed strategy for the phase generation. The experimental results are summarized in Table I.

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