A Temperature Sensor with Single Resistor Set-Point Programming

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Abstract— **An integrated circuit set point temperature controller has an open collector output which switches low at a temperature determined by an external resistor. The programming resistor may be determined from a universal formula relating resistance to desired trip temperature. The circuit is laser trimmed at a single temperature in manufacture to conform with the formula to better than 1°C over a range between −40°C and 150°C. The circuit is low cost and includes temperature hysteresis, for well defined switching, and an optional output pull-up resistor.**

I. Introduction

TEMPERATURE set-point switches are used in applications from electric irons to industrial controls. A monolithic circuit combining simplicity with user programmability is ideal for many PC board applications such as over-temperature warning, cooling control, warranty verification, and u-P clock speed control. Small size facilitates sensor applications off the PC board, such as automotive cooling fan control and process sampling control functions.

Fig. 1 illustrates the function of the circuit described below. A single power supply and a programming resistor suffice to cause the circuit to switch its output from high to low as the die temperature reaches a selected value. Built-in hysteresis stabilizes the switching point against electrical and thermal noise. An optional on-chip pull-up resistor can be connected as a load for the open collector output.

The temperature sensitivity of silicon IC's is well known, both as a problem and as a feature in a variety of temperature sensing circuits. Circuits which switch at a critical temperature have been used to protect power IC's from overload. The challenge for this design was to develop a low cost circuit that could be programmed using a single resistor selected by the user with a universal expression for resistance versus trip temperature. A part of this challenge was to devise the circuit so that it could be calibrated by trimming on-chip SiCr thin-film resistors at a single temperature to match this expression over a wide range of temperature.

II. Overview

Temperature measurement IC's often use the temperature proportional "delta-V_{BE}" which results from operating similar bipolar transistors at different current densities [1]. This

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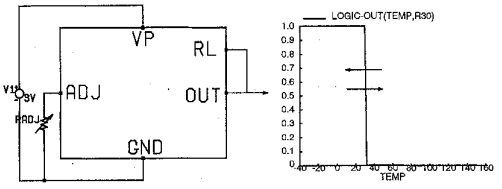

Function

OUT Switches Low As Die Reaches Temperature Set By Resistance Of R_{ADJ}

Applications

- **Temperature Set-Point Controller/Thermostat**
- **Over/Under Temperature Alarm**
- **Warranty Verification**
- **Clock Speed Controller**

Fig. 1. Basic operation of the IC.

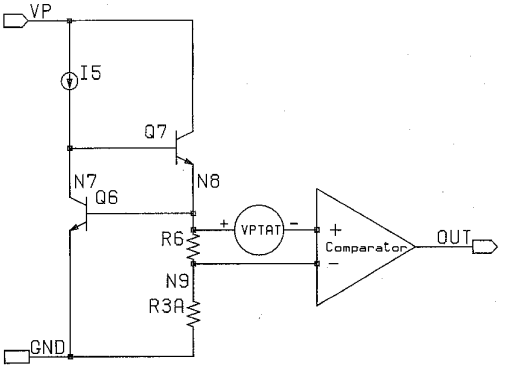

Fig. 2. Circuit functions of the IC.

voltage extrapolates to zero at zero Kelvin and is a reliably reproducible measure of die temperature [2]. This voltage must be compared to a standard voltage or reference to determine the temperature. For set point operation, it could be compared to, for example, the output of a band-gap reference voltage [3]. This voltage is the sum of a voltage proportional to delta-V_{BE} and another voltage proportional to V_{BE}. The delta-V_{BE} voltage is sometimes referred to as proportional-to-absolute temperature (PTAT). In the same context, V_{BE} is often referred to as the complementary-to-absolute temperature (CTAT), since its approximately linear fall with increasing temperature complements the PTAT voltage to produce the temperature invariant band-gap voltage. Since comparing the

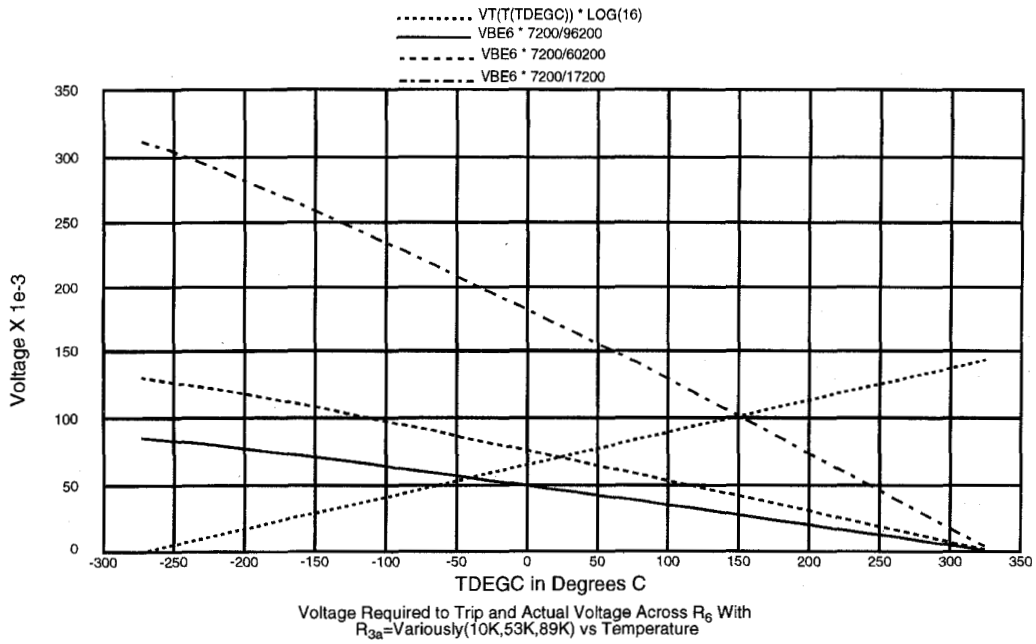

Fig. 3. Equalizing PTAT voltage to various fractions of the CTAT voltage.

PTAT voltage to a band-gap essentially takes the difference between a PTAT voltage and a voltage which is the sum of a PTAT and CTAT voltage, it seems expedient to just compare the PTAT and CTAT voltages directly to derive a signal which passes through zero at a selected temperature [4]. While this eliminates the opportunity to trim the band-gap voltage independently, as part of the calibration, it also eliminates the need to do so, along with considerable circuitry if an alternative calibration method can be found.

The circuit of Fig. 2 illustrates how a PTAT and CTAT signal can be compared to produce an output that switches high to low as the die is raised beyond some temperature. Bias current I_5 is forced in Q_6 by Q_7 which establishes the necessary base voltage on Q_6. In so doing, it also drives the voltage divider consisting of R_6 and R_{3a}. These resistors present a fraction of the V_{BE} of Q_6 to a comparator circuit. The comparator is made to have a PTAT offset voltage as represented by the VPTAT symbol.

At low temperatures, where $V_{\mathrm{BE}(6)}$ is large and VPTAT is relatively small, the comparator is driven positive at its input and its output will be high. As temperature increases, however, V_{BE6} will fall, while VPTAT will increase. If the ratio of R_6 and R_{3a} is suitably chosen, the comparator input voltage will pass through zero at some temperature and the comparator output will change from high to low.

Fig. 3 shows a simulation of a PTAT voltage which might be produced by a current density ratio of 16 compared to voltages which might be developed across R_6 when it is 7.2 KΩ for various values of R_{3a}. When R_{3a} is 10 KΩ, the PTAT voltage will equal the fraction of V_{BE6} across R_6 at about 150°C [5]. That means the output of the circuit of Fig. 2 will switch at about 150°C. Similarly, values of 53 KΩ and 89 KΩ for R_{3a} correspond to switching at room temperature and −55°C respectively.

III. Circuit Implementation

Fig. 4 is a schematic diagram of the entire IC and includes the supply voltage source $V1$ and the external programming resistor R_a. Biasing circuits operate Q_5 and Q_8 to produce currents I_5 and I_8, and Q_{12} drives an inverting output buffer. Combining R_3 with R_a, these features and others with similar identification can be recognized in Fig. 5, a simplified drawing of the core circuitry.

A. Temperature Sensing Core

In Fig. 5, I_5, Q_6, and Q_7 operate as in Fig. 2 to establish the V_{BE} of Q_6 at a nominal value. The voltage divider provides the base bias for Q_9 which has I_8 available as collector current. At low temperatures, however, most of this current is diverted to the base of Q_{12}, causing it to be on and to drive its load.

The way the comparator function is achieved can be seen by noting that the emitters of Q_6 and Q_9 are connected, so that the difference in their base voltages operates them as a differential pair, albeit one with no common mode compliance. If Q_6 and Q_9 were the same size and I_8 was equal to I_5, the collector currents should balance and Q_9 should just conduct all of I_8 when the base voltages were equal. These things are not the case, however, since Q_9 is larger than Q_6 by factor eight and I_8 is smaller than I_5 by factor two, set by the bias circuitry. As a result, the equilibrium condition where Q_9 just conducts all of I_8 will occur when the two base voltages differ in the amount

$$\Delta V_{\mathrm{BE}} = \frac{kT}{q} \cdot \ln\left(\frac{ni_5}{i_8}\right) \tag{1}$$

where n is the emitter area ratio; 8 in the actual circuit. This quantity is the VT of the Fig. 3 simulation. The equation expresses the voltage across R_6 required to cause Q_9 to just take the last of I_8 away from the base of Q_{12}. However, the

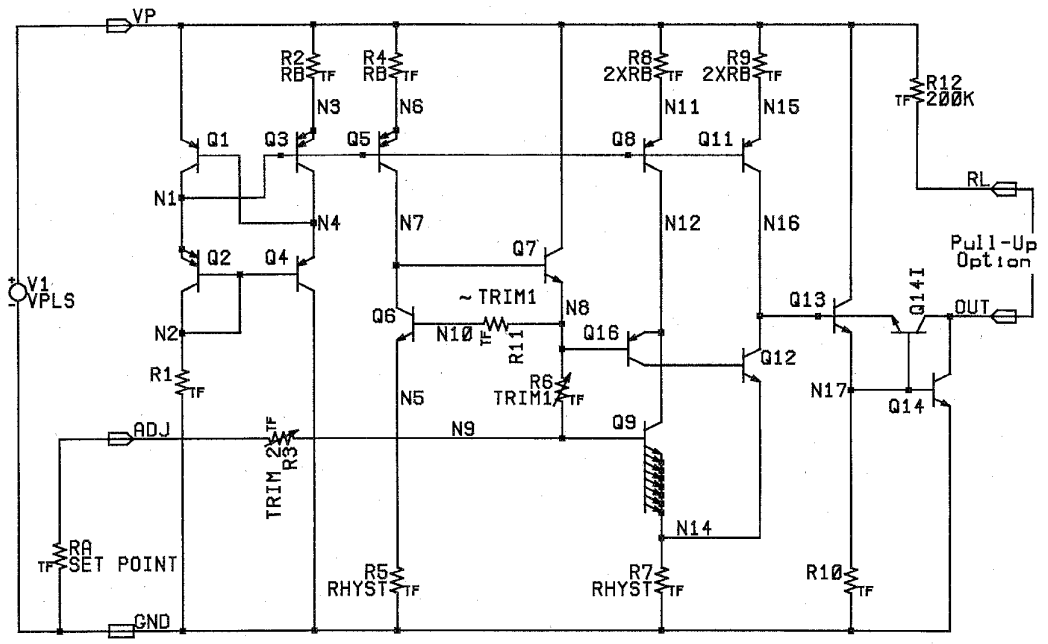

Fig. 4. Complete schematic diagram with power supply and programming resistor.

actual voltage across R_6 is a fraction of the $V_{\rm BE}$ of Q_6 so that this condition depends on the ratio of the resistors and the temperature. It will be analytically convenient to express the R_6 voltage as a function of the $V_{\rm BE}$ of Q_9, and since the two $V_{\rm BE}$'s will differ by $\Delta V_{\rm BE}$ at the trip temperature, this will be easy to do there. At all temperatures T we can express $V_{\rm BE(9)}$ as [6]

$$V_{\rm BE(9)} = V_{G0} - \frac{T(V_{G0} - V_{\rm BE0(9)})}{T_0} + \frac{kT}{q}\ln\frac{i_c}{i_0} + \frac{mkT}{q}\ln\frac{T_0}{T} \tag{2}$$

where V_{G0} is the band-gap voltage extrapolated to zero K, T_0 is a more convenient temperature for measurements, $V_{\rm BE0(9)}$ is the $V_{\rm BE}$ of Q_9 at this temperature when operated with i_0 in the collector, i_c is the present operating current, m is the "curvature constant" and k and q are Boltzman's constant and electron charge, respectively.

Neglecting base currents, the $V_{\rm BE}$ of Q_9 divided by R_{3a} should give the current in R_6 as well, so that at the trip temperature we can assert

$$\frac{R_{3a}}{R_6}\left(\frac{kT}{q}\right)\ln\frac{ni_5}{i_8} = V_{G0} - \frac{T(V_{G0} - V_{\rm BE0(9)})}{T_0} + \frac{kT}{q}\ln\frac{i_8}{i_0} + \frac{mkT}{q}\ln\frac{T_0}{T} \tag{3}$$

by equating (1) to (2) multiplied by the resistor ratio, and rearranging. Note that i_8 is PTAT so that i_0T/T_0 can be substituted for i_8 on the right side of the equation, allowing the last two terms to be combined. After this change, (3) can be rearranged to give

$$R_{3a} = R_6\left(\frac{q}{k\ln\frac{ni_5}{i_8}}\right) \times \left(\frac{V_{G0}}{T} - \frac{(V_{G0} - V_{\rm BE0(9)})}{T_0} + \frac{(m-1)k}{q}\ln\frac{T_0}{T}\right). \tag{4}$$

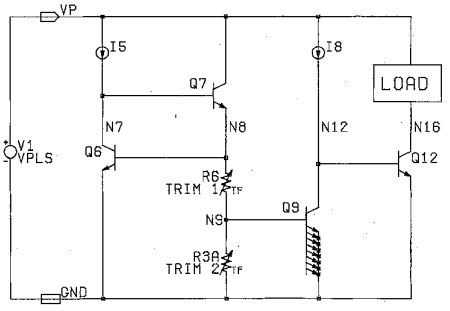

Fig. 5. Simplified core diagram.

This expression for R_{3a} shows that the value which causes the circuit to trip at a given temperature is proportional to R_6. This means that the absolute value of R_6 can be adjusted by trimming so that R_{3a} can be scaled to a particular value, despite some difference of the on-chip resistors from unit to unit.

The factor following R_6 in (4) is intended to be a constant. In practice, however, there may be some variation of the ratio of i_5 to i_8 which ideally is two, and the area ratio factor n which ideally is eight. Adjusting R_6 can clearly correct for manufacturing variation in this factor as well.

The third factor of (4) contains the temperature sensitivity which is desired for the programming function. Unfortunately, in addition to a number of known constants, it also contains $V_{\rm BE0(9)}$ within a term. This means that an equation for R_{3a} as a function of temperature will depend on the manufacturing variable $V_{\rm BE0(9)}$ so that a universal equation cannot be used for it, despite normalization by R_6.

To overcome this problem, the resistor can be divided into two pieces, thus

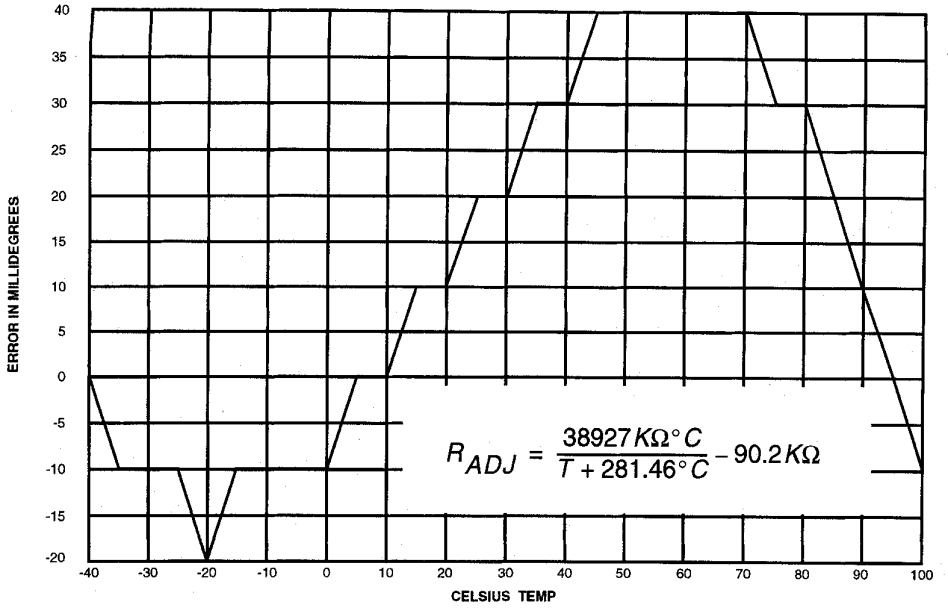

Fig. 6. Simulated trip temperature error, using calculated R_a values.

set

$$R_{3a} = R'_3 + R'_a \tag{5}$$

where

$$R'_3 = -\frac{R_6 q}{k \ln(ni_5/i_8)} \left(\frac{V_{G(0)} - V_{\mathrm{BE0(9)}}}{T_0} \right) \tag{6}$$

and

$$R'_a = \frac{R_6 q}{k \ln(ni_5/i_8)} \left(\frac{V_{G0}}{T} + \frac{(m-1)k}{q} \ln \frac{T_0}{T} \right). \tag{7}$$

The first of these resistances contains the $V_{\mathrm{BE0(9)}}$ term, along with a collection of constants and the R_6 factor, but is independent of temperature. The other resistance contains all the temperature dependent terms, along with another collection of constants and the R_6 normalizing factor. Note that the form of this second expression (7) is such that it can be made the basis of a universal formula for R_a versus desired trip temperature. Assuming that the value of m is invariant for a given process, and that T_0 can be fixed by choice, the second factor is a temperature function which is independent of any of the manufacturing variables and can be accurately predicted. The first factor consists of constants and factors selected for nominal value along with the R_6 factor which can be trimmed to normalize the value of the expression at a single temperature.

The second temperature dependent factor in (7) contains a logarithmic function of temperature; its second term. This term is the same one that appears in the analysis of the bandgap reference, where it constitutes an error from perfect temperature invariance. In the case of (7) it is not actually an error, since to the extent that m is invariant, the term is a strict function of temperature so that it can be part of the desired universal equation. It is, however, a complication that would be desirable to eliminate for computational convenience. Fortunately, this term is relatively small and has a more-or-less simple form. It is a simple convex curve which looks vaguely hyperbolic. The first term of this factor, V_{G0}, is hyperbolic in T, so that the possibility to approximate the second term by an adjustment of the first presents itself.

A second issue in this decomposition of R_{3a} is that the R'_3 portion given by (6) is intrinsically negative. While mathematically minor, that is a serious practical inconvenience. The simple expedient of adding and subtracting the same value to R'_3 and from R'_a, respectively, leaves their sum unchanged, but yields two new variables, both of which can be positive. Adding R_x to R'_3 and subtracting R_x from R'_a to give unprimed variables yields

$$R_3 = R_x - \frac{R_6 q}{k \ln(ni_5/i_8)} \left(\frac{V_{G0} - V_{\mathrm{BE0(9)}}}{T_0} \right) \tag{8}$$

and

$$R_a \cong \frac{R_6 q}{k \ln(ni_5/i_8)} \left(\frac{V_{G0}}{T + T_x} \right) - R_x. \tag{9}$$

The first of these transformations is exact, while the second approximately satisfies (5). The approximation consists of omission of the logarithmic term and the addition of T_x, an offsetting temperature constant. This simplifies the universal formula and contributes only a small error, as will become apparent.

These new values are the ones used to make the circuit and to determine the programming resistance. The diagram of Fig. 4 shows R_3 as an on-chip resistor, while R_a becomes the external programming resistor.

Fig. 6 is a simulated result for the circuit of Fig. 4 using nominal values for the various parameters and resistor values. This figure was generated by calculating the values for the adjustment resistor at 5° intervals from −40°C to 100°C. The calculated value was used for R_a in a simulation around the

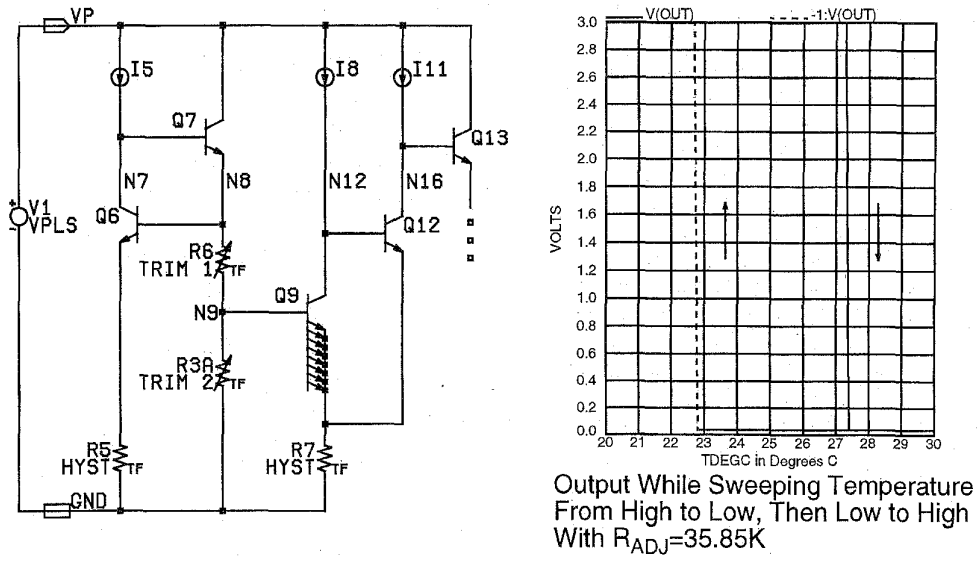

Fig. 7. Core functions including hysteresis and load driver.

nominal temperature to determine the actual (simulated) trip point. The difference from the calculated trip temperature was then plotted as a function of temperature. The conformance to the calculated curve is quite good, with an error less than the errors anticipated in the measurement and trim of the finished circuits. The third-order shape of the error curve is consistent with the approximation made to eliminate the logarithmic term. That is, the hyperbolic approximation would be expected to suppress the first- and second-order terms of the error expressed as a series, leaving a small residue dominated by the third and higher order terms.

B. Hysteresis Generation

Fig. 7 shows additional circuitry associated with the switching core of the circuit. The load on Q_{12} consists of a follower/driver transistor driven by a current i_{11}. This current is made equal to i_8, so that taken together i_8 and i_{11} equal i_5. Below the trip temperature i_8 flows into the base of Q_{12} turning it on. As a result, Q_{12} takes all of i_{11} at its collector, holding the base of Q_{13} low. Ideally both i_8 and i_{11} should be delivered by the emitter of Q_{12} to R_7, a resistor omitted from Fig. 5 to simplify it. A corresponding resistor R_5 in the emitter circuit of Q_6 will have most of i_5 flowing in it. The resistors R_5 and R_7 are made equal so that the voltage drop across R_5 caused by i_5 should equal the drop across R_7 due to the two currents i_8 and i_{11}. These currents and the resulting voltages are PTAT, and cause the base voltages of both Q_6 and Q_9 to be displaced by this PTAT amount. This voltage is qualitatively the same as the voltage which would result from a different operating current density in both devices or a different value of V_{BE0}. Since this voltage behaves the same as a change in the manufacturing variables, it does not disturb the conclusions of the analysis concerning trip temperature at or below this temperature. However, when the trip temperature is reached, Q_9 will divert i_8 from the base of Q_{12}, causing it to begin switching off. As current is diverted from Q_{12} toward the base of Q_{13}, the voltage drop across R_7 will be reduced. This will increase the base-emitter voltage applied to Q_9 causing it to increase its collector current. This will further reduce the drive to Q_{12}, which will drop the emitter voltage of Q_9 further causing a greater increase in collector current, driving Q_{12} further off.... This positive feedback causes the circuit to switch regeneratively as it reaches the trip temperature where Q_9 takes all of i_8.

Once the switching occurs and i_{11} is diverted to drive Q_{13}, the current in R_7 drops in half, resulting in a PTAT difference in the emitter voltages of Q_6 and Q_9. This is equivalent to a change in the PTAT voltage which is required across R_6 to cause Q_9 to be in equilibrium, with i_8 flowing in its collector. In order for the base-emitter voltage of Q_9 to fall so that it will release some of i_8 and turn Q_{12} back on, the voltage across R_6 must increase. This will happen when the temperature falls by a small but controlled amount. When it does, Q_9 will reduce its collector current so that Q_{12} will get some base drive. The resulting collector current will be conveyed to R_7, causing the emitter voltage of Q_9 to rise, further reducing the collector current of Q_9 and precipitating regenerative switching; this time from on to off.

The plot shown in Fig. 7 is a simulated output signal as temperature is swept from low to high and then (in the -1 plot) from high to low.

Temperature changes frequently occur very slowly, and this regenerative action insures an abrupt and well defined event at the circuit output, when the preset temperature is reached. A small (about 4.5°C) hysteresis insures that the circuit output will not dither due to small fluctuations around the critical temperature. The magnitude of the hysteresis is set by the ratio of R_5 and R_7 to resistances in the bias circuit and is readily adjustable at the mask level, but is not a trimmed parameter.

C. PTAT Biasing

A requirement of the circuit core is for dependable PTAT biasing. The important ratios discussed above are achieved by driving ratio-matched sets of transistors and resistors from

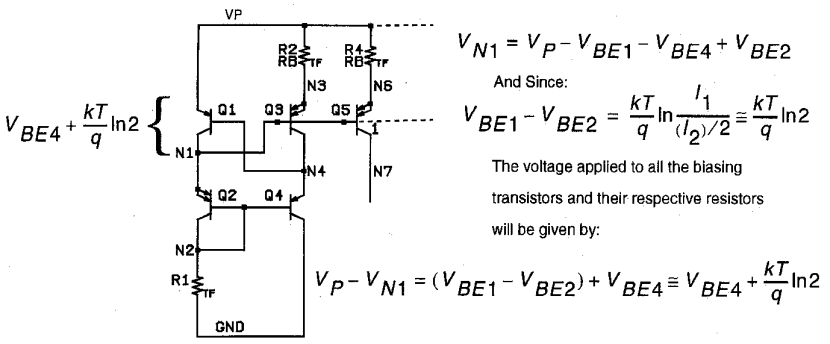

Fig. 8. Alternative analysis of PTAT bias generator.

a common source. Fig. 8 shows the bias circuitry used to control these transistors and produce a PTAT current in them. The cross-connected quad of transistors Q_1 through Q_4 is frequently used to produce a PTAT bias current [7]. The usual analysis indicates that the voltage across R_2 is PTAT and is governed solely by the area ratios of transistors in the circuit. The current in R_2 and Q_3 should also be PTAT so that replica bias circuits like Q_5-R_4 in the figure, as well as others shown in the full schematic, will produce images of this current. To the extent that base currents can be neglected, this result is independent of the excitation current, provided in this example by R_1.

An objective of the design of this circuit was to achieve low voltage operation, but with good supply voltage rejection in the temperature threshold. The magnitudes of the PTAT bias currents directly affect the temperature trip points, and while the effect of their initial values vanishes in the trim calibration, variation with supply voltage will result in errors. Cascoding the bias generator and replica current sources would keep them relatively unaffected by supply voltage. However, the headroom required by the cascodes would directly add to the minimum operating supply voltage of the part, so this solution is undesirable.

The usual analysis neglects the effect of supply voltage variation on Q_4 as compared to Q_3 which does not "see" these variations. Usually this problem is minimized by cascoding Q_4, and in many circuits the cascode current is used for biasing in addition to any replicas which may be used. In this circuit, however, low voltage operation would be compromised by a cascode for Q_4.

An alternative analysis of the circuit, shown in Fig. 8, helps to make clear a method of converting this bug to a feature. As the analysis shows, the voltage at node $N1$, applied to both Q_3 and the replica transistors, is equal to the $V_{\rm BE}$ of Q_4 (a similar voltage can also be obtained with other feedback current sources, such as the improved Wilson mirror, to achieve the same end described here). This means that as the supply voltage changes and the $V_{\rm BE}$'s of the replica transistors are changed by the Early effect, the $V_{\rm BE}$ of Q_4 will be modified in the same way. Since the replica transistors are driven by a voltage which includes $V_{\rm BE4}$, their control voltage will be compensated almost exactly for changes in supply voltage. While this arrangement does not actually raise the output impedance of the current sources (which might be more important in a high gain amplifier) it very effectively reduces output current variation due to supply voltage changes.

A further complication of this circuit is that in correcting for the base width modulation of the replica transistors it also applies the compensation to Q_3 which does not "see" supply voltage changes and does not need compensation. At first it appears that this might be quite undesirable, since it modifies the voltage at $N3$ causing the actual current in Q_4 to be reduced with increasing supply voltage (and yes, the output impedance from Q_4 is negative, another interesting and variously useful/vexing property of this circuit). One more neglected detail is that base width modulation of the replica transistors also changes their beta and their base current, which should result in a small increase in collector current with increasing supply voltage. This change is counteracted by the change in voltage at $N3$, so that this simple arrangement actually provides quite outstanding performance. The consequences are that the silicon typically exhibits less than 0.1°C/V change in trip temperature versus power supply voltage change.

Operating current for the whole device has a small power supply voltage dependence, due to R_1, and also depends on the programming resistor, increasing for higher trip temperature settings. It is in the range of 60 μA to 100 μA for most common conditions, so that self-heating errors can usually be neglected.

D. Other Circuit Details

Referring again to Fig. 4, the remaining circuit features will be described. In the hysteresis diagram Q_{12} was seen to drive Q_{13}, which can be seen as an emitter follower driving an output transistor, Q_{14}, in the complete schematic diagram. When Q_{12} switches off at the trip temperature, i_{11} from Q_{11} is diverted into Q_{13}'s base and it drives Q_{14} to pull down the output load. It is important to have enough drive to Q_{14} so that it can drive loads greater than the on-board pull-up resistor.

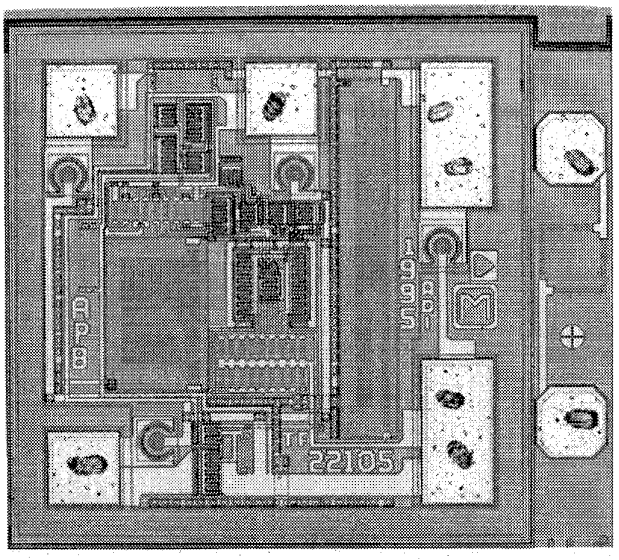

Fig. 9. Photo of the monolithic set point sensor.

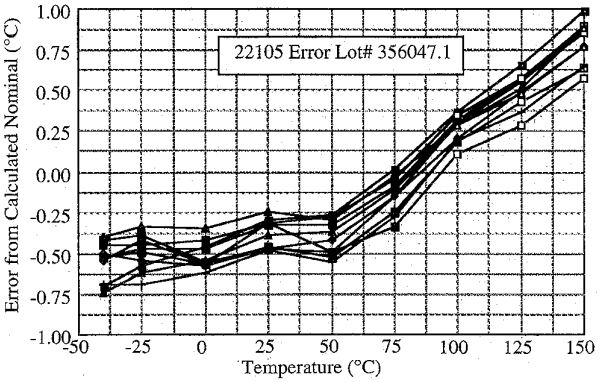

Fig. 10. First trim lot error measurement: Trip temperature versus calculated R_a.

On the other hand, it is undesirable to allow Q_{13} to operate at beta $\times$ i_{11} whenever the output switches. An extra emitter on Q_{14}, indicated on the diagram as $Q_{14}I$, is used as an inverted collector to detect when Q_{14} saturates and divert excess drive away from the base of Q_{13}.

Transistor Q_{16}, not shown on the simplified diagrams, conveys i_8 to the base of Q_{12}. The V_{BE} of Q_{16} allows the collector voltage of Q_9 to rise, so that it more nearly approximates the collector voltage of Q_6. This helps to maintain the precision of the ΔV_{BE} function that sets the trip temperature.

Base current from Q_9 flowing in R_6 adds to the voltage across it and would produce an error if it were not compensated by R_{11} carrying the base current of Q_6. An equal voltage drop results, which displaces node $N8$ and leaves the two bases at the correct voltage.

Finally, another potential error is simply cancelled in a subtle way. The base current of Q_7 subtracts from i_5 current intended for Q_6. In an operating circuit with a given programming resistor, this current is clearly the ratio of beta and the CTAT current developed in R_{3a}. However, examining this current at the trip temperature as the adjustment resistor is swept shows the current is PTAT when plotted only versus trip temperature. This may be made more apparent by noting that the voltage across R_6 must equal some PTAT voltage as a function of trip temperature, and the current in Q_7 is proportional to this current. Therefore, scaling the resistance level of R_a so that the emitter current of Q_7 at the trip temperature is twice i_8 and i_{11} insures that the proportion of current taken from i_5 by Q_7 is the same as the proportion of i_8 taken by the base of Q_{12}. This happens only at the trip temperature, but of course that is the only place the error would appear, if uncorrected.

IV. Technology

The circuit is fabricated in a complementary bipolar dielectrically isolated process. This process was selected for its small device size (1 μM $\times$ 1 μM minimum emitter) and excellent complementary devices. Incidentally, its inherent speed makes this circuit probably the world's fastest thermostat.

An almost identical circuit has also been incorporated as a subcircuit of a more complex chip on a junction isolated process. The behavior of that silicon and conformance to the resistance formula is very similar.

Fig. 9 shows the die layout, dominated by the two trim resistors. The shorter resistor to the left is R_6 and the other, longer, resistor is R_3. Some space was sacrificed to permit the use of large beam lasers for trimming, adding to flexibility in manufacturing. At the extreme right is a trim alignment target placed off-chip in the scribe grid to reduce the size of finished dice to 35 μM $\times$ 36 μM.

V. Thin Film Trimming

Since the circuit must be made to work with a single external resistor of known value, an adjustment is required to correct for lot-to-lot variation in thin film sheet resistance as well as the parameters noted analytically above. Typically, this is the largest factor in the range of trim required.

Finished wafers are probed, and the device temperature is accurately determined. The programming conditions for that temperature are emulated, and R_6 is laser-trimmed so that the circuit trips at the test temperature. This adjusts for the sheet resistance of thin film resistors on the die and for individual variation in the current density ratio ni_5/i_8.

Next, R_3 is trimmed so that the value of external resistance, R_a, calculated from the universal formula, just causes the circuit to trip at the known die temperature. Because the circuit is arranged to make the formula for R_a independent of individual device characteristics, trimming out the individual variations in this way, so that the universal formula fits at a known temperature, should make it fit at all temperatures.

VI. Temperature Measurement Results

Using the formula from Fig. 6, the parameters for a trim algorithm were estimated. The results of using these param-

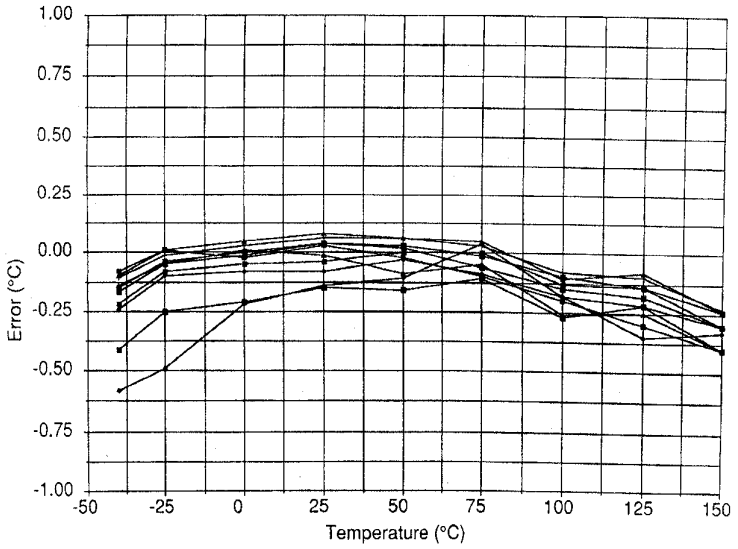

Fig. 11. Sample error measurement after trim parameter adjust: Trip temperature versus calculated R_a.

eters to trim the first wafer lot of the circuit are shown in Fig. 10. Using these results to incrementally adjust the trim program and simultaneously modify the universal formula to obtain more "round" values, we achieved the results shown in Fig. 11. These figures are similar to Fig. 6 in that they show the actual error at individual temperatures (measured using a liquid bath) compared to the temperature corresponding to the programming resistance.

Errors associated with wafer temperature measurement, electrical stimulation at trim, subsequent processing to the packaged devices, and DUT measurement error are indicated by the distribution around 25°C. Departures from this value at other temperatures indicate the error associated with the balance between the two trims, trip temperature measurement error, and failure of an individual device to conform to ideal behavior.

VII. Conclusion

A simple integrated circuit and a method for trimming it at a single temperature have been devised, fabricated, and tested. The circuit can be programmed as a set-point controller over a wide range of temperature using a single external resistance, determined from a universal formula. Devices trimmed at room temperature conform to the formula to better than 1°C over a range from −40°C to 150°C. It can be operated from supply voltages between 2 V and 10 V with less than 0.1°C/V error. The typical operating current is less than 100 μA so the circuit is suitable for portable as well as instrumentation applications.

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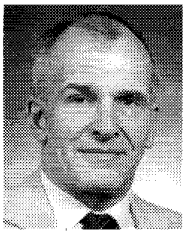

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