Brief Papers

Design of a One-Transistor-Cell Multiple-Valued CAM

Takahiro Hanyu, Naoki Kanagawa, and Michitaka Kameyama

Abstract— **A new high-density multiple-valued content-addressable memory (CAM) is proposed to perform highly parallel search operations in a limited chip area. The number of cells in the CAM is reduced by the use of multiple-valued data representation. Moreover, multiple-valued stored data correspond to the threshold voltage of a floating-gate MOS transistor, so that the cell circuit can be designed using only a single transistor. As a result, the cell area of the proposed four-valued CAM is reduced to 14% of that of a conventional dynamic binary CAM, and its performance is about 5.4-times higher than that of the corresponding binary one under a 0.8-μm standard EEPROM technology.**

I. Introduction

PARALLEL search and parallel comparison are major advantages of content-addressable memories (CAM's) over random access memories [1]. CAM's perform various operations in a word-parallel manner and many intelligent systems such as file maintenance, pattern recognition, and language translations have been designed as fine-grain systems [2]–[4]. These application fields generally require high computational power and large memory capacity at low cost. However, a CAM is more complex to build and has lower storage density than a conventional address-based memory because of the overhead involved in the storage, comparison, manipulation, and output-selection logic.

In this paper, a new high-performance CAM based on multiple-valued logic is proposed for high-speed word-parallel magnitude comparison. In the application to a collision-detection VLSI processor for intelligent vehicles, such magnitude comparison is utilized frequently [5]. The number of cells in the proposed CAM is reduced by the use of multiple-valued logic in comparison with that of a corresponding binary one [6], [7]. Consequently, the operating speed for digit-serial comparison is also improved as well as the chip density because the number of the comparison steps is reduced using multiple-valued logic.

To realize a high-density multiple-valued CAM cell, functionally separated configuration is introduced. Since the cell functions in the CAM are divided into a logic-value conversion for input data and two threshold functions perform in each cell, a conventional multiple-valued CAM cell circuit has been realized by using two floating-gate MOS transistors with different thresholds, respectively [8]. In the proposed CAM cell, two threshold functions for one-digit comparison are performed serially in the same cell, so that the cell circuit can be implemented using only a single floating-gate MOS transistor. Moreover, for high-speed digit-serial comparison, multiple-valued threshold functions performed in different cells are overlapped using two match lines in each word without area penalty. As a result, the cell area of the proposed multiple-valued CAM is reduced to 14% in comparison with that of a conventional dynamic binary CAM, and performance becomes 5.4 times higher than that of the binary one [9].

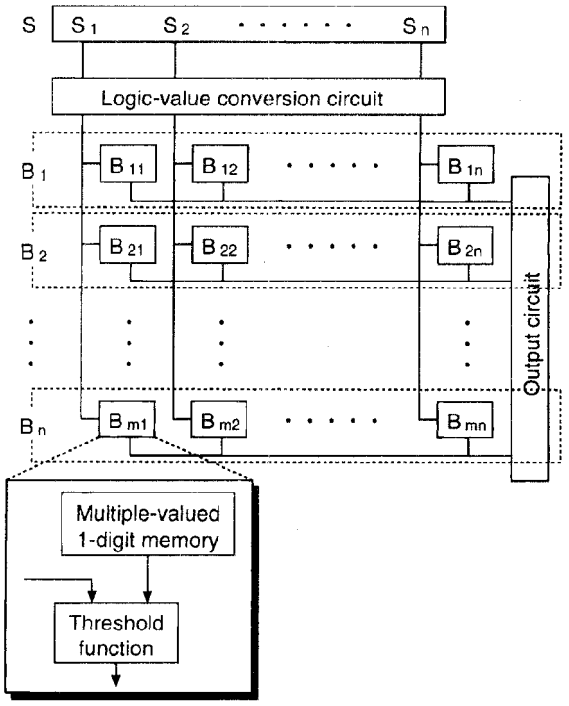

Fig. 1. Block diagram of a multiple-valued CAM.

II. Hardware Algorithm for a Multiple-Valued CAM

Fig. 1 shows a block diagram of a multiple-valued CAM. In the case of R-valued encoding, an input word S and the ith stored word $B_i (1 \leq i \leq m)$ are expressed as follows:

$$S = \sum_{j=1}^{n} R^{n-j} \cdot S_j \tag{1}$$

$$B_i = \sum_{j=1}^{n} R^{n-j} \cdot B_{ij} \tag{2}$$

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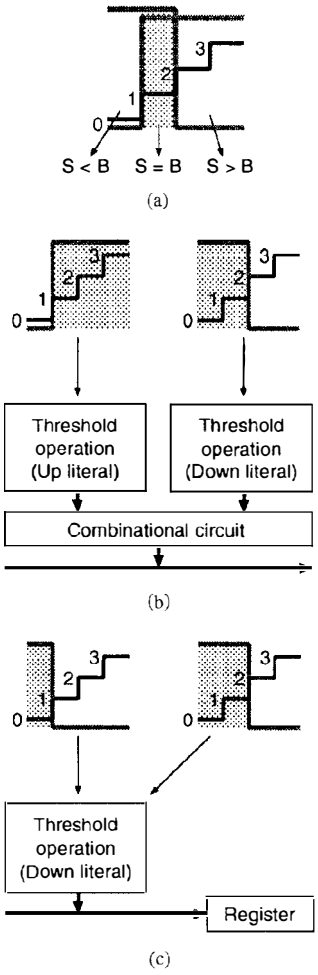


Fig. 2. Cell for four-valued one-digit comparison. (a) Principle of one-digit comparison. (b) Cell with two threshold elements. (c) Cell with one threshold element.

where S_j and $B_{ij}(1 \leq j \leq n)$ indicate the jth digits of S and B_i, respectively, and $S_j, B_{ij} \in \{0, 1, \cdots, R-1\}$. S_1 and B_{i1} are the most significant digits, and S_n and B_{in} are the least significant digits, respectively.

Several complicated search operations are performed by the combination of two basic functions: a threshold function and a logic-value conversion. Using two multiple-valued input signals, x and y, the threshold function $g(x, y)$ is represented as

$$g(x,y) = \begin{cases} R-1 & \text{if } x + y \leq R-1, \\ 0 & \text{if } x + y > R-1 \end{cases} \tag{3}$$

where the symbol "+" indicates an arithmetic addition.

The logic-value conversion is a one-variable function which is represented by $f = \langle p_0, p_1, \cdots, p_{R-1} \rangle$ as

$$f(s) = \begin{cases} p_0 & \text{if } s = 0 \\ p_1 & \text{if } s = 1 \\ \vdots & \vdots \\ p_{R-1} & \text{if } s = R-1 \end{cases} \tag{4}$$

where $p_i (0 \leq i \leq R-1) \in \{0, 1, \cdots, R-1, R\}$ and $s \in \{0, 1, \cdots, R-1\}$.

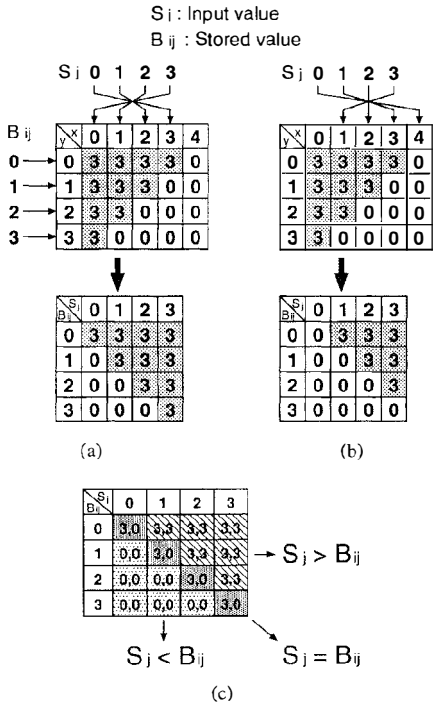


Fig. 3. Principle of four-valued one-digit comparison. (a) Step 1. (b) Step 2. (c) Comparison result.

In multiple-valued one-digit comparison, two threshold operations must be performed in a single CAM cell as shown in Fig. 2(a). If these functions are directly performed in a cell, two threshold elements and a circuit to combine their outputs are provided as shown in Fig. 2(b). On the other hand, only a single threshold element is effectively utilized in the proposed cell circuit as shown in Fig. 2(c). A multiple-valued input value is permuted serially by two different logic-value conversions and these outputs are transferred to the cells in the corresponding column of the CAM array. Therefore, two threshold operations are performed serially in each CAM cell. One-digit comparison is performed by the accumulation of the results from these two threshold operations.

For example, let us discuss a four-valued one-digit comparison scheme shown in Fig. 3. Assume that the jth input digit S_j be "2" and the jth stored digit B_{ij} in the ith word be "2." When S_j is first permuted by the logic-value conversion $f_a = \langle 3, 2, 1, 0 \rangle$, the output of f_a becomes "1." Then, the output of the threshold operation becomes "3" as shown in Fig. 3(a).

Similarly, when S_j is permuted by the logic-value conversion $f_b = \langle 4, 3, 2, 1 \rangle$, its output still remains "2." Then, the output of the threshold operation becomes "0" instead of "3" as shown in Fig. 3(b). From the combination of the above two outputs shown in Fig. 3(c), you can see that S_j is equal to B_{ij}.

In general, the R-valued one-digit comparison is described by the following three steps where a stored value is memorized in advance.

Step 1: The logic-value conversion f_1 of the jth input digit S_j and the threshold function $g(x_1, y)$ are performed according

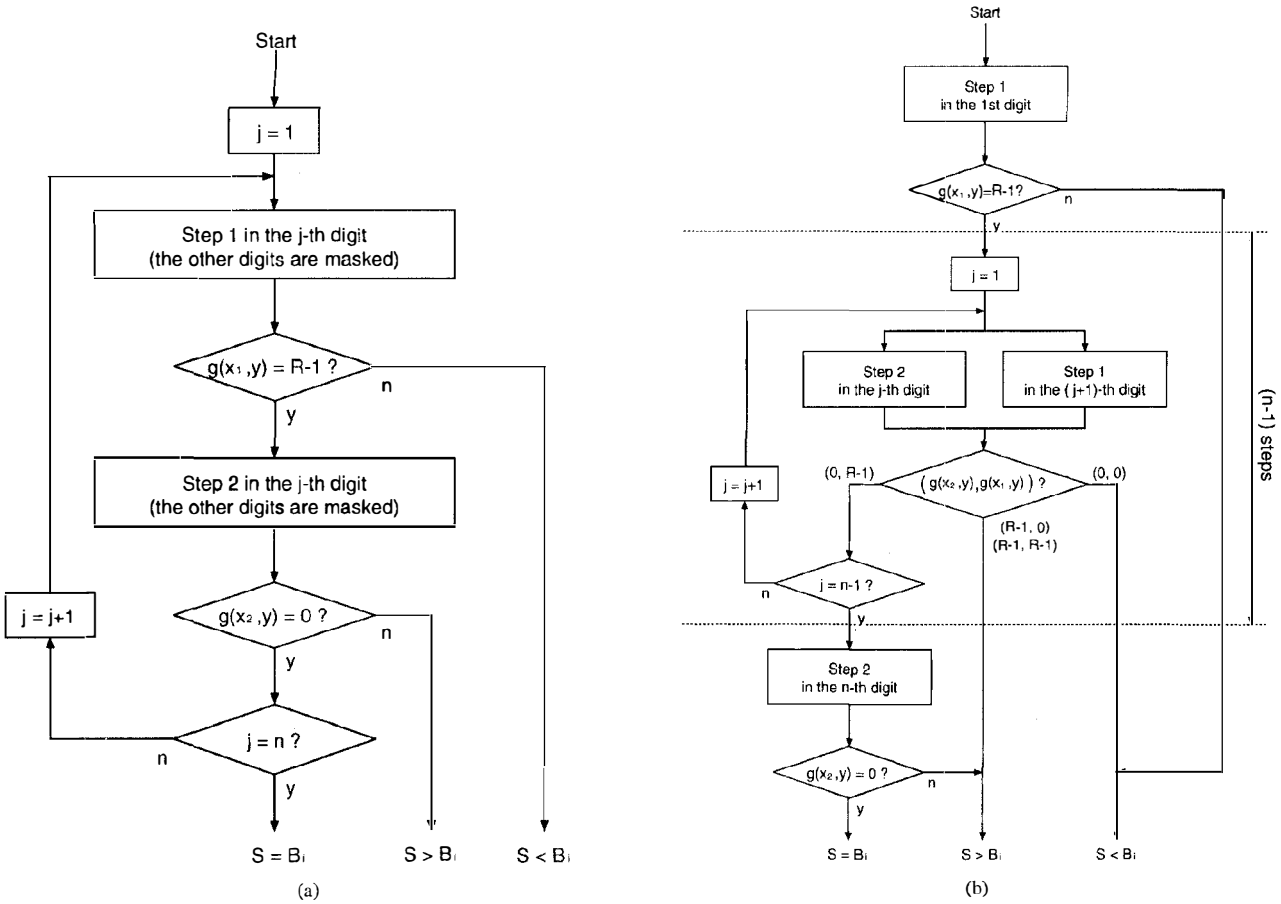


Fig. 4. Flow chart of one-word comparisons. (a) One-word comparison with $2n$ steps. (b) One-word comparison with $(n+1)$ steps.

to (5) as

$$g(x_1, y) = \begin{cases} R-1 & \text{if } S_j \geq B_{ij}, \\ 0 & \text{if } S_j < B_{ij} \end{cases} \tag{5}$$

where x_1 is the output from the logic-value conversion f_1 and $y = B_{ij}$, and f_1 is given in (6) as

$$f_1 = \langle R-1, R-2, \cdots, 1, 0 \rangle. \tag{6}$$

Step 2: The logic-value conversion f_2 of the jth input digit S_j and the threshold function $g(x_2, y)$ are performed according to (7) as

$$g(x_2, y) = \begin{cases} R-1 & \text{if } S_j > B_{ij}, \\ 0 & \text{if } S_j \leq B_{ij} \end{cases} \tag{7}$$

where x_2 is the output from the logic-value conversion f_2, and f_2 is given in (8) as

$$f_2 = \langle R, R-1, \cdots, 2, 1 \rangle. \tag{8}$$

Step 3: Result of one-digit comparison from Step 1 and Step 2 is interpreted as

$$\begin{aligned} &S_j < B_{ij} \text{ if } (g(x_1, y), g(x_2, y)) = (0, 0), \\ &S_j = B_{ij} \text{ if } (g(x_1, y), g(x_2, y)) = (R-1, 0), \\ &S_j > B_{ij} \text{ if } (g(x_1, y), g(x_2, y)) = (R-1, R-1). \end{aligned} \tag{9}$$

Using the above one-digit comparison scheme, one-word comparison can be performed in a digit-serial fashion as shown in Fig. 4. For the masked digit, the logic-value conversion f_{mask} of an input value is performed as

$$f_{\text{mask}} = \langle 0, 0, \cdots, 0, 0 \rangle. \tag{10}$$

In this comparison scheme, $2n$ threshold operations must be performed for an n-digit word as shown in Fig. 4(a).

On the other hand, if both Step 1 and Step 2 are performed simultaneously for the different digits, one-word comparison can be performed by $(n+1)$ steps in an n-digit word as shown in Fig. 4(b). As a result, the number of the comparison steps is reduced to about half compared with that of a simple iterative comparison scheme.

III. Design of a Multiple-Valued CAM

A. Design of a CAM Cell Circuit

The threshold element is realized using only a floating-gate MOS transistor as shown in Fig. 5. Since multiple-valued stored data are represented by the threshold voltage of a floating-gate MOS transistor, a threshold operation is performed by storing a multilevel charge on the floating gate of the transistor.

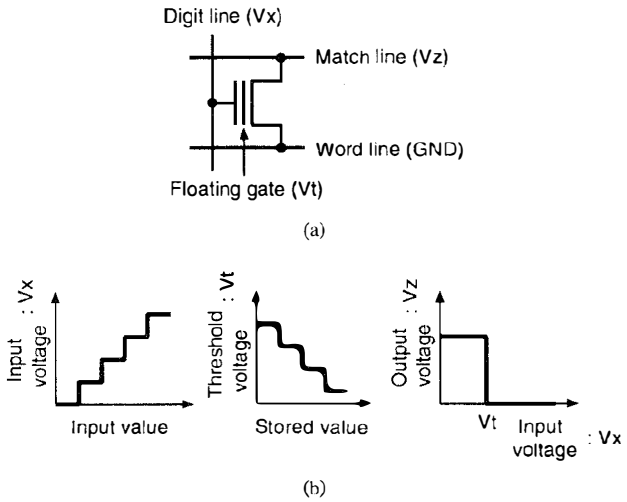


Fig. 5. Threshold element. (a) CAM cell circuit. (b) Relationship between logic values and voltage levels.

The match line is precharged to a high level. Then, the input voltage V_x is loaded to the digit line. When V_x is smaller than the threshold voltage V_t, the transistor still remains off. When V_{R-1} and V_y indicate a voltage corresponding to a threshold value of the threshold operation and a multiple-valued stored voltage, respectively, V_t is described as follows:

$$V_t = V_{R-1} - V_y. \tag{11}$$

If V_x is larger than V_t, the transistor turns on and the match line is discharged to a low level. Then, the following condition must be satisfied from (11) as

$$V_x - V_y > V_{R-1}. \tag{12}$$

In the case of an R-valued threshold operation, V_x, V_y, and V_{R-1} are generally given as

$$V_x = \frac{V_{dd}}{R-1} \cdot x, \tag{13}$$

$$V_y = \frac{V_{dd}}{R-1} \cdot y, \tag{14}$$

$$V_{R-1} = \frac{V_{dd}}{R-1} \cdot (R - 0.5) \tag{15}$$

where the symbols x and y are R-valued input and stored values, respectively, and V_{dd} is a supply voltage. From (11), (14), and (15), V_t is written as

$$V_t = \frac{V_{dd}}{R-1} \cdot (R - 0.5 - y). \tag{16}$$

In the case of four-valued encoding with $V_{dd} = 5(\mathrm{V})$, V_x and V_t are shown in Table I.

B. CAM Cell Operation

In the proposed CAM cell, we use the read/write operations of a conventional multiple-valued flash EEPROM [10]. Fig. 6 shows the circuit diagram for read/write operations in the CAM cell. In the initiate state before writing, the electric charge on the floating gate in every multiple-valued CAM cell is erased simultaneously during the erase operation as shown in Fig. 6(a). After the erase operation, the threshold voltage of every CAM cell transistor is set to 0.83(V) which indicates the logic value "3."

TABLE I
VOLTAGES CORRESPONDING TO LOGIC LEVELS

Input logic value	0	1	2	3	4
Input voltage Vx (V)	0.00	1.67	3.33	5.00	6.67

Stored logic value	0	1	2	3
Threshold voltage Vt (V)	5.83	4.17	2.50	0.83

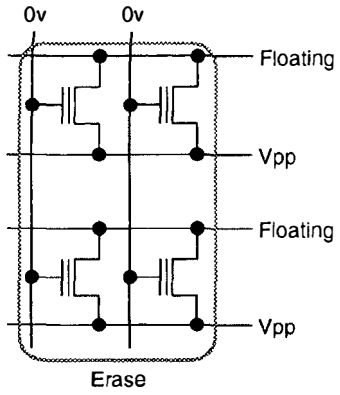
In the write operation, the threshold voltage V_t of the selected cell is programmed by the number of pulses with the adequate voltage level V_{pp}, which is loaded on the selected digit line as shown in Fig. 6(b). To avoid changing the threshold voltage of every nonselected cell, an intermediate voltage $V_{hs}(= 8(\mathrm{V}))$ is loaded on the corresponding digit lines, word lines, and match lines.

In the read operation, the staircase-pulse is loaded on the selected digit line as shown in Fig. 6(c). If the voltage on the digit line is higher than the threshold voltage of the selected cell transistor, the match line is discharged and the stored multiple-valued data in the selected cell is read out on the match line.

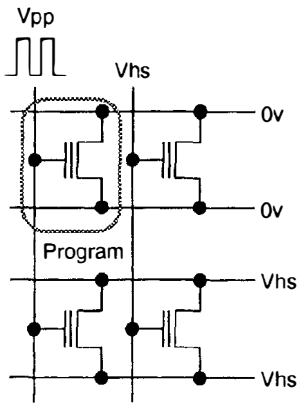
Fig. 7 shows characteristics of the cell in case of four-valued encoding experimented using discrete components. These waveforms indicate that the programming of the multiple threshold voltages of the floating-gate MOS transistors and the threshold operations can be precisely performed.

C. Design of a One-Word Circuit with Two Match Lines

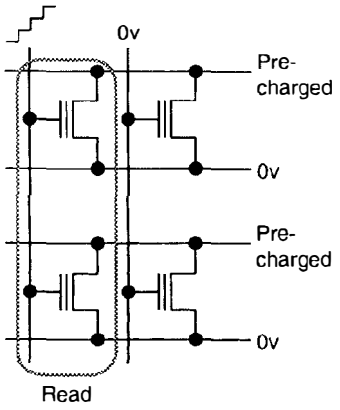
The use of two match lines improves the operating speed without area penalty in a one-word circuit. Figs. 8 and 9 show the block diagrams of one-word comparison circuits and their timing diagrams. In the case of a single-match-line circuit shown in Fig. 8(a), only a single threshold function is performed every time step, so that one-word comparison is executed in $2n$ steps for an n-digit word as shown in Fig. 9(a). For a high-speed operation, two match lines are used in the proposed circuit shown in Fig. 9(b). In this circuit, two threshold functions are performed simultaneously in a pair of different cells so that Step 2 of the jth digit $(1 \le j \le n-1)$ and Step 1 of the $(j+1)$th digit are performed in parallel as shown in Fig. 9(b). The output of each threshold function is transferred to one of the two match lines every time step, and the result of one-word comparison is stored in a temporary data register outside of the CAM cell array as shown in Table II. As a result, one-word comparison can be executed in just $(n+1)$ steps for an n-digit word. Fig. 10 shows the layout of the proposed CAM cell based on a standard 0.8-μm double-metal double-polysilicon technology. Although two match lines are used in each word, there is no hardware overhead in terms of the cell area. Therefore, the performance of the proposed CAM can be about two times higher than that of a CAM using a single match line.



(a)



(b)



(c)

Fig. 6. CAM cell operations. (a) Erase operation. (b) Write operation. (c) Read operation.

IV. Evaluation

Table III summarizes the comparison of performances in a conventional binary and the proposed CAM's using PSPICE simulation. Both the number of the cells and the execution steps for one-word comparison are reduced to half by using multiple-valued encoding. Moreover, the use of a floating-gate MOS transistor makes the cell area smaller, and makes the length of the match lines shorter, which results in higher access speed in each threshold operation than that of a conventional binary implementation. The new CAM cell based on a single transistor makes it possible to implement a high-density CAM using the same manufacturing process as that of conventional flash EEPROM's. As a result, the cell area of the four-valued CAM is reduced to 14% of that of a conventional dynamic binary CAM, and its performance is about 5.4 times higher

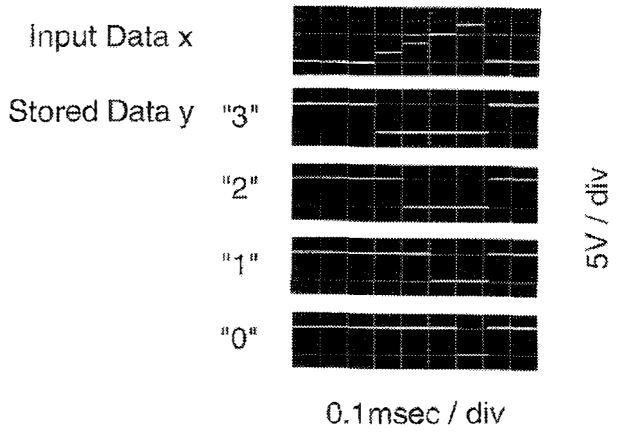


Fig. 7. Characteristics of an multiple-valued CAM cell.

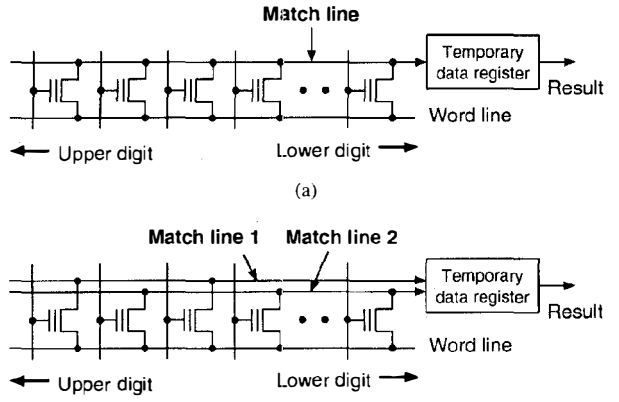


Fig. 8. One-word comparison circuits. (a) Single match-line circuit. (b) Double-match-line circuit.

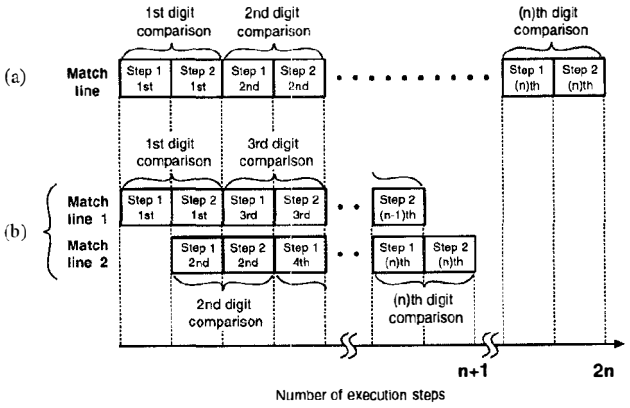


Fig. 9. Timing diagrams of one-word comparison. (a) Single-match-line circuit. (b) Double-match-line circuit.

TABLE II
RESULT OF ONE-WORD COMPARISON

Odd steps		Even steps		$\overline{\text{Large}}$	$\overline{\text{Small}}$	Result
ML 1	ML 2	ML 1	ML 2			
*	3	3	*	0	1	S > B
0	0	0	0	1	0	S < B
3	0	3	0	1	1	S = B (Intermediate)

* Don't Care

ML1 : Match line 1 S : Input word
ML2 : Match line 2 B : Stored word

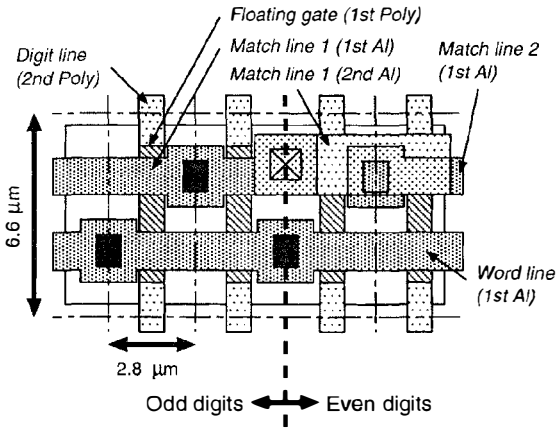


Fig. 10. Layout of the CAM cell.

TABLE III
COMPARISON OF CAM'S

	Binary	Proposed (4-valued)
Technology	0.8-μm CMOS Triple-polysilicon Double-metal	0.8-μm CMOS Double-polysilicon Double-metal
Cell area	132.0 μm^2 (2 cells)	18.48 μm^2
Access time	30.0 ns	10.7 ns
Number of execution steps (60-bit comparison)	60	31
Execution time (60-bit comparison)	1800 ns	331.7 ns
Dynamic power dissipation	0.19 mW/word (25 MHz)	0.078 mW/word (25 MHz)

(PSPICE simulation based on 0.8-μm CMOS technology)

than that of the corresponding binary one [9]. Fig. 11 shows the layout of 4 Mb four-valued CAM. The area of logic-value conversion circuits is less than 10% of the total chip area because a logic-value conversion circuit is shared by all one-word comparison circuits.

Not only four-valued data, but also higher radix data can be stored in each CAM cell. This property reduces the number of CAM cells and interconnections. In general, the number of CAM cells is reduced by a factor of $1/\log_2 R$ using R-valued encoding if the threshold voltage of the floating-gate MOS transistor can be precisely programmed by external signals.

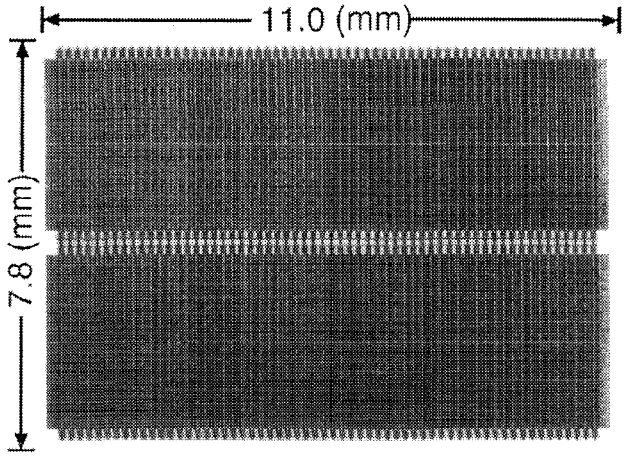


Fig. 11. Layout of the 4 Mb four-valued CAM.

V. CONCLUSIONS

A new high-density multiple-valued CAM based on one-transistor cell has been described. Several comparison operations are realized by the combination of two threshold operations performed serially in each cell. The proposed multiple-valued CAM cell is directly designed by using only a single floating-gate MOS transistor. To reduce the operation steps of one-word comparison, two match lines are used in each word without area penalty. These approaches make it possible to design a high-density CAM with high-speed operation capability.

In this paper, we have suggested the advantage of a multiple-valued CAM using the same technology of a conventional flash EEPROM. Such a high-performance CAM will be of great use in real-time applications for large-scale artificial intelligence systems.

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