CMOS Instrumentation Amplifier with Offset Cancellation Circuitry for Biomedical Application

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Abstract: - This paper presents the design and development of a CMOS Instrumentation Amplifier for biomedical application. This design manages to achieve 101dB gain, PSRR > 102dB and 91dB CMRR. The final circuit consumes total of 0.318μWatts power at 1.8V supply voltage and possesses die size of 9.6nm^2 area. It also has a full CMOS implementation of offset cancellation circuitry, among the first of its kind. Comparison with more complex work shows improved or comparable results.

Key-Words: - instrumentation amplifier, biomedical application, CMOS

1 Introduction

A biomedical instrumentation system usually consists of transducer, amplifier, and associated signal conditioning circuitry. The most sensitive element in the system are the input signals, like blood pressure, body temperature, pulse or heart beat rate. These signals are acquired and transformed into voltage signal with the amplitude of several milli-volt. Since the voltage signal is very low and very susceptible to noise, the amplifier playing an important role to amplify signals into significant value for signal processing. Instrumentation amplifier is very crucial in biomedical instrumentation system due to its high input impedance, and high common-mode rejection ratio to reject the unwanted signals [1]-[2].

An instrumentation amplifier is normally employed in portable and battery powered device. The development of CMOS instrumentation amplifiers is gaining popularity nowadays because of its low power requirement. CMOS transistor uses little power and does not produce as much heat as the traditional Biopolar Junction Transistor (BJT). Since the size of channel length of CMOS transistor is shrinking very significantly, it allows a high density of logic functions on a chip.

This paper illustrates the functionality of different modules of the instrumentation amplifier, followed by the integration of the blocks to make a full instrumentation amplifier. The design techniques applied in order to optimize the performance of the circuits are also highlighted. Comparison with a recent published work [1] is also made.

2 Circuit Building Blocks

A. Operational Amplifier

The two-stage rail-to-rail input/output operational amplifier is used as the main amplifier stage. The CMOS op amp is designed based on the TSMC Mixed Signal 0.18μm-process technology. The power supply is set to 1.8V for low powered biomedical application devices. The op amp is design to process 0.9V common mode input voltage and able to amplified several milivolts of differential mode input voltage. Figure 1 shows the simplified schematic diagram of the CMOS op amp. The first stage is the folded-cascode op amp where the channel length of both input differential pair transistor M1n, M2n, M1p and M2p is set to minimum length which is 0.18μm. Input transconductance has been increased to increase the gain efficiency of the first stage and to have a lower thermal noise. This also helps minimizing the capacitance at the internal nodes as well.

The channel length of transistors M3, M4 and M9, M10 are sized larger than minimum length, which is 0.3μm and 0.62μm respectively, to increase the drain to source impedance. Since the transconductance of these transistors have no effect on the DC small signal gain, thus the transconductance efficiency is not a design concern.

To achieve a greater gain from the push-pull amplifier in the second gain stage, the gate length of transistors M11 and M12 are sized 0.3μm and 0.62μm respectively. This increases the miller effect at the end stage, thus the transistor size of the compensation capacitors N12 and P12 are set to

minimum value to reduce the miller effect.

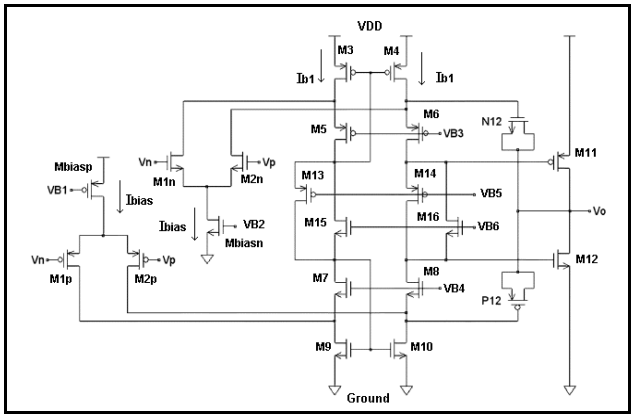

Figure 1 – Simplified schematic of CMOS op-amp

B. Biasing Circuit

The bias circuit of the operational amplifier consists of two basic current sources. The current sources are designed to supply I_{bias}, 20 μA for the two differential input pair. For the NMOS current source, transistors M1, M2 and M3 are used as voltage divider to control the gate-source voltage of transistor M7 and M11. The size of M7 and M11 are made identical to M3 thus the output current I_{bias} mirrors exactly the drain current through M2 and M3. In the PMOS current source, the size of transistors M8 and M12 are set equal to M4 to get output current I_{bias}.

C. Clock Generator

Figure 2 shows the circuitry that generates the non-overlapping clocks ph1 and ph2. The clock signals are used to activate the NMOS switches in the input offset cancellation circuitry. The clock signals ph1b and ph2b have an opposite phase to the ph1 and ph2 respectively. Ph1b and ph2b are the control signals of the dummy transistors, which connect both side of the NMOS switch [2].

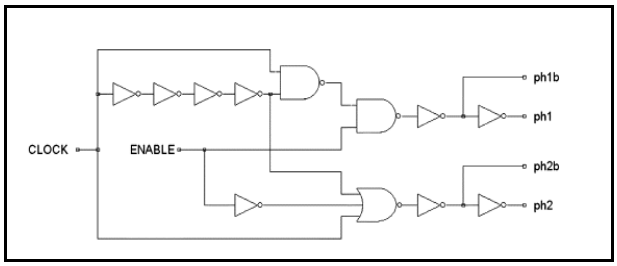

Figure 2 – Clock generator

The static CMOS design is used to implement the NOT, NAND and NOR gates for the clock generator. A static CMOS gate is a combination of the pull-up network (PUN) and the pull-down network (PDN). The PUN and PDN networks are connected in a mutually excusive fashion such that at every point in time, the gate output is connected to either positive power supply (V_{DD}) or negative power supply (V_{SS}). The PDN is constructed using NMOS devices, where an NMOS switch is on when the gate signal is high and off when the gate signal is low. On the other hand, PMOS transistors are used in PUN, where the PMOS transistor act as an inverse switch that is turn on when gate signal is low and turn off when the gate signal is high.

D. Instrumentation Amplifier

Figure 3 shows the structure of the three op amp instrumentation amplifier. At first, the gain stage is design without the consideration of the input offset voltage cancellation circuitry.

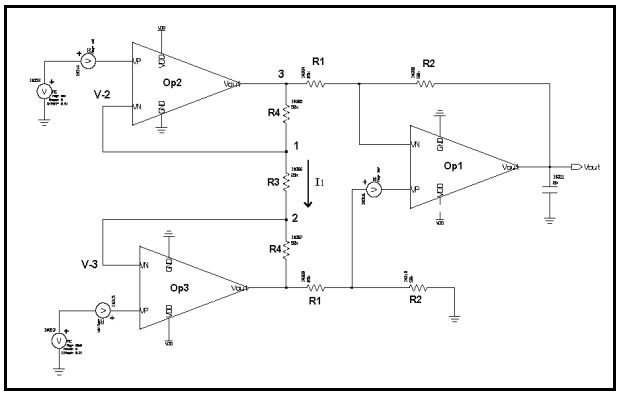

Figure 3 – Instrumentation Amplifier

The two non-inverting amplifiers Op2 and Op3 are function as input buffer stage to increase the input impedance. Op amp 1 is a differential amplifier function as an amplifying stage. By observation, the negative feedback of the upper-left op amp causes the voltage at point 1 (top of R3) to be equal to V1. Likewise, the voltage at point 2 (bottom of R3) is held to a value equal to V2. This establishes a voltage drop across R3 equal to the voltage difference between V1 and V2. That voltage drop causes a current through R3, and since the feedback loops of the two input op-amps draw no current, that same amount of current through R3 must be going through the two resistors R4 above and below it. The regular differential amplifier on the right-hand side of the circuit then takes this voltage drop between points 3 and 4, and amplifies it by a gain of R2/R1.

E. Complete Circuit

The complete circuitry of the CMOS instrumentation amplifier with input offset cancellation is shown in Figure 4. The two non-inverting amplifiers Op2 and Op3 function as an input buffer stage to increase the input impedance. Differential amplifier Op1 function as an amplifying stage. The negative feedback of Op2 causes the voltage at point 1 to be equal to Vn1. Likewise, the voltage at point 2 equal to Vp1. This establishes a voltage drop across R1 equal to the voltage difference between Vn1 and Vp1, which causes a current through R1. Since the feedback loops of the two input op-amps draw no current, thus this current flow through the two resistors R2. Differential amplifier Op1 amplifies this voltage drop by a gain of R4/R3.

The non-overlapping clock generator is used to control all the NMOS switches [3]. The capacitors Cos1, Cos2, and Cos3 that are connected between the input terminals, store the input offset voltage corresponding to Vos1, Vos2 and Vos3 for each op amp. When ph1 goes high, switches S1, S2, S4, S5, S7, and S8 are closed, the IA is in the offset storage mode, and the offset voltages of each op amp are stored across each capacitor. Eventually ph1 goes low and ph2 goes high, switches S3, S6, and S9 are closed, and the circuit is in the offset cancellation mode.

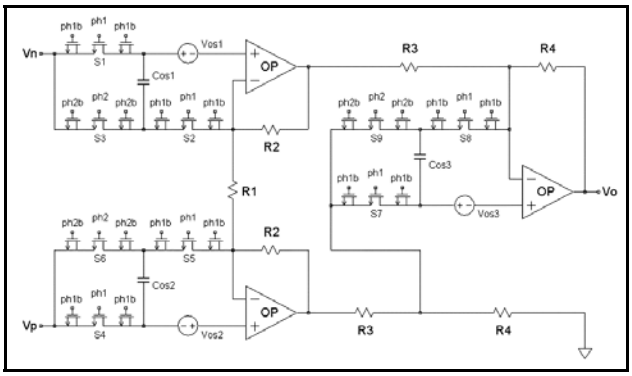

Figure 4 – Complete Circuit with Offset Cancellation Circuitry

The input offset voltages are cancelled by the precharged voltages stored in the capacitors Cos1, Cos2, and Cos3. It is connected with opposite polarity to the positive input terminal of each op amp. Each time a switch is turned off, the charges in its conducting channel are released and removed through the NMOS source and drain terminals. Thus, two dummy transistors are placed on the both sides of each switch transistor, to absorb the channel charges split equally between source and drain of NMOS switch. The two dummy transistors are controlled by ph1b and ph2b clock signals, which have the opposite phases to the switch transistor. The Cgs or Cgd of a switch transistor is approximated to the total parallel capacitance of (Cgs + Cgd) of a half-sized dummy transistor with source and drain short [4]-[7]. Capacitors Cos1, Cos2, and Cos3 are chosen to be 110fF. The (W/L) of NMOS switches is set to 2, while the minimum (W/L) of 1 are used for the dummy transistors to reduce total error voltage.

3 Results and Discussion

The CMOS instrumentation amplifier is designed using Mentor Graphics design tools based on TSMC 0.18um technology. The complete schematic of the instrumentation amplifier consists of 3 CMOS op amp, clock generator and input offset cancellation circuitries. The clock generator is represented by an instance to output the clock signals ph1, ph1b, ph2 and ph2b to the input offset cancellation circuitry. For the purpose of testing, the resistor R1 and R3 is chosen to be 50kΩ, R2 and R4 is set 25kΩ to create voltage gain of 10. Resistors R1, R2, R3 and R4 are intended to be off chip component, which were not included in the circuit layout to reduce the size of overall layout. The Capacitors Cos1, Cos2, and Cos3 have value of 110fF to store the offset voltage of each op amp. The offset voltage is set 1mV and connected in opposite polarity to each positive terminal of op amp. Table 1 shows the summary of the results and comparison with [1].

Table 1

Comparison with results from [1]

Description	Circuit designed by Chih-Jen Yen [1]	Circuitry design in this project
Technology	0.5μm	0.18μm
Power supply	2.5V -7.5V	1.8V
Gain average	19.99 dB	19.6 dB
Gain Bandwidth	20kHz	100MHz
CMRR (at DC)	>110 dB	92 dB
PSRR (at DC)	> 102dB	> 102 dB
Input-reffered noise	175nV/ Hz	2.28e-5 V/ √Hz
Current consumption	61μA - 125μA	413μA
Die area	0.2mm^2	13.34nm^2

This instrumentation amplifier has managed to get a comparable gain, CMRR and PSRR. This design also consumes power in micro-watts range which is suitable for low power biomedical instrumentation application. Since the minimum channel length of the transistor has reduced to 0.18μm, the switching speed of the MOS transistor had been greatly increased. This design has significant increase in the gain bandwidth to 100MHz. This means the CMOS instrumentation amplifier in this project able to function at higher frequency compare to the circuit designed by [1]. The chip area has been greatly reduced, which led to smaller die size.

It must be noted that the instrumentation amplifier designed by Chih-Jen Yen et al [1] has a lower input offset noise and lower current consumption. However, these advantages were achieved by using more complex CMOS and BJT wide swing design with start-up circuit to supply the bias current. The price is higher fabrication cost, compared to our full CMOS approach, which uses standard 0.18u process. The layout of the project is shown in Figure 5 below.

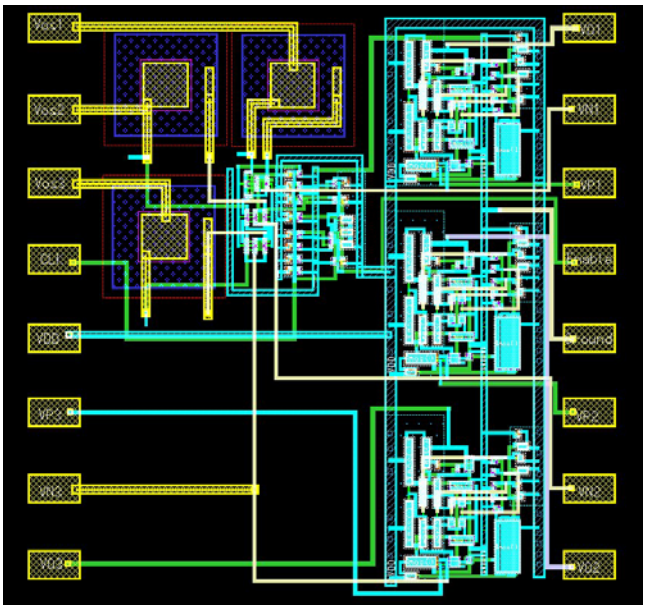

Figure 5 – Full layout

4 Conclusion

The design and development of a CMOS Instrumentation Amplifier for biomedical application is presented. It is found that the design has lower power supply, wider frequency response and smaller size, compared to the previous works. This design managed to achieve a comparable gain, CMRR and PSRR. The previous design has more complex and higher fabrication cost, since it used CMOS and BJT wide swing design, while this design uses full CMOS 0.18u standard process [8].

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