

# *A Low Noise Cascode Amplifier*

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We describe the design, schematics, and performance of a very low noise FET cascode input amplifier. This amplifier has noise performance of less than  $1.2 \text{ nV}/\sqrt{\text{Hz}}$  and  $0.25 \text{ fA}/\sqrt{\text{Hz}}$  over the 500 Hz to 50 kHz frequency range. The amplifier is presently being used in conjunction with a Penning ion trap but is applicable to a wide variety of uses requiring low noise gain in the 1 Hz to 30 MHz frequency range.

**Key words:** cascode amplifier; low bias current amplifier; low noise FET amplifier; noise analysis; noise current; noise voltage.

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## Introduction

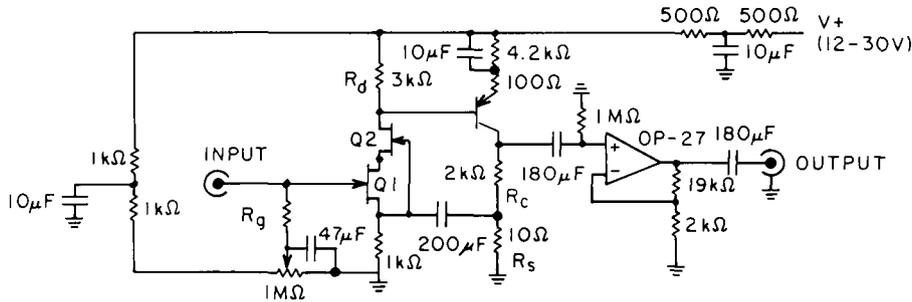
A low noise amplifier has been designed using a 2SK117 N channel J-FET as the input device in a cascode [1] configuration. Noise measurements on this amplifier yield a low frequency noise current of  $0.25 \text{ fA}/\sqrt{\text{Hz}}$  and a voltage noise of less than  $1.2 \text{ nV}/\sqrt{\text{Hz}}$  in the 500 Hz to 50 kHz region. Bloyet *et al.* [2] suggest a figure of merit of the product of the noise voltage and current as being appropriate for amplifiers of this type. This amplifier has a figure of merit of  $\sim 3 \times 10^{-25} \text{ W/Hz}$ , which is almost two orders of magnitude smaller than other amplifiers reported elsewhere. [2]

The amplifier described here is presently being used in conjunction with a Penning trap to detect small image currents ( $\sim 0.01 \text{ pA}$ ) induced by ion motion in the trap. [3] This amplifier also appears to be well suited for use in noise thermometry experiments. [4]

This paper discusses some general design criteria for cascode amplifiers and draws some conclusions concerning the optimum choice of FETs for such amplifiers. A particular design having the noise performance described above is presented and analyzed. Variations of the design which either have much larger bandwidth, 30 MHz, or draw extremely low input bias current, less than 0.01 pA, are briefly discussed.

## Equivalent Circuit for Noise Analysis

The schematic of the amplifier is shown in figure 1. The biasing scheme used for Q2, the common base portion of the cascode, is attractive for its simplicity and inherent low noise. However, to work properly it requires that  $I_{\text{dss}}$  [5] of Q2 be larger than  $I_{\text{dss}}$  of Q1.

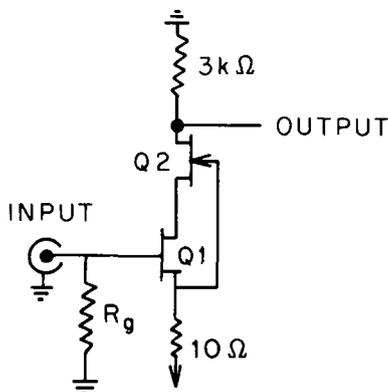


**Figure 1.** Schematic diagram of the low noise preamplifier. NOTE: 1) All resistors 1% metal film. 2) All capacitors are tantalum. 3) V+ must be well filtered. 4) The OP-27 power supply leads should be bypassed with 10 Ω and 0.1 μF close to the OP-AMP.

The gain of the cascode input stage is large, about 50. Hence, the noise in this stage is the dominant noise mechanism in the amplifier, and we will therefore confine our analysis to the cascode input stage and the associated biasing circuitry. The signal frequency equivalent circuit of the input stage is illustrated in figure 2. From figure 2 we can proceed to draw the noise equivalent circuit as shown in figure 3. Using this model, we can write the equivalent input noise,  $E_{ni}$ , as [6]

$$E_{ni}^2 = E_{nR_g}^2 + E_{nQ1}^2 + I_{nQ1}^2 Z_g^2 + \left(\frac{1}{K_{Q1}}\right)^2 \left[ E_{nQ2}^2 + I_{nQ2}^2 R_{sl}^2 \right] + \left(\frac{1}{K_t}\right)^2 E_{nR_d}^2 \quad (1)$$

where  $K_t = gm_1 R_d$  and  $K_{Q1} = -gm_1/gm_2$  is the gain of the common source component of the cascode.  $Z_g$  is the impedance presented to the gate of Q1 formed by the parallel combination of  $C_g$ , the gate capacitance, and  $R_g$ , the gate bias resistor. The choice of Q2 is governed by a tradeoff between



**Figure 2.** Signal frequency equivalent circuit of the cascode input stage.

bootstrapping  $C_{gd}$  of Q1 for lowest input capacitance and gain in Q1 suppressing voltage noise in Q2 relative to Q1. This suggests that the choice of identical FETs for Q1 and Q2 may not be optimum. For this amplifier, we chose Q2 to be a 2N4416, yielding  $gm_1/gm_2 \sim 4$ , which suppresses the voltage noise of Q2 well below that of Q1 and still provides a reduction of input capacitance from  $\sim 44$  to  $\sim 11$  pF.

## Noise Measurements

The amplifier noise was determined by first measuring the transfer function of the amplifier on a spectrum analyzer (see fig. 4). The input capacitance was then obtained by using a known value of the capacitor in series with the input of the amplifier and measuring the change in apparent amplifier gain as a function of capacitance. In order to measure the input current noise, the gate bias resistor,  $R_g$ , was increased to  $7 \times 10^{11} \Omega$  so that the term  $I_{nQ1}^2 Z_g^2$  would dominate in eq (1). A measurement of the noise from 1.5 to 10 Hz coupled with the known input capacitance,  $C_g$ , allows one to write

$$\frac{1}{E_{ni}(f)} \approx \frac{1}{R_g I_{nQ1}} (1 + 2\pi C_g R_g f), \quad (2)$$

where  $E_{ni}(f)$  is the equivalent noise at frequency  $f$  at the input of Q1. Using a linear regression analysis to find the slope,  $m$ , of the  $1/E_{ni}$  vs  $f$  line, we can then write

$$I_{nQ1} \approx \frac{2\pi C_g}{m} \quad (3)$$

This analysis holds, assuming that the thermal noise current of  $R_g$  does not swamp the noise current of Q1 and that the perturbation of  $1/f$  noise is small. The first assumption is easily checked as our

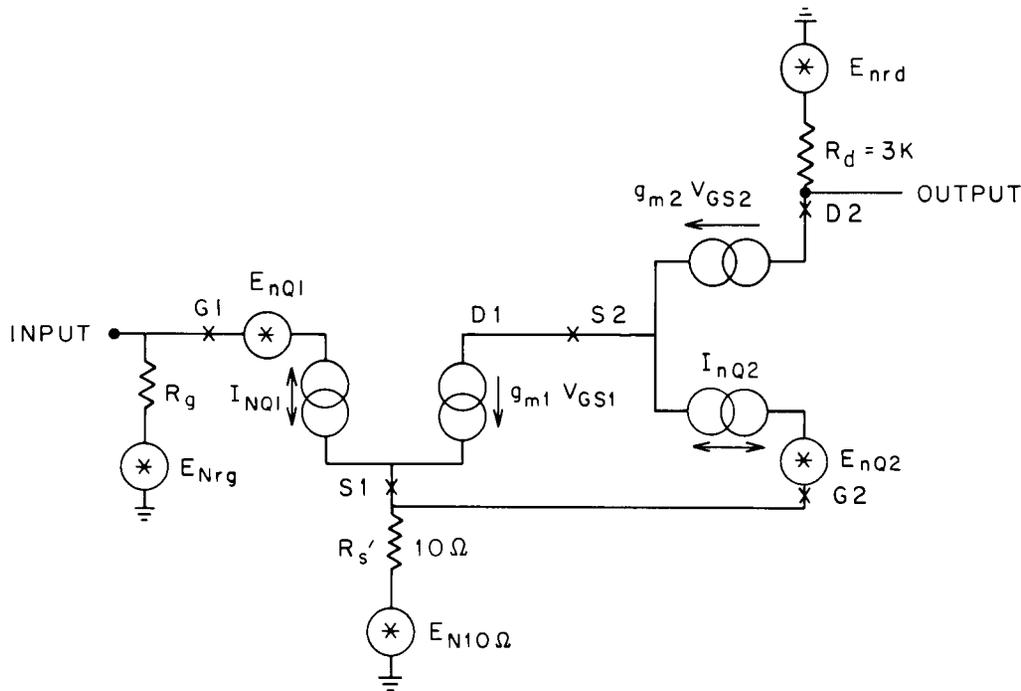


Figure 3. The noise equivalent circuit of the cascode input state.

$7 \times 10^{11} \Omega$  resistor used for  $R_g$  generates only  $0.15 \text{ fA}/\sqrt{\text{Hz}}$  noise current which is of the same order of magnitude as the noise current associated with Q1. The  $1/f$  contribution of current noise in both the input FET and  $R_g$  was measured to be less than  $10^{-16} \text{ A}/\sqrt{\text{Hz}}$  at 1.5 Hz.

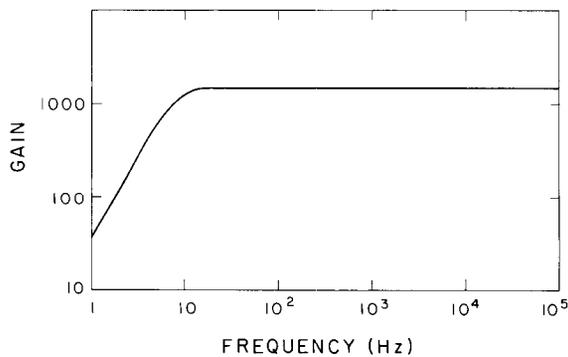


Figure 4. Measured transfer function of the amplifiers.

$E_{nQ1}$ , the voltage noise associated with Q1, was measured by replacing the  $7 \times 10^{11} \Omega$  resistor used for  $R_g$  with a  $10 \Omega$  resistor. This makes the  $I_{nQ1}^2 Z_g^2$  term in eq (1) insignificant and the equation can then be rewritten to yield:

$$E_{nQ1}^2 = E_{ni}^2 - E_{nRg}^2 - \left( \frac{E_{nQ2}}{K_{Q1}} \right)^2 - \left( \frac{E_{nRd}}{K_t} \right)^2 \quad (4)$$

If the noise associated with Q2,  $gm1/gm2$ , and the output noise are measured, one can infer the noise associated with Q1.

### Results

Measurements using three different 2SK117 FETs for Q1 and a variety of different 2N4116 FETs for Q2 give the following results for the amplifier

$$E_{ni} \approx 1.1 \text{ nV}/\sqrt{\text{Hz}} \quad I_{ni} \approx 0.25 \text{ fA}/\sqrt{\text{Hz}} \quad (5)$$

Figure 5 shows the measured voltage noise as a function of frequency for the amplifier. Independent measurements with 2N4416 FETs show that the noise voltage associated with them is approximately  $3 \text{ nV}/\sqrt{\text{Hz}}$ . Using this value and eq (5) we can infer a noise voltage for the 2SK117 of about  $0.8 \text{ nV}/\sqrt{\text{Hz}}$ . It is interesting to compare this to the theoretical result derived by van der Ziel: [7]

$$e_{nQ1} = \left( \frac{2}{3} \frac{4KT}{gm1} \right)^{1/2} \quad (6)$$

Using  $gm1 = \frac{1}{60 \Omega}$ , the transconductance of the

2SK117 at 3 mA drain current, we obtain  $e_{nQ1} = 0.82 \text{ nV}/\sqrt{\text{Hz}}$  which is in agreement (possibly fortuitous) with the measured result.

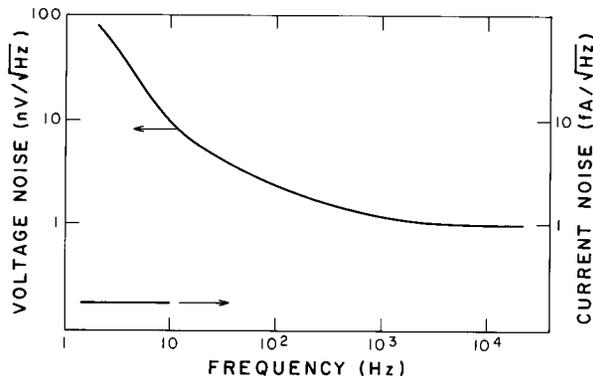


Figure 5. Measured input voltage noise.

If one measures the gate current of the input FET in a version of this amplifier in which Q2, the common gate portion of the cascode, is shorted, making the input of the amplifier a common source stage, an interesting effect occurs. The gate current, as measured by the voltage drop across  $R_g$ , decreases and finally changes sign with increasing drain current. A measurement of the noise current in this region suggests that in fact two (at least) competing currents are responsible, as the noise current is monotonically increasing in the region of apparently zero gate bias current. This is as would be expected for the noise from two competing processes. Thus, this effect is potentially useful in an application in which the amplifier must draw a minimal bias current through the gate. However, a drawback to this circuit is that the input capacitance is  $\sim 50 \text{ pF}$  as opposed to  $\sim 11 \text{ pF}$  for the cascode configuration. The cascode amplifier also exhibits very low input bias current, typically less than  $0.3 \text{ pA}$  for drain currents in the  $3 \text{ mA}$  range, but it does not exhibit an apparent vanishing of this bias current as does the common source configuration. It should be noted that this effect prevents us from inferring that the noise current in Q1 is due to shot noise in the measured gate current of Q1, since the true gate current is not a well determined quantity in the presence of these competing currents.

The bandwidth of the amplifier as shown in figure 1 is limited to about  $500 \text{ kHz}$ . This bandwidth limitation is, however, due to the limited bandwidth of the op-amp used for the output stage. If additional bandwidth is required,  $R_c$  and  $R_d$  should be reduced and a video amplifier should be used as the output stage.

## Conclusion

We have discussed the design and test of a FET cascode input amplifier with extremely low voltage noise, less than  $1.2 \text{ nV}/\sqrt{\text{Hz}}$ , and extremely low current noise,  $0.25 \text{ fA}/\sqrt{\text{Hz}}$ .

This amplifier also has a low input capacitance of  $11 \text{ pF}$ . Thus it can be used to provide useful low noise gain from  $1 \text{ Hz}$  to more than  $30 \text{ MHz}$ . Another significant attribute is the very low bias current drawn by the amplifier, less than  $0.3 \text{ pA}$ ; a modified version of this amplifier draws even less input bias current. A short discussion of design criteria and noise mechanisms in cascode amplifiers is also provided.

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## References

- [1] The term cascode amplifier refers, in a historical sense, to a pair of triode vacuum tubes operated as a grounded cathode amplification stage followed by a grounded grid amplification stage. In the case of bipolar transistors it refers to a common emitter stage followed by a common base stage and in FETs it is a common source-common gate pair as used here. Hybrid cascode amplifiers using a common source FET followed by a common base bipolar transistor are also common. See, for example, R. Q. Twiss and Y. Beers, in *Vacuum Tube Amplifiers*, MIT Radiation LABS Series edited by G. E. Valley Jr. and M. Wallman (Boston Technical Lithographers, 1963), Ch. 13.
- [2] Bloyet, D., Lepaisant, J., and Varoquaux, E., *Rev. Sci. Instrum.* **56**, 1763 (1985).
- [3] Barlow, S. E., Luine, J. A., and Dunn, G. H., *Int. J. Mass. Spectrom. Ion Proc.* **74**, 97 (1986).
- [4] Anderson, P. T., and Pipes, P. B., *Rev. Sci. Instrum.* **45**, 42 (1974).
- [5]  $I_{dss}$  is the value of the saturated drain-source current in a FET operated at zero gate source voltage.
- [6] Motchenbacher, C. D., and Fitchen, F. C., in *Low Noise Electrical Design* (Wiley, New York, 1973), p. 231.
- [7] van der Ziel, A., *Proc. IEEE* **50**, 1808 (1962).