A CMOS Programmable Gain Amplifier with a Novel DC-offset Cancellation Technique

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***Abstract*- A programmable gain amplifier (PGA) with a novel DC offset cancellation (DCOC) technique for IEEE 802.11b/g wireless LAN direct-conversion receiver (DCR) is presented. An operational amplifier (OPAMP) utilizing an improved Miller compensation approach is adopted in this PGA design. A gain tuning range of 0 dB to 56 dB with 2 dB per step is achieved. The DCOC loop is based on a voltage-current negative feedback that includes a switchable bandwidth algorithm to speed up the settling time of DCOC. The proposed approach requires no external components and demonstrates excellent DCOC capability in measurement. Fabricated in a 0.13 µm CMOS technology, this PGA dissipates 9.7 mW from a 1.2 V supply voltage and occupies an area of 0.17 mm^2.**

I. INTRODUCTION

In recent years, direct conversion has become the most popular architecture of receivers due to its lower power consumption, lower complexity and fully monolithic integration capability comparing with super-heterodyne counterparts. Nevertheless, direct conversion entails some design challenges that do not exist in heterodyne architectures. These issues are DC offset, I/Q mismatch, flicker noise, even-order distortion and local oscillator (LO) leakage. Among them, DC offset is the most detrimental issue. Extraneous DC offset located in down-converted signal spectrum may corrupt the signal, degrade sensitivity and dynamic range of the receiver system, and even saturate the following analog baseband stages if a high gain is required [1]. Thus DC offset cancellation is inevitably becoming a challenge in design of direct conversion receivers.

Generally, there are two conventional DCOC techniques: AC coupling [2] and digital cancellation with digital-to-analog converters (DAC) [3]. AC coupling involves a high pass filter with extremely low cut-off frequency near DC. Large capacitors which are unsuitable for monolithic integration are required for AC coupling. The digital solution involving DAC can achieve a fast settling time during a baseband gain step at the cost of complicating the design and increasing power dissipation.

In this paper, a PGA with a novel DC offset cancellation technique for IEEE 802.11b/g wireless LAN DCR is presented. System diagram of this receiver is shown in Fig. 1. Based on a fully-differential resistive feedback topology, the proposed PGA achieves high linearity, precise gain and extended closed loop bandwidth due to the high-performance OPAMP, which employs a modified Miller compensation approach. This approach offers a solution for the problem that traditional OPAMP usually has difficulty to obtain high open loop gain at the down converted signal band such as 10 MHz and keep stable at the same time. Furthermore, the proposed DCOC technique overcomes the drawbacks of AC coupling and digital solution. This new technique requires no external components and occupies a small area. Without complicating the design or increasing power consumption greatly, the proposed technique demonstrates good DC offset cancellation capability. Both signal integrity and fast settling are achieved due to the use of a switchable bandwidth algorithm.

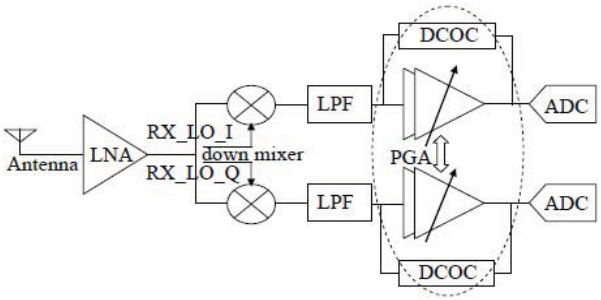

Fig. 1. Block diagram of the direct- conversion receiver

This paper is organized as follows. Firstly, circuit analysis and design of the proposed PGA is presented in section II. Secondly, experimental results are given in section III. Finally, conclusions are drawn in section IV.

II. CIRCUITS ANALYSIS AND DESIGN

A. PGA Circuit Design

PGA is one of the key building blocks of DCR system owing to its role of dynamic range extension and optimization. In general, a design of PGA needs to trade off among gain, bandwidth, linearity and noise under power consumption and die area constraints. Fig. 2 illustrates the basic architecture of the proposed PGA. A fully-differential resistive feedback topology is adopted. Assuming an ideal OPAMP, the closed loop voltage gain is given by

$$Gain \approx R_2 / R_1 . \quad (1)$$

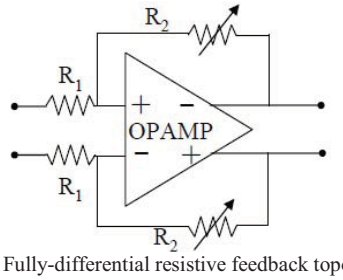

Fig. 2. Fully-differential resistive feedback topology

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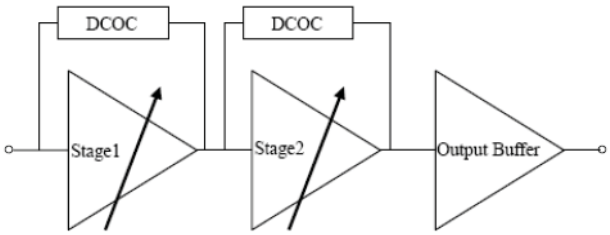

Fig. 3. Configuration of the proposed PGA

As illustrated in Fig. 3, the main architecture of PGA consists of two gain stages and an output buffer stage with 0 dB gain for driving the following analog-to-digital converters. Gain tuning is accomplished by switching feedback resistors with the help of a 5-bit decoder. The first stage can realize a gain tuning range of 0 dB to 28 dB, while the second stage achieves discrete gain tuning steps ranging from 0 dB to 28 dB. Owing to proper combination of gain switching, a gain tuning range of 0 dB to 56 dB with 2 dB per step is obtained with appropriate decoding. Each gain stage has a DC offset cancellation loop. These two DCOC loops working together can attain great DC attenuation.

B. The Operational Amplifier

Since the performance of PGA mainly depends on the OPAMP, high-performance OPAMP is required. In general, DC gain, gain-bandwidth product (GBW) and phase margin (PM) characteristics are major considerations about OPAMP design. High DC gain, large GBW and proper PM always indicate high linearity, precise gain and reliable stability. Schematic architecture of the proposed OPAMP is shown in Fig. 4.

Based on conventional two-stage OPAMP, this OPAMP consists of two common-source amplifying stages and one common mode feedback (CMFB) loop. Current mirrors are employed to supply the OPAMP with bias current. Differential amplifier in stage1 plays an important role of high DC gain acquirement. Stage2 is comprised of two common-source amplifiers actively loaded with the current-source transistors. Common mode signal, which is detected by two pairs of parallelized resistor and capacitor at the output of stage2, is compared with the reference common mode voltage and sends feedback to stage1.

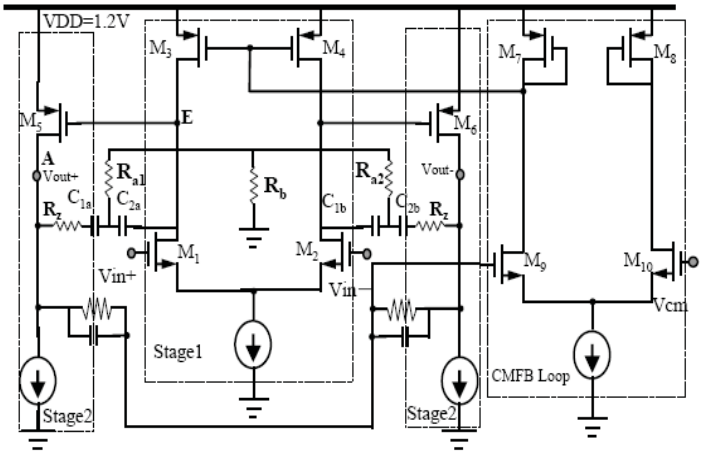

Fig. 4. Two-stage OPAMP with the proposed Miller Compensation.

It is difficult to achieve high open-loop gain at the down-converted signal band like 10 MHz and keep reliable stability at the same time with the conventional two-stage OPAMP. To settle this problem, one new approach has been introduced to improve the conventional Miller compensation [4].

To gain more insight into this new approach, a review of the conventional Miller compensation is presented firstly. As shown in Fig. 5(a), A_{V1} andA_{V2} represent two stages of the OPAMP. R_Z and C_C are incorporated in series to form Miller compensation. Due to Miller Effect, C_C founds an equivalent capacitor at node E, whose value is $(1+A_{V2})$ times bigger than C_C. The dominant pole at node E and the non-dominant pole at node A are made separated from each other much farther than they were before compensation. This effect on poles is called pole splitting, which is beneficial for gaining high PM. R_Z is used to cancel the effect of right half-plane zero(RHZ) introduced by feedforward path of C_C.

As illustrated in Fig. 5(b), the proposed approach based on conventional Miller compensation can attain higher gain at 10 MHz and extend closed-loop bandwidth at the cost of a little increase of die area. Since the equivalent impedance of $2C_C$ is much higher than R_a at low frequency, most of the feedback current from node A flows to the ac ground through R_a. At high frequency, the influence of R_a could be neglected for its much higher impedance value compared to the impedance of $2C_C$. Similar frequency response can be obtained just as the conventional Miller compensation at high frequency. R_b in Fig. 4 is used for keeping the CMFB loop stable. Comparison result of open-loop frequency response of OPAMP with the conventional and the improved Miller compensation is given in Fig. 6. The crossed frequency point occurs when the impedance of $2C_C$ equals to R_a and is given by

$$f_{crossed} = 1/(2\pi \cdot 2C_C \cdot R_a). \quad (2)$$

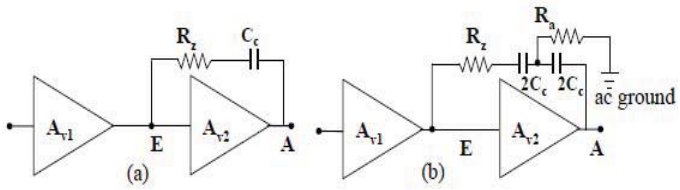

Fig. 5. (a) The conventional Miller compensation
(b) The proposed Miller compensation

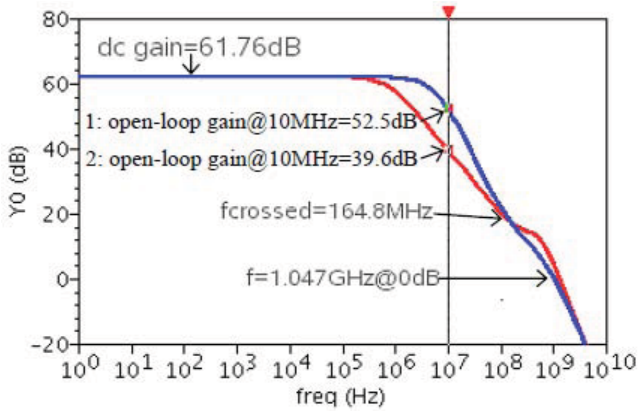

Fig. 6. Simulated frequency response the OPAMP with the proposed (curve 1) and the conventional (curve 2) Miller compensation schemes

The proposed OPAMP characters with 61.7 dB DC gain, 52.5 dB gain @10MHz, 57° PM of differential mode, 70° PM of common mode, and 1.05 GHz unit gain frequency (UGF) with 1 pF differential capacitor load. The power consumption of this OPAMP is 1.7 mA with a 1.2 V supply voltage.

C. DC offset Cancellation Loop

The DC-offset cancellation loop is designed based on voltage-current negative feedback [5]. Simplified architectures of stage1 of PGA and its DCOC loop are shown in Fig. 7. Stage2 employs the similar architecture.

DC offset at node V_o is extracted by the low pass filter formed by R_3 and C_0 at first, and then is amplified by β, and converted to feedback current at node F through R_4. R_{3a} and R_{3b}, in place of R_3, are used to speed up the settling time of DCOC by means of switchable bandwidth algorithm. C_1 is used as Miller capacitor and the equivalent capacitance C_0 approximates to the product of the compensation capacitor C_1 and the gain of β, as describes in the following equation.

$$C_0 = \beta \cdot C_1. \tag{3}$$

Without large die area consuming, a large capacitance C_0 is obtained with a small capacitor C_1 whose value is set as 5 pF in this design.

PGA gain is given by Eq. 1. The closed loop transfer function can be modeled as an adding function of V_i and V_o at node F. Therefore, we can write

$$V_o = V_o' \cdot (-\frac{R_2}{R_4}) + V_i \cdot (-\frac{R_2}{R_1}), \tag{4}$$

where

$$V_o' = V_o \cdot (\frac{\beta}{1+\frac{s}{\omega_0}}) \tag{5}$$

and

$$\omega_0 = \frac{1}{R_3 \cdot C_0} = \frac{1}{R_3 \cdot \beta \cdot C_1}. \tag{6}$$

The transfer function of PGA and DCOC loop can be derived as

$$H(s) = \frac{V_o}{V_i} = \frac{(-\frac{R_2}{R_1}) \cdot (s+\omega_0)}{s + (\beta \cdot \frac{R_2}{R_4} + 1) \cdot \omega_0}. \tag{7}$$

Generally, $\beta R_2 / R_4$ is much larger than 1. Hence, the high pass cutoff frequency can be expressed approximately as

$$\omega_C = (\beta \cdot \frac{R_2}{R_4} + 1) \cdot \omega_0 \approx \beta \cdot \frac{R_2}{R_4} \cdot \omega_0 \approx \frac{R_2}{R_3 \cdot C_1 \cdot R_4}. \tag{8}$$

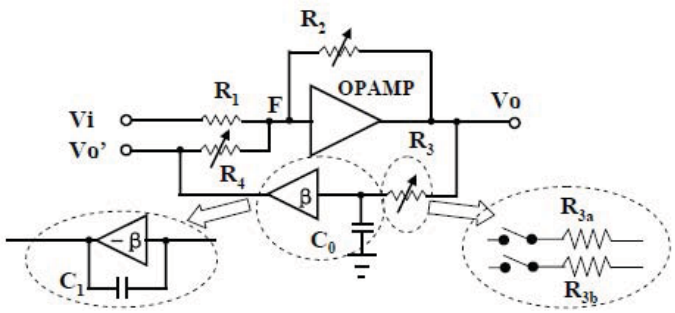

Fig. 7. Simplified architectures of stage1 and its DCOC loop

Since C_0 is set as 5 pF for die area considerations and R_{3a}, R_{3b} are used to realize the switchable bandwidth algorithm, Eq. 8 suggests that ω_C will maintain constant if the value of R_2 / R_4 stays constant. Hence, we keep the value of R_4 equals to $3.8R_2$ all the time to make ω_C independent of PGA gain switching in this design.

To gain more insight into the advantages of the switchable bandwidth algorithm, calculation work on DCOC settling time is carried out firstly. Suppose the residual offset at the output terminal is ΔV_{o1} when PGA gain is A_1. When the gain of PGA switches to A_2, the residual offset changes to ΔV_{o2}. Modeling the DCOC loop with a first-order filter, the DCOC settling time t_S could be defined as

$$t_S = \frac{1}{\omega_C} \cdot \ln \frac{A_2 \cdot \Delta V_{o1}}{A_1 \cdot \Delta V_{o2}}. \tag{9}$$

Eq. 9 suggests that the DCOC settling time t_S mainly depends on ω_C. Since C_0 is 5 pF and the value of R_2 / R_4 stays constant, Eq. 8 indicates that ω_C is decided by R_3. R_{3a} and R_{3b} occupy different values in order to realize two switchable bandwidths. Since down-converted signal occupies a bandwidth of 160 kHz to 10 MHz in 802.11b/g standards, we determinate the low cut-off frequency ω_{CL} at 10 kHz for signal integrity and the high cut-off frequency ω_{CH} at 700 kHz for fast DCOC settling. With switchable bandwidth algorithm, we can achieve both fast settling and signal integrity.

In addition to ω_C, DC attenuation can also be obtained from the transfer function as

$$H(0) = \frac{Gain}{\beta \cdot (R_2/R_4) + 1} = \frac{Gain}{\beta \cdot cons\tan t + 1}. \tag{10}$$

where constant equals to 0.263 in this design. DC attenuation varies according to PGA gain. For instance, when β and this constant have values of 61 dB and 0.263 respectively, DC gain is attenuated by 43 dB at 56 dB (28 dB of stage1, 28 dB of stage2) gain level and 94 dB at 0 dB gain level approximately. The calculated results of Eq. 10 match well to the results of simulation. We can change either β or the constant (R_2 / R_4) to get appropriate DC attenuation. Fig. 8 demonstrates the simulated frequency response of PGA with DCOC loops.

The proposed PGA design was implemented in a 0.13μm CMOS technology, occupying an area of 0.17 mm^2. Die photograph of this design is shown in Fig. 9.

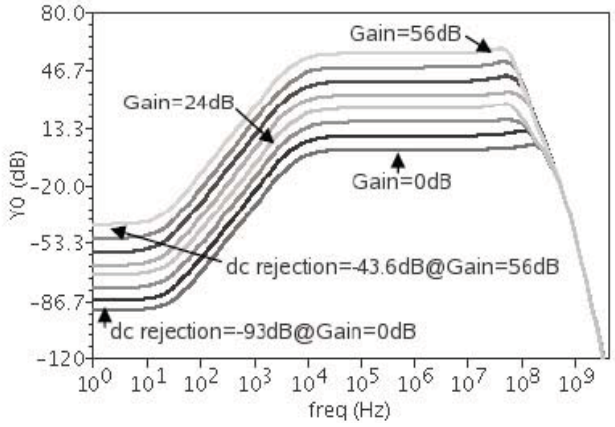

Fig. 8. Frequency response of PGA with DCOC loops: ω_C=ω_{CL}=10 kHz.

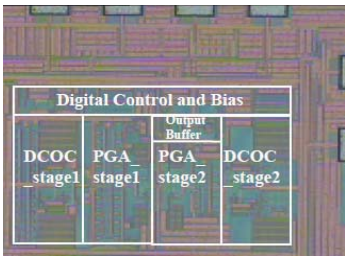

Fig. 9. Die photograph of the proposed PGA and DCOC

III. Experimental Rerults

A. Measurement of PGA

Experimental results of PGA gain tuning range are shown in Fig. 10. The proposed PGA covers a gain tuning range of 0 dB to 56 dB in 2-dB steps with a total of 28 steps. Step error is less than 0.2 dB.

The input third intercept point (IIP3) is 0.8 dBm at 24 dB gain level. Noise figure at the same gain level is 19.3 dB referred to 50 Ω. Measured IIP3 and noise figure are shown in Fig. 11. Attention should be paid to that neither the linearity nor the noise figure of PGA has been deteriorated obviously with DCOC loop. 1.84 V differential peak-to-peak voltage swing has been measured at the output of PGA. 3-dB bandwidth is 57 MHz at the maximum gain.

B. DCOC Effect

The proposed DCOC technique shows good cancellation capability in test, as shown in Fig. 12. The residual DC offset measured at the output of PGA is less than 3 mV. With the proposed switchable bandwidth algorithm, both signal integrity and fast settling are achieved. As shown in Fig. 13, when the gain of PGA switches from 0 dB to 32 dB, the DCOC settling time reaches to 252 ns approximately.

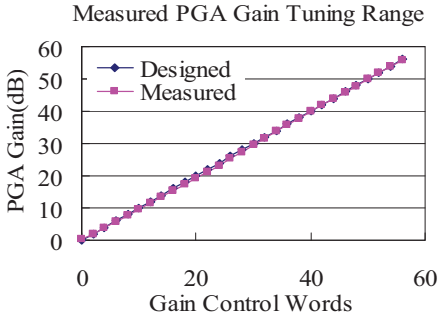

Fig. 10. Measurement of PGA gain tuning range: step error is less than 0.2 dB.

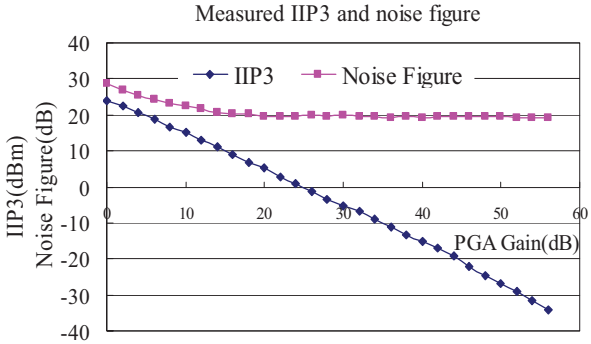

Fig. 11. Measurement results of IIP3 and noise figure of PGA.

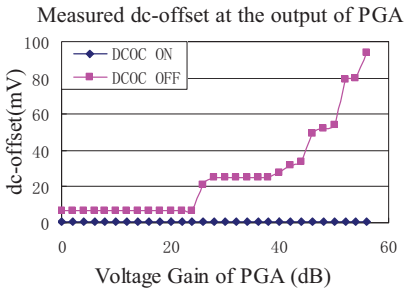

Fig. 12. Measurement results of dc-offset at the output of PGA.

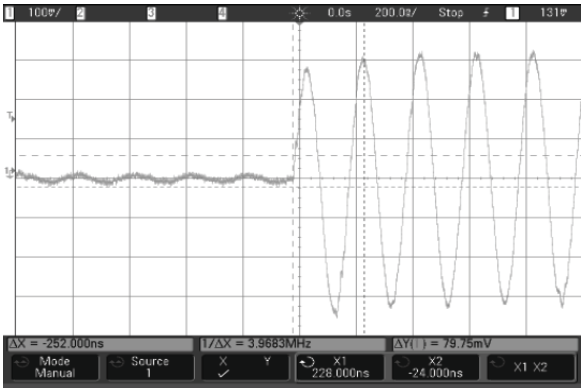

Fig. 13. Measurement of DCOC settling time: t_S =252 ns. PGA gain switches from 0 dB to 32 dB. The high pass cut-off frequency $\omega_C = \omega_{CH}$=700 kHz.

IV. Conclusion

A PGA with a novel DC offset cancellation technique is proposed. An OPAMP utilizing an improved Miller compensation approach is adopted in PGA design. This proposed DCOC technique requires no external components and demonstrates good cancellation capability. Table I gives the performance summary of the proposed PGA and DCOC.

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TABLE I. Measured Performance Summary

Technology	0.13 μm CMOS process
Area Occupying	0.17 mm^2 (0.38 mm×0.45 mm)
Gain Tuning Range	0 dB to56 dB in 2-dB steps
IIP3 @24 dB gain level	0.8 dBm referred to 50 Ω
Noise Figure @24dB gain level	19.3 dB referred to 50 Ω
3-dB Bandwidth	57 MHz@ Maximum Gain
DCOC settling time	252 ns($\Delta Gain$=32 dB)
DCOC cut-off frequency	ω_{CL} =10 kHz, ω_{CH} =700 kHz
Power Dissipation	9.7 mW (1.2 V supply voltage)