A guide to using FETs for voltage controlled circuits, Part 1

Ron Quan - October 13, 2017

Editor's note: I am so happy that there are still companies around that create precision, discrete transistors in our industry; Linear Integrated Systems is one of the best I have encountered. There are so many applications for the need to design circuitry using quality discrete components instead of integrated circuitry. This multi-part article will show the many advantages of doing these types of designs.
—*Steve Taranovich*

Linear Integrated Systems manufactures a variety of FETs (field effect transistors). In particular they have a variety of matched dual products. There are advantages in having matched devices. For example, if you are building a two-channel stereo audio product, having two or four devices in the same package allows for the two audio channels to be more closely matched.

This paper will explore using FETs in voltage controlled circuits.

Several approaches will be shown:

1. Using FETs as voltage controlled resistors.
2. Using FETs as voltage controlled amplifiers and active mixers.
3. Using FETs as voltage controlled phase shifters for processing music.
4. Using FETs as voltage controlled band pass filters.

[See more circuitry using discrete FETS here: Building a JFET voltage-tuned Wien bridge oscillator.]

We will also explore ways to reduce nonlinearities or distortions and automatically bias the FETs.

FET voltage controlled resistors

Figure 1 shows a typical current-voltage relationship of an N Channel FET.

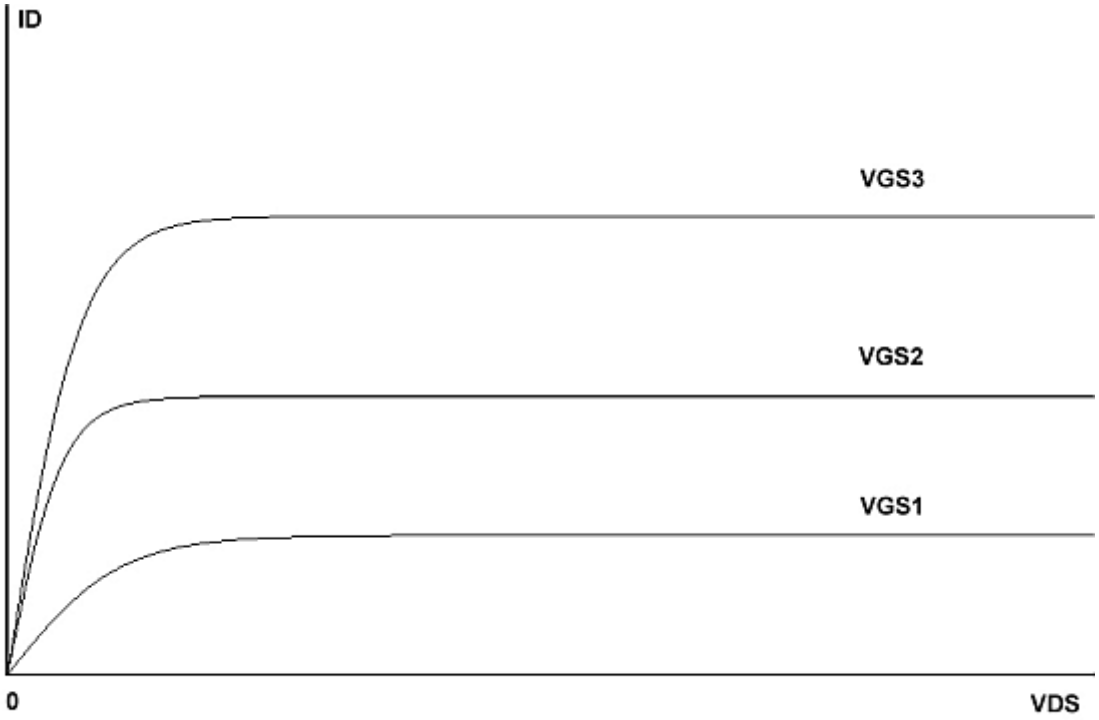

Figure 1 A typical N-Channel FET I/V curve for different gate-to-source voltages, VGS1, VGS2, and VGS3.

An FET has basically two regions:

The **saturation region**, which includes each of the horizontally flat portions where the FET acts as a voltage-controlled current source and the other region that includes the sloped “curved portions” is the **triode or ohmic region** where the FET can operate as a voltage-controlled resistor. If we look carefully we will notice that the triode region in Figure 1 is shown for drain to source voltages (VDS) that are non-negative.

Note: The triode or ohmic region in an FET is sometimes known as the linear region. The FET operating as a voltage-controlled resistor (VCR) works in this region. Preferably, there is no DC voltage across the FET’s drain and source terminals in the VCR mode.

If we extend the VDS voltage range to include slightly negative voltages for a particular gate-t--source voltage, we see that the there is still a resistive effect (**Figure 2**).

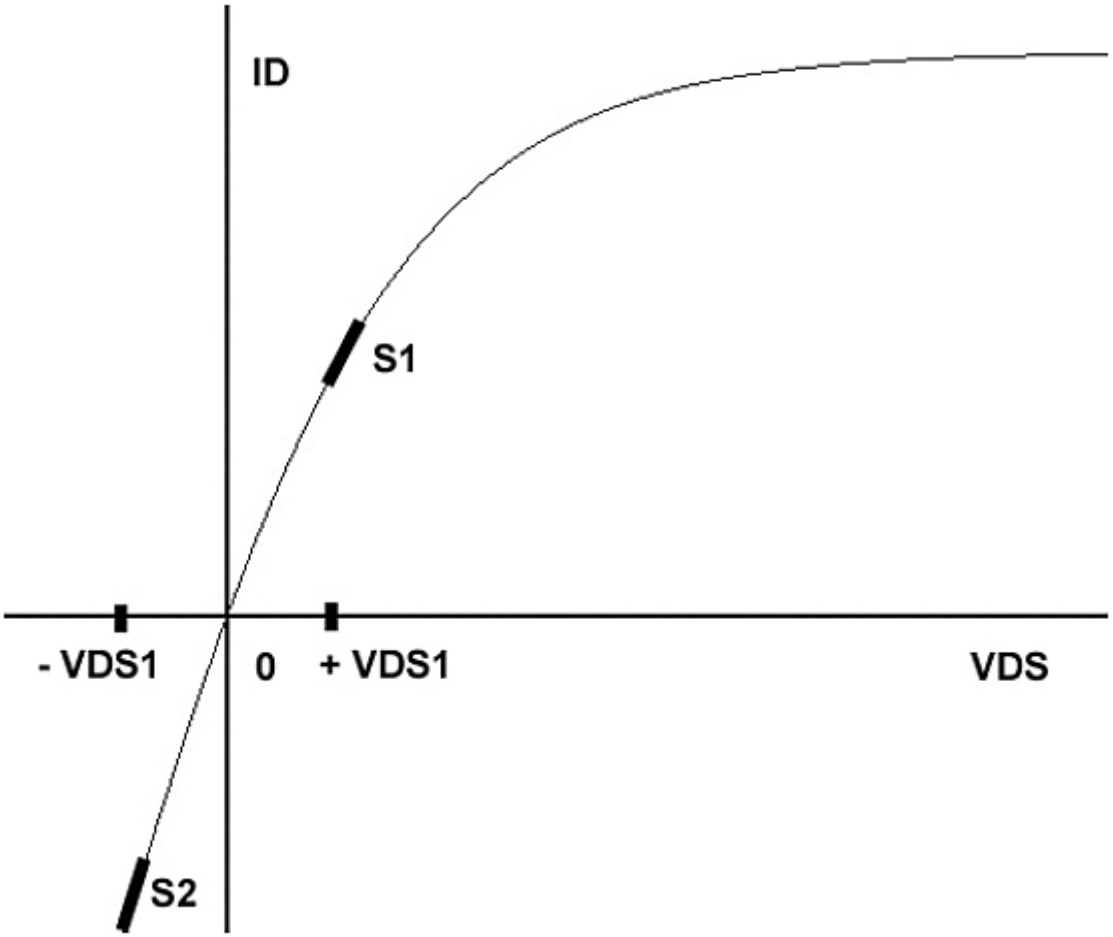

Figure 2 FET's triode region extended to a negative VDS voltage, - VDS1, that still shows a resistance effect.

The slope is defined as:

Slope = $\Delta ID/\Delta VDS = g_{ds}$ = conductance between the drain and source.

And the resistance across the drain and source is the reciprocal of the conductance,

$R_{ds} = 1 / g_{ds} = \Delta VDS/\Delta ID$

As we look at the two slopes that denote g_{ds}, S1 and S2, we will see that they are approximately the same. But if we look very closely, they actually are slightly different with the S2's slope being steeper than slope S1. A steeper slope yields a higher conductance, which results in a lower resistance. For example, the resistance around the high sloped region around S2 or – VDS1 is lower than the resistance around S1 or + VDS1. The gradual change in resistance from +VDS1 to – VDS1 results in distortion. Fortunately, the distortion can be kept small.

For instance, with small AC signals (e.g., < 500 mV peak to peak) across the drain and source, the harmonic distortion can be "reasonably" low. As an example, if the AC signal voltage across the drain and source is between – 250 mV and +250 mV, then the harmonic distortion will be "small", typically < 3%.

At this point, one may ask if are there specific FETs made just for voltage controlled resistor applications? The answer is yes (e.g., VCR11), but it turns out that virtually any other FET (e.g.,

JFET and MOSFET) can be used as a voltage controlled resistor.

Basic voltage controlled resistor circuits

Basic voltage controlled resistor (VCR) circuits

One of the simplest uses of a voltage controlled resistor is an electronically controlled attenuator or "volume control". The basic circuit forms a voltage divider as shown in **Figures 3, 4, 5, and 6**.

In each of these circuits, the drain and source terminals of the FETs (Q1, Q2, Q3, and Q4) provide a voltage controlled resistance. For frequencies greater than 20 Hz, C1's impedance can be considered as an AC short circuit. Let's look at **Figure 3** below:

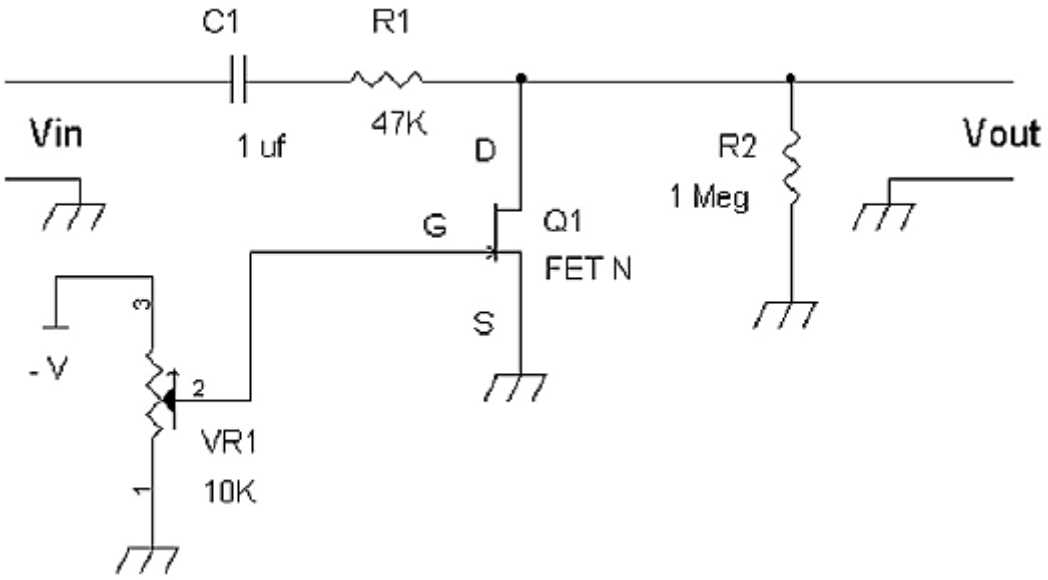

Figure 3 N Channel JFET attenuator circuit.

In **Figure 3**, maximum attenuation is achieved by setting Q1's gate voltage to 0 volt or ground. R2 is to establish a DC path to ground for Q1's drain. It can be omitted if C1 is replaced with a wire, and the input signal source has no appreciable DC offset voltage (e.g., < 10 mV DC), and the input signal source has a DC path to ground.

Minimum attenuation (e.g., a "pass through") happens when the negative voltage at Q1's gate causes Q1 to be in cut-off (e.g., the gate voltage → V_p, the pinch off voltage).

The attenuator's transfer function is then:

V_{out}/V_{in} = [R_{ds} || R2] / [R1 + (R_{ds} || R2)]

Note that R_{ds} is the drain to source resistance for a given gate to source voltage.

If R_{ds} << R2, then

V_{out}/V_{in} = [R_{ds}] / [R1 + Rds]

For example, if Rds = 10KΩ then

V_{out}/V_{in} = [10KΩ] / [47KΩ + 10KΩ] = 10KΩ/57KΩ = 10/57 = 0.1754

The drain current for a ***"depletion mode"*** N Channel JFET is given via "Microelectronic Circuits" by Sedra and Smith:

$$I_d = I_{DSS}\left[\,2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \qquad (1)$$

I_{DSS} = drain current when $V_{gs} = 0$. This "maximum" drain current is given in the specification sheet.

V_{gs} = gate to source voltage that is a non-positive voltage for an N Channel device.

V_p = pinch off voltage or cut off voltage. This is the voltage applied to the gate and source to provide zero drain current. The pinch off voltage, $V_p \leq 0$ volt for an N Channel JFET, is given in the specification sheet. Also, then $Vgs = Vp$, the drain to source resistance is infinite because there is no current flow into the drain of the FET.

V_{ds} = drain to source voltage. This can be the AC voltage across drain and source such as Vout in Figures 3, 4, 5, and 6.

Equations (1) through (5) are valid only when $V_p \leq V_{gs} \leq 0$ volt for an N Channel JFET in the ohmic, triode, or linear region.

The conductance, g_{ds}, is given by taking the derivative of I_d with respect to V_{ds}.

$$g_{ds} = \frac{d}{dVds} I_{DSS}\left[\,2\left(1 - \frac{Vgs}{Vp}\right)\left(\frac{Vds}{-Vp}\right) - \left(\frac{Vds}{Vp}\right)\left(\frac{Vds}{Vp}\right)\right] \qquad (2)$$

$$g_{ds} = I_{DSS}\left[\,-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right) - 2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right)\right] \qquad (3)$$

The resistance, R_{ds} is then the reciprocal of the conductance, g_{ds}

$$R_{ds} = 1/g_{ds} = 1/\{\, I_{DSS}\left[\,-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right) - 2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right)\right]\,\} \qquad (4)$$

Equation 4 shows that R_{ds} is non-linear resistor based on the fixed parameters I_{DSS}, V_p, and a fixed gate to source voltage Vgs with a dependence on the (AC signal's) voltage across the drain and source, V_{ds}.

For a first approximation for small signals across the drain and source, where$V_{ds} \rightarrow 0$

$$\text{term: } -2\left(\frac{Vds}{Vp}\right)\left(\frac{1}{Vp}\right) \rightarrow 0$$

This leads to:

$$R_{ds} = 1/\{I_{DSS}\left[\,-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right)\right]\} \qquad (5)$$

Equation (5) then is a function of fixed parameters, I_{DSS}, Vp, and the fixed gate to source voltage V_{gs}. The voltage controlled "linear" resistance is then set by the V_{gs} voltage.

For example, if Vp = -1.5 volts, V_{gs} = - 1.0 volt, and I_{DSS} = 0.005 A = 5 mA, then

$$R_{ds} = 1/\{I_{DSS}\left[\,-2\left(\frac{1}{Vp}\right)\left(1 - \frac{Vgs}{Vp}\right)\right]\} = 1/\{0.005A\left[\,-2\left(\frac{1}{-1.5v}\right)\left(1 - \frac{-1.0v}{-1.5v}\right)\right]\} = 450\Omega = R_{ds}$$

From equation (5), if we set V_{gs} = *Vp*, then the drain to source resistance will be infinite (e.g., open circuit):

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\}$$

$$R_{ds} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vp}{Vp}\,)]\} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\,1\,)]\}$$

$$R_{ds} \rightarrow 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,0\,)]\} \rightarrow (1/0)\Omega \rightarrow \text{infinite ohms}$$

$$R_{ds} \rightarrow \text{infinite ohms for } Vgs = Vp$$

Now let's look at what happens when we want minimum resistance by setting V_{gs} = 0 volt for an N Channel JFET.

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,-\tfrac{Vgs}{Vp}\,)]\} = R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1-\tfrac{0v}{Vp}\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1-0\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})(\,1\,)]\}$$

$$R_{ds} = 1/\{I_{DSS}\,[\,-2\,(\tfrac{1}{Vp})]\}$$

Or better yet for *Vgs* = 0 volt, this reduces to an easier form:

$R_{ds} = Vp/[-2I_{DSS}]$

For example, if again *Vp* = -1.5 volts and I_{DSS} = 0.005 A = 5 mA, with V_{gs} = 0 volt

R_{ds} = -1.5 v/[-2(0.005 A)] = -1.5 v/[-0.01 A] = 1.5 v/0.01 A = 150Ω

R_{ds} = 150Ω

Figure 4 shows a P Channel FET attenuator circuit. It works similarly to **Figure 3**, except that the gate's control voltage is positive to cut off Q2 for a minimum attenuation. Again, we get maximum attenuation when the gate voltage is zero or grounded.

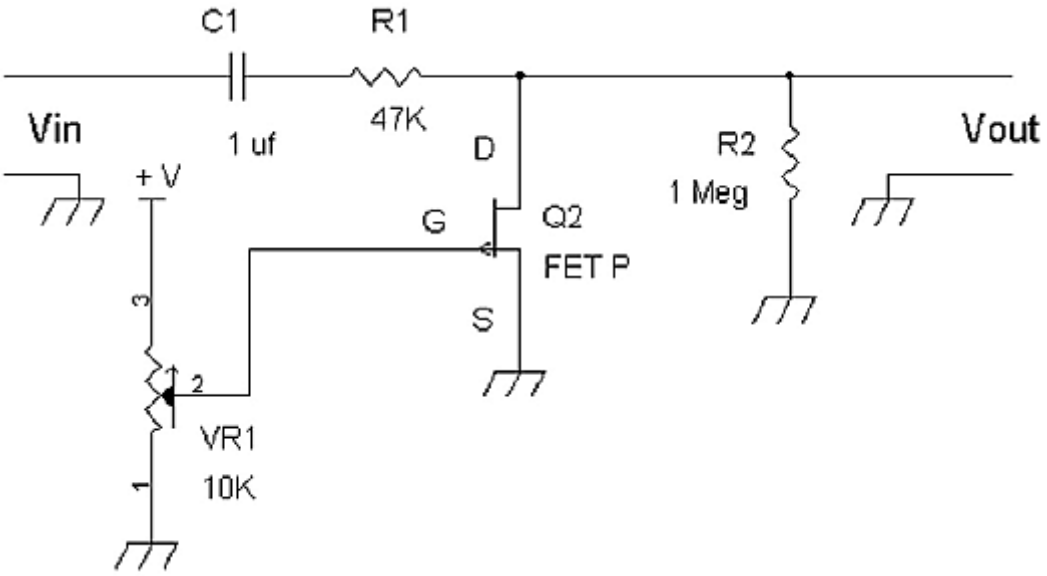

Figure 4 P Channel JFET attenuator circuit.

MOSFETs used as voltage controlled resistors

In **Figure 5**, MOSFETs have also been used as voltage controlled resistors. Because most MOSFETs today tend to be "***enhancement mode"***, this means that the required biasing at the gate is a positive voltage to turn on the drain current to lower its R_{ds}. Thus, if the gate voltage is 0 volts, the MOSFET is turned off.

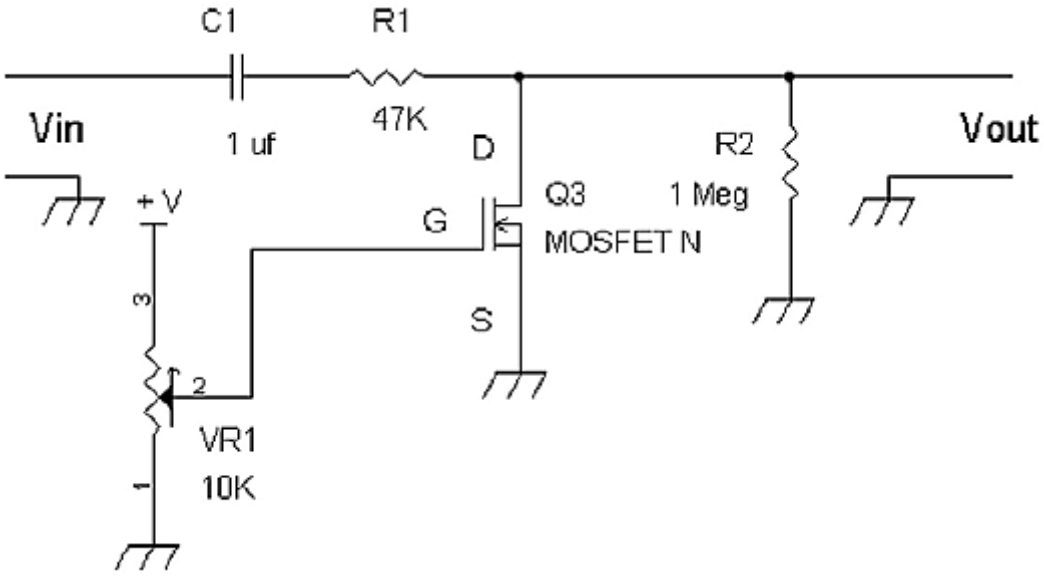

Figure 5 N Channel MOSFET attenuator circuit

With an N Channel enhancement mode device, Q3, at zero volts the attenuator passes the input signal to Vout with minimum attenuation. If VR1 is set to a positive voltage greater than the ***threshold voltage***, V_{th}, Q3's drain to source resistance will start to drop. Note that the threshold voltage, $V_{th} > 0$ volt for an N Channel MOSFET

From "Analysis and Design of Analog Integrated Circuits" by Gray and Meyer, the drain current of an N Channel MOSFET is characterized by equation (6):

$$I_d = \frac{k'}{2}\frac{W}{L}\left[2(V_{gs} - V_{th})V_{ds} - (V_{ds})(V_{ds})\right] \qquad (6)$$

Where:

$k' = \mu_n C_{ox}$

$C_{ox} = \varepsilon_{ox} / t_{ox}$

W = width of the MOS device

L = channel length of the MOS device

It should be noted that most discrete MOSFET spec sheets will not list $k' = \mu_n C_{ox}$, $C_{ox} = \varepsilon_{ox} / t_{ox}$ W and L. Instead, they will give a plot of typical IV curves and threshold voltage ranges.

If we look at equation (1) for an N Channel JFET, we will see that equation (6) is very similar. Note that they both include a " - (*Vds*)(*Vds*)" term, which results in a nonlinear resistance.

To reiterate, the N Channel JFET's equation is:

$$I_d = I_{DSS} \left[2\left(1 - \frac{Vgs}{Vp} \right)\left(\frac{Vds}{-Vp} \right) - \left(\frac{Vds}{Vp} \right)\left(\frac{Vds}{Vp} \right) \right] \qquad (1)$$

Figure 6 shows a P Channel MOSFET voltage controlled resistor circuit.

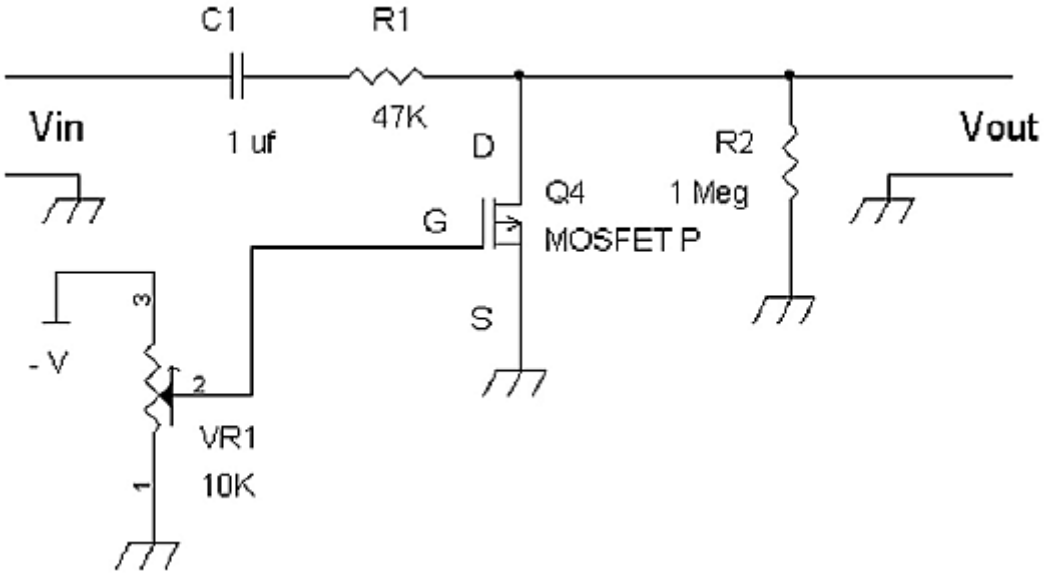

Figure 6 P Channel MOSFET attenuator circuit.

With a P Channel enhancement mode device, Q4, at zero volts the attenuator passes the input signal to Vout with minimum attenuation. If VR1 is set to a more negative voltage than the threshold voltage, V_{th}, Q4's drain to source resistance will start to drop. Note the threshold voltage for the P Channel MOSFET is a negative voltage (e.g., $V_{th} < 0$ volt).

Generally, the attenuator circuits shown in **Figures 5 and 6** will allow for reasonably small harmonic distortion for small signals, < 500 mV peak to peak at Vout. If there is distortion, second order harmonic distortion will be dominant.

A balanced or push pull VCR circuit

We can further linearize or reduce substantially second order distortion by making a push-pull circuit as shown in **Figure 7**. In particular, having a dual matched FET (e.g., VCR11N, LSK489, LSK389, etc.) allows for even order distortion cancellation.

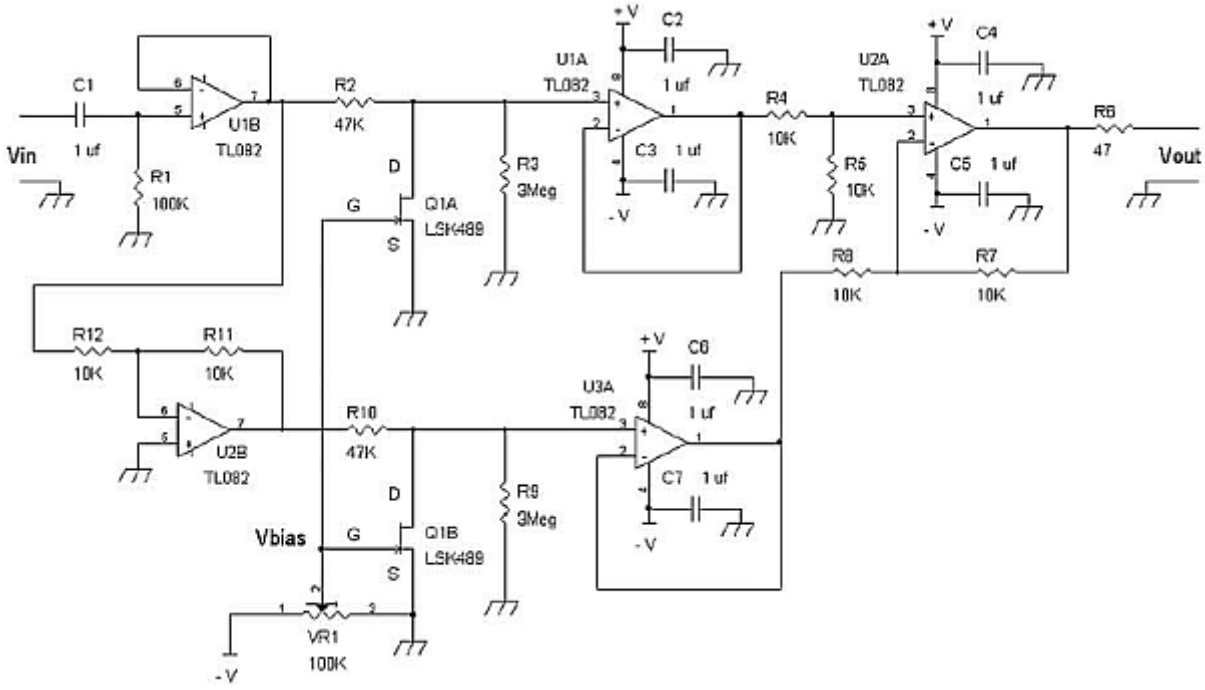

Figure 7 N Channel balanced configuration example for lowering distortion using a dual matched FET, LSK489, Q1A and Q1B.

A push pull or balanced VCR attenuator circuit cancels or reduces the second order distortion. In **Figure 7**, U1B buffers the input signal Vin, and drives the first voltage controlled attenuator circuit with Q1A (one half of the dual FET package). Vbias, which is shown as a variable DC negative voltage varies Q1A's drain to source resistance to provide a voltage controlled voltage divider circuit via series resistor R2. Voltage follower amplifier U1A buffers Q1A's drain terminal's voltage controlled attenuated signal. Note that FET input op amps such as TL082, TL062, LF353, AD712, etc. are generally used with high impedance input resistors such as R3 and R9.

Op amp circuit R12, R11, and U2B form an inverting amplifier that sends an out of phase signal to the second voltage controlled attenuator circuit via R10. Q1B's gate has the same Vbias signal that allows for matched attenuation characteristics across the drains and sources of Q1A and Q1B. Voltage follower U3A buffers the voltage controlled attenuated out of phase signal via Q1B's drain. A differential amplifier formed by U2A, R4, R5, R7, and R8 subtracts the outputs from U1A and U3A to cancel out second order distortion via Vout. See below for more details.

At this point, there are second order distortions at both Q1A's and Q1B's drain that are in phase. The reason is that second order distortion implies an x^2 function.

But observe that squaring a negative signal and squaring a positive signal gives the same result. That is

$(- x)^2 = (+ x)^2$

The output signals can be characterized as the following:

a_1 = linear **voltage divider** coefficient

a_2 = second order distortion coefficient

For the non-inverting signal, U1A pin 1 = a_1 Vin + a_2 $(Vin)^2$

For the inverting signal, U3A pin 1 = a_1 (- Vin) + a_2 $(- Vin)^2$

Note that: $(Vin)^2 = (- Vin)^2$

So, we have for the inverting signal,

U3A pin 1 = - a_1 Vin + a_2 $(Vin)^2$

Differential amplifier U2A performs a subtraction of the non-inverting and inverting signals from U1A pin 1 and U3A pin 1, we have:

a_1 Vin + a_2 $(Vin)^2$ - [- a_1 Vin + a_2 $(Vin)^2$] = a_1 Vin + a_2 $(Vin)^2$ + a_1 Vin - a_2 $(Vin)^2$ =

a_1 Vin + a_1 Vin + a_2 $(Vin)^2$ - a_2 $(Vin)^2$ = $2a_1$ Vin + 0 $(Vin)^2$ = $2a_1$ Vin

Note that a_2 $(Vin)^2$ - a_2 $(Vin)^2$ = 0

Thus, the output of differential amplifier circuit U2A pin 1 = $2a_1$ Vin, and note the absence of the second order distortion term. What this means is that we get a voltage controlled attenuated signal amplified by 2, and without the second order distortion.

Note that **Figure 7** shows an N Channel JFET example, but the basic principle of push pull or balanced operation can be applied to P Channel JFET, N Channel MOSFET, and P Channel MOSFET voltage controlled attenuator circuits shown in Figures 4, 5, and 6 respectively.

Alternatively, we can apply feedback to the basic voltage controlled resistor circuit to substantially remove second order distortion. When we apply this feedback, ***the output signal distorts symmetrically***. This implies mostly odd order distortion products.

In Part 2 of this series we'll look at examples.

Ron Quan is an author, design engineer, and inventor with over 75 US patents.

Related articles:

- A guide to using FETs for voltage controlled circuits, Part 2
- Use a photoelectric-FET optocoupler as a linear voltage-controlled potentiometer
- Building a JFET voltage-tuned Wien bridge oscillator