A 4-D chaotic oscillator based on a differential hysteresis comparator

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A 4-D Chaotic Oscillator Based on a Differential Hysteresis Comparator

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***Abstract*— A design approach for higher orders of chaotic systems is proposed. The chaotic oscillator presented is hierarchically modeled and simulated at the system, building-block, and circuit levels. The approach shows that the finite response times of hysteresis elements can be used to increase the order of differential hysteresis comparators. The hysteretic comparator demonstrated is a differential hysteresis which provides two orders of freedom and three possible output values. Experimental results are given for a triple-scroll chaotic oscillator constructed using a *RC*-opamp design approach. Results from the experimental four-dimensional system are in good agreement to theoretical results.**

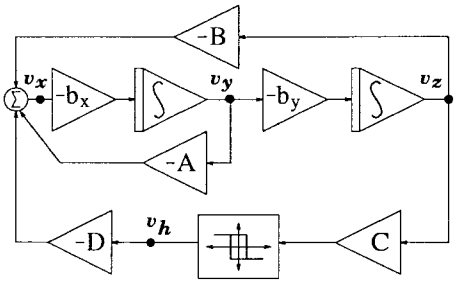

Fig. 1. Block diagram of 3-D tuned chaotic oscillator.

I. Introduction

MUCH has been investigated recently in exploring chaotic behavior, the design of chaos, and its properties. In response to this interest, circuit designers have been investigating ways of realizing these mathematical systems in a variety of monolithic implementations using various signal processing systems and nonlinear functions [1]–[3]. Most of these realizations have been single-ended in design, with nonlinear building blocks constructed to meet the requirements of the mathematical system. All such systems can, of course, be extended to fully-differential implementations [4]. However, without proper incentive (e.g., improved linearity, larger S/N ratio), this effort is not easily justified.

Recently, four-dimensional hysteretic chaotic systems [5]–[7] have been investigated. These higher order systems have been realized by adding additional linear storage elements to existing 3-D chaotic systems. In one case where this method of generating 4-D chaos has been realized, the system includes a hysteresis nonlinearity and has been designed to be single-ended. The result is a system that can be described by two symmetric linear equations which are connected to each other by hysteresis switchings [8]. The investigation described here is similar, but has been designed for use in a fully-differential hysteresis circuit implementation. Here we may exploit the common-mode response of the hysteresis element to increase the number of hysteresis switching states or levels, such that the order of the system is increased, not by increasing the number of linear storage elements, but by increasing the number of hysteresis storage regions.

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We begin with a discussion on chaotic oscillator design using a simple feedback system with a hysteresis nonlinearity in Section II. This discussion is followed by a presentation of the macromodels used to investigate the proposed design approach. Section III includes these macromodels and provides a system level simulation of a 4-D chaotic oscillator using the proposed hysteresis comparator. This section is followed by a discussion of higher order chaos, and gives simulation results for a quintuple-scroll chaotic oscillator using the proposed design approach. In Section V, a practical implementation of the proposed 4-D chaotic oscillator is given with measured results showing the feasibility of the proposed design approach. Finally, conclusions are given in Section VI.

II. Chaotic Oscillator Design

Here we will consider a simple tuned chaotic oscillator with a positive feedback loop which includes a hysteresis element [9], [10]. A block diagram of this 3-D system is given in Fig. 1. The linear portion of the system is of second order, comprised of linear intergrators and amplifiers. This quadrature-type oscillator is designed such that its complex conjugate poles are in the right half plane. This would normally lead to an unstable system, if it were not for the limiting action of the hysteresis feedback loop. Note in Fig. 1 that the output of the hysteresis element is negative in sign. The set of differential equations describing this system are

$$\frac{dv_x}{dt} = -D \cdot \frac{dv_h}{dt} + Bb_y v_y + Ab_x v_x \tag{1}$$

$$\frac{dv_y}{dt} = -b_x v_x \tag{2}$$

$$\frac{dv_z}{dt} = -b_y v_y \tag{3}$$

For the 3-D system, the function $h_1(\cdot)$ is the normalized hysteresis function. The time response of the system at v_z can

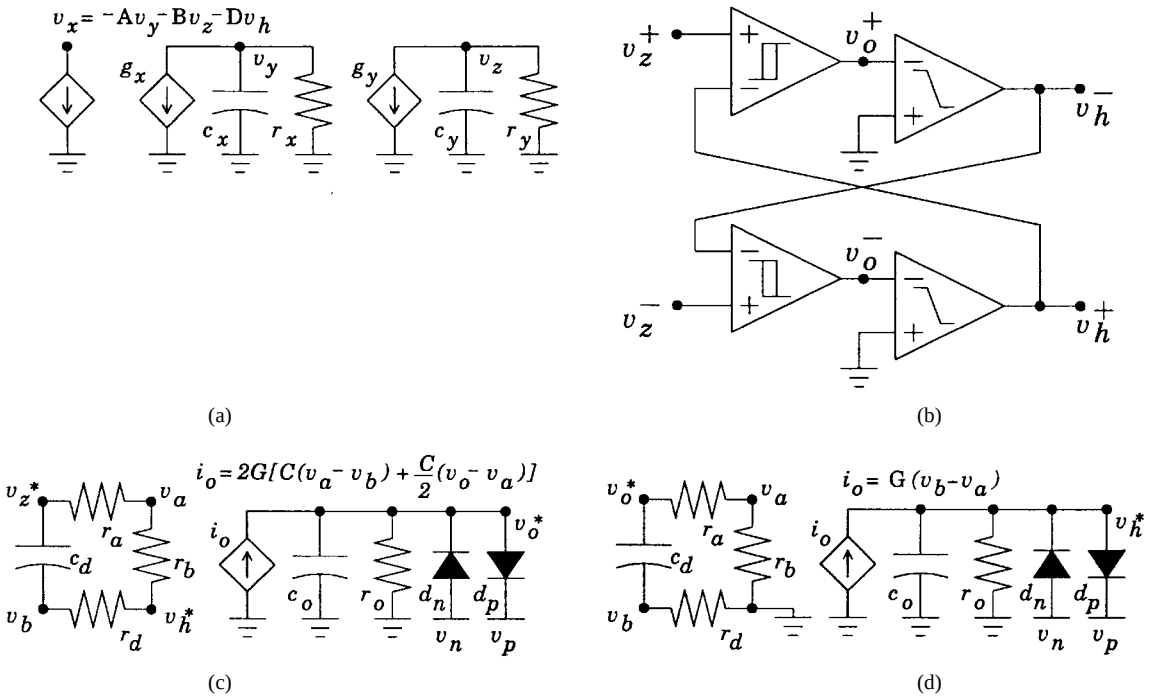

Fig. 2. Hspice models for 4-D chaotic oscillator. (a) Circuit model of quadrature-type oscillator. (b) Block diagram of differential hysteresis comparator. (c) Circuit model of hysteresis element. (d) Circuit model of comparator.

be described by the following equations inbetween hysteresis switchings:

$$v_z(t) = \frac{D}{B}\cdot h_1(v_z(t)) - \exp(Ab_x t/2)[C_1\cdot\cos(\omega t) - C_2\cdot\sin(\omega t)] \quad (4)$$

$$C_1 = \frac{D}{B}\cdot h_1(v_z(t)) - v_z(0), C_2 = \frac{Ab_x}{2\omega}\cdot C_1 \quad (5)$$

$$\omega = \frac{1}{2}\sqrt{4Bb_xb_y - A^2b_x^2} \quad (6)$$

From (4), we may note that the average value of the state variable $v_z(\cdot)$ depends on the output value of the hysteresis element $h_1(\cdot)$ in between switchings. For the conventional 3-D system, only two output values are given from the hysteresis element, and only one energy storage region. However, the investigation presented here proposes a 4-D oscillator based on a fully-differential hysteresis implementation where three hysteresis output values are possible and two energy storage regions exists. Thus, with this hysteresis comparator, the order of the 3-D system presented can be increased to four [11].

III. 4-D Chaotic Oscillator Macromodel

The 3-D system shown in Fig. 1 has been constructed in both single-ended and fully-differential implementations [4], [12]. In considering the proposed implementation, we may replace the normalized hysteresis element $h_1(\cdot)$ with the proposed hysteresis comparator $h_2(\cdot)$. Then, the design can be separated into two parts: the linear portion and the hysteresis. Macromodel building blocks for both parts appear in Fig. 2. The linear portion, shown in Fig. 2(a), is comprised of a voltage-controlled voltage source to implement a voltage summation, and two voltage-controlled current sources g_x, g_y with capacitors c_x, c_y to implement voltage integrators. Output resistors r_x and r_y are large in value in order to keep the integrations close to ideal.

The block diagram of the proposed differential hysteresis comparator $h_2(\cdot)$ is shown in Fig. 2(b). It is comprised of two voltage hysteresis elements and two voltage comparators. A circuit macromodel for the hysteresis appears in Fig. 2(c). It is comprised of an all-pass filter whose phase delay is determined by r_d and c_d when $r_a = r_b$, and a transconductance output stage with positive feedback. The output values of the hysteresis is bounded by the diodes d_p and d_n, and voltages v_p and v_n. The circuit macromodel for the voltage comparator as

$$v_h(t) = v_h^+(t) - v_h^-(t) = h_2(v_z^+(t) - v_z^-(t)) = h_2(v_z(t)) \quad (7)$$

where $h_2(\cdot)$ denotes a hysteresis function with two storage regions. The macromodels for the hysteresis and comparator functions are given in Fig. 2(c) and (d), respectively. For each macromodel, we have identical output stages, and may write this nonlinear output function in the time domain:

$$c_o\frac{dv_o^*(t)}{dt} + \frac{v_o^*(t)}{r_o} = \frac{1}{2}\left(\left|i_o(t) + \frac{v_p}{r_o}\right| - \left|i_o(t) + \frac{v_n}{r_o}\right|\right) \quad (8)$$

$$c_o\frac{dv_h^*(t)}{dt} + \frac{v_h^*(t)}{r_o} = \frac{1}{2}\left(\left|i_o(t) + \frac{v_p}{r_o}\right| - \left|i_o(t) + \frac{v_n}{r_o}\right|\right) \quad (9)$$

where $v_o^*(t)$ is the output of the hysteresis, v_h^* is the output of the comparator, r_o is the impedance at output nodes v_o^* and v_h^*, and v_p and v_n are the limiting voltages at output nodes through diodes d_p and d_n, respectively. It is assumed here that $v_p = -v_n$, and that the limiting voltages for the hysteresis are not equal to the limiting voltages for the comparator.

For each macromodel, an all-pass filter appears at each input comprised of $r_a = r_b, r_d$ and c_d. This filter is used to

model the finite response time of the hysteresis and comparator elements. Thus, $i_o(t)$ for the hysteresis in (8) can be written as

$$i_o(t) = 2GC \cdot [v_a(t) - v_b(t)] + CG \cdot \left[v_o^*(t) - \frac{v_z^*(t) + v_h^*(t)}{2} \right] \tag{10}$$

$$\left[\frac{dv_a(t)}{dt} - \frac{dv_b(t)}{dt} \right] + \frac{v_a(t) - v_b(t)}{r_d c_d} = -\frac{1}{2}\left[\frac{dv_z^*(t)}{dt} - \frac{dv_h^*(t)}{dt} \right] + \frac{1}{2}\,\frac{v_z^*(t) - v_h^*(t)}{r_d c_d} \tag{11}$$

where C is the system design parameter given in (1) and shown in Fig. 1, and G is the transconductance gain of the voltage-controlled current source. Note from (10) tht the hysteresis macromodel has local positive feedback. The limiting voltages v_p, v_n determine the trigger voltages as well as the upper limits of the output voltage. For the comparator, $i_o(t)$ in (9) is given by

$$i_o(t) = G \cdot [v_b(t) - v_a(t)] \tag{12}$$

$$\left[\frac{dv_b(t)}{dt} - \frac{dv_a(t)}{dt} \right] + \frac{v_b(t) - v_a(t)}{r_d c_d} = \frac{1}{2}\,\frac{dv_o^*(t)}{dt} - \frac{1}{2}\,\frac{v_o^*(t)}{r_d c_d} \tag{13}$$

Note in both (11) and (13) that a small value of voltage is accumulated over time across the integrating capacitor c_d. This accumulation gives rise to the nonzero response time of these nonlinear elements. We may complete this set of equations by solving (8)–(13) simutaneously with initial conditions for two sets of inputs and outputs, one set for each hysteresis/comparator pair, as illustrated in Fig. 2(b).

In the case of the comparator, the result from the macromodel in Fig. 2(d) above is a delay from input to output that is primarily a function of r_d and c_d. Thus, for a monolithic design with small parasitics that contribute to an all-pass input function at the input of the comparator, the comparator response time can often be made much smaller than the speed of its input signals, in turn contributing little to the dynamics of the system. However, in the case of the hysteresis element, the delay from input to output is multiplied by the gain of the feedback loop, making the response time of the hysteresis element much greater; typically the feedback gain is made large so that the hysteresis will switch quickly between output limit voltages. This result is further exacerbated by the coupling of output parasitics r_o and c_o to the all-pass response at the input through the feedback loop. The final result is a hysteresis element that is more sensitive to the speed of its input signal in relation to a comparator with similar parasitics, and results in a hysteresis element whose trigger voltages are a function of both the limiting voltages at its output and the speed of the input signal.

To understand its operation, consider again the differential hysteresis comparator in Fig. 2(b). If we first assume that each block has no delay, then it is clear that the proposed

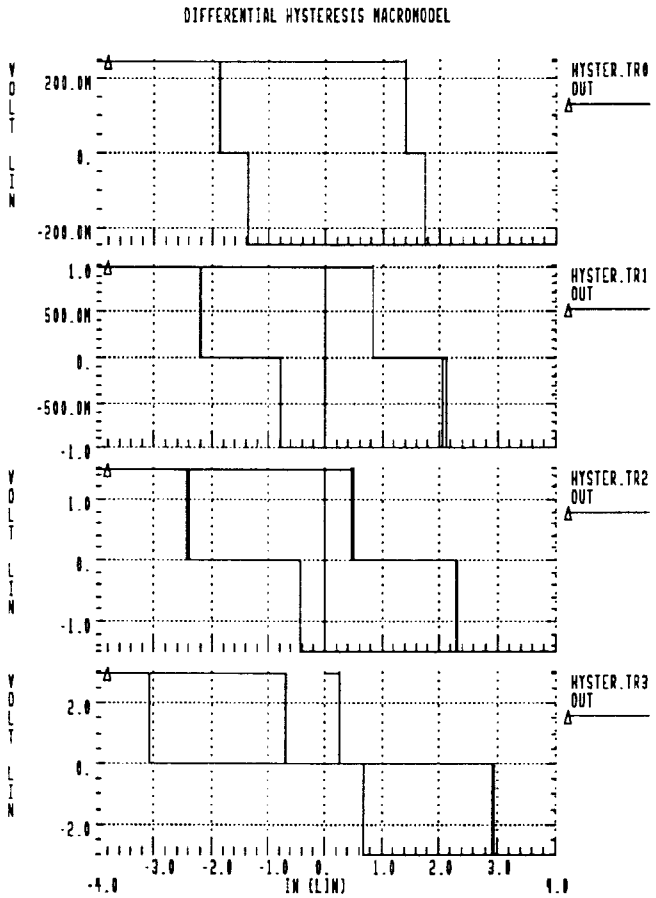

Fig. 3. Hspice simulations of macromodel of proposed hysteresis comparator for various output voltage limits. The horizontal axis is input voltage $v_z(t)$ and the vertical axis is output voltage $v_h(t)$.

comparator will be *fully-differential*[1] because of symmetry. However, if any delay is present, then is it possible for one of the hysteresis elements to change its output state before the other, even for a fully-differential input at v_z. This operation is illustrated in Fig. 3 for four different values of output voltage limits (v_p, v_n) from the output comparators. In the first trace, the output voltage limits are $(v_p, v_n) = (0.25, -0.25)$ V, in the second $(v_p, v_n) = (1.0, -1.0)$ V in the third $(v_p, v_n) = (1.5, -1.5)$ V, and in the fourth trace $(v_p, v_n) = (2.5, -2.5)$ V. From the figure, it can be observed that as the output voltage limits are increased, that is, as the reference voltages for both hysteresis elements are increased, the two hysteresis storage regions shift left and right. Also note spurious switching in each of the four simulation results. This result is due to zero initial conditions at the start of each simulation.

Given the operation of the proposed hysteresis comparator in Fig. 3, and the complete chaotic system in Fig. 1, we may design the chaotic system given in Fig. 1 using (4)–(6). Assuming that the absolute value of the output of the hysteresis comparator is unity, the location of the repelling points can be given by $r_{p1} = -r_{p2} = D/B, r_{po} = 0$. Given these parameters, the amount of divergence given by Ab_x can be adjusted until a chaotic response is obtained. For this example,

[1]We define differential as $v_h(t) = v_h^+(t) - v_h^-(t)$. The conventional definition of fully-differential includes the constraint that: $v_h^+(t) = -v_h^-(t)$.

```
Triple Scroll 4-D Macromodel
*
.subckt comparator in+ in- put cap=10.0p res=1.0k
vp   v2   0  0.5
vn    0  v3  0.5
dp  out  v2  diode
dn   v3 out  diode
ra  in+  va  0.5t
rb   va in-  0.5t
rp  in+  vb  res
cp   vb in-  cap
go    0 out  poly(2) va 0 vb 0 0 -10.0m 10.0m
ro  out   0  1meg
co  out   0  10n
eo  put   0  poly(1) out 0 0 1.0
.ends comparator

.subckt hysteresis in+ in- out cap=10.0p res=1.0k
vp   v2   0  1.0
vn    0  v3  1.0
dp  out  v2  diode
dn   v3 out  diode
ra  in+  va  0.5t
rb   va in-  0.5t
rp  in-  vb  res
cp   vb in+  cap
go  out   0  poly(2) vb va out va 0 -20.0m 10.0m
ro  out   0  1meg
co  out   0  10n
.ends hysteresis

.subckt diff-hys in out
ex  vz+ vz-  poly(1) in 0 0 4.0
xha vz+ vh-  va hysteresis cap=10.0p res=1.0k
xhb vz- vh+  vb hysteresis cap=10.5p res=1.0k
xca   0  va vh+ comparator cap=10.0p res=1.0k
xcb   0  vb vh- comparator cap=10.0p res=1.0k
eh   vh   0  poly(1) vh+ vh- 0 1.0
.ends diff-hys

gx   vy   0  poly(1) vx 0 0 1.0
rx   vy   0  1t
cx   vy   0  1.0m
gy   vz   0  poly(1) vy 0 0 1.0
ry   vz   0  1t
cy   vz   0  0.1m
es   vx   0  poly(3) vy 0 vz 0 vh 0 0 -0.65 -1.5 -2.4
ec   vc   0  poly(1) vz 0  0 0.63
xh   vc  vh  diff-hys

.model diode d(is=1.0f n=0.001)
.options post=1 method=gear accurate interp
.tran 20u 0.2 uic
.ic v(vz)=-0.30
.fft v(vy) np=1024 format=norm window=harris
.end
```

Fig. 4. Hspice input file of 4-D chaotic oscillator macromodel.

values of $A = 0.65, B = 1.5, C = 0.63, D = 2.4, b_x = 1$ krad/s, and $b_y = 10$ krad/sec were chosen. For the hysteresis comparator $h_2(\cdot)$, the output limits are chosen at ± 0.5 V, and normalized hysteresis elements are used. This is the design used in the Hspice input file that appears in Fig. 4. Note from the Hspice input file that the delays in each building block of the hysteresis comparator are small, and that one value of capacitance is different from the others. This was done to insure that one forward path of the hysteresis comparator was slightly faster than the other to break the symmetry of the feedback in the hysteresis system. Simulation results for this Hspice input file appear in Fig. 5.

In the top traces of Fig. 5, the signals $v_z(t), v_y(t), v_x(t)$, and $v_h(v_z(t))$ from Fig. 1 using the proposed differential

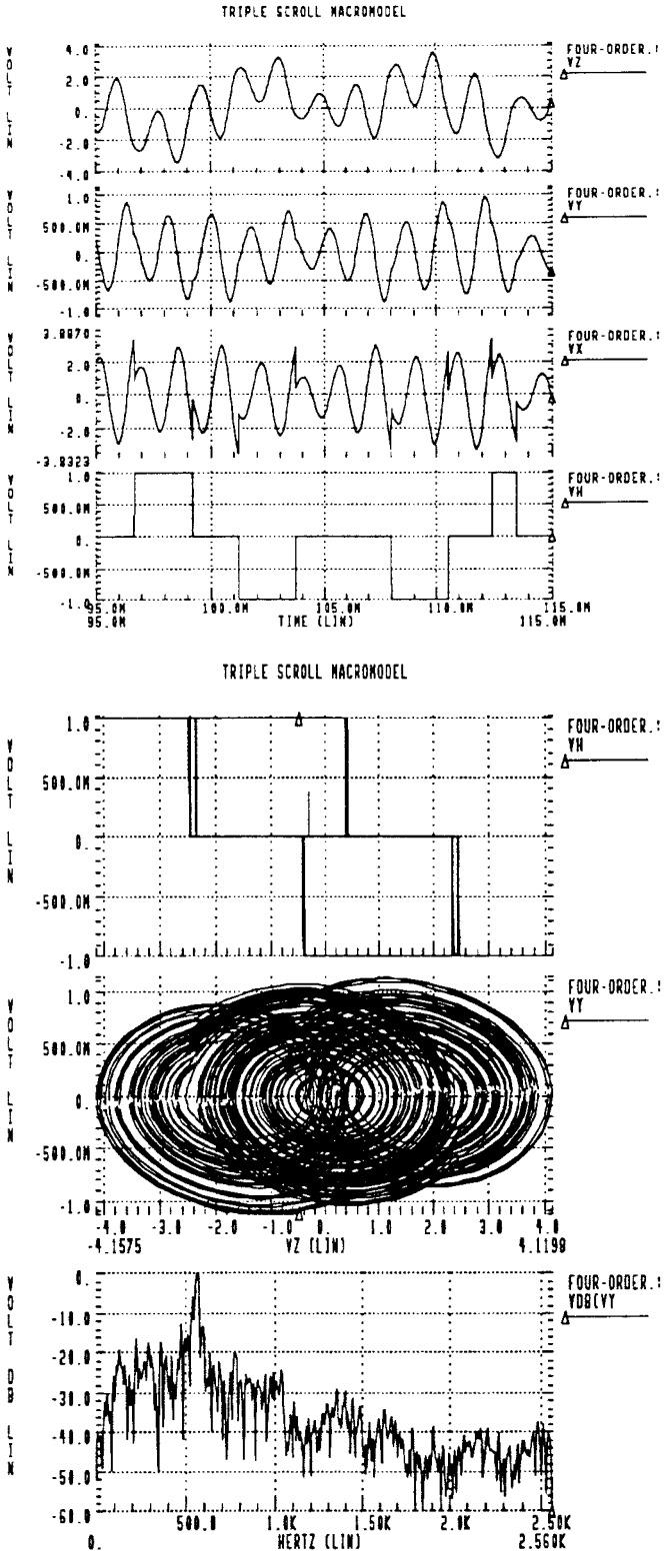

Fig. 5. Hspice simulation of 4-D chaotic oscillator.

hysteresis element are given. Note that for the signal $v_z(t)$, the response closely resembles the expression given in (4), that is, an exponentially growing sinusoidal response with an average value related to the output value of the hysteresis comparator $h_2(\cdot)$. Also note that the signal $v_z(t)$ is "restarted" each time it exceeds the normalized thresholds of the hysteresis for this system. This "restarting" can be observed in the trace

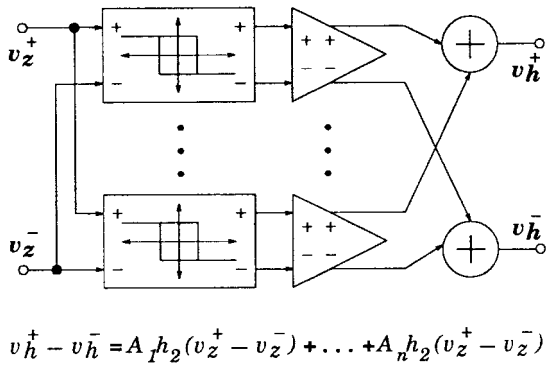

Fig. 6. Block diagram of design approach for higher order hysteresis.

of $v_x(t)$. The output of the hysteresis $v_h(v_z(t))$ is given in the fourth trace of Fig. 5. However, by comparing the signal $v_h(v(t))$ with the signal $v_z(t)$, we may observe the shape of the proposed second-order hysteresis comparator. Also, by comparing the signal $v_y(t)$ with the signal $v_z(t)$, we may observe the triple-scroll geometry of the chaotic response. Finally in Fig. 5, by using an FFT on the time response we may observe the frequency spectrum of the signal $v_y(t)$ and note that the natural oscillating frequency at 560 Hz is the largest component in the spectrum.

IV. Higher Order Chaos

The chaotic system described above is of fourth order, using a second-order linear tuning section and a second-order hysteresis comparator. The order of the system can be further increased by increasing the complexity of the hysteresis, as shown in Fig. 6. By constructing more than one of the proposed differential hysteresis comparators, and placing them in parallel, two or more differential hysteresis outputs can be generated. By adjusting the output voltage limits of the comparators within each individual hysteresis comparator, the storage regions of each hysteresis comparator can be shifted, as was shown in Fig. 3. Finally, these individual outputs can be linearly combined to construct a composite differential hysteresis output, whose order will be equal to $2n$, where n is the number of individual differential hysteresis comparators:

$$v_h = v_h^+ - v_h^- = A_1 h_2(v_z^+ - v_z^-) + \cdots + A_n h_2(v_z^+ - v_z^-) = h_{2n}(v_z) \tag{14}$$

Using this approach, a sixth-order chaotic oscillator was simulated using the macromodels described above. The oscillator is constructed from one second-order linear tuning stage and two differential hysteresis comparators whose outputs were linearity combined to produce a fourth-order hysteresis $h_4(\cdot)$. The results of this simulation appear in Fig. 7.

The time responses for $v_z(t), v_y(t), v_x(t)$, and $v_h(v_z(t))$ are given in the top four traces of Fig. 7. Note in the first trace that the signal $v_z(t)$ now takes on five average values in between hysteresis switchings, while the signals $v_y(t)$ and $v_x(t)$ look very much like those given for the fourth-order system in Fig. 5. The shape of the hysteresis is given in the the fifth trace of Fig. 7. Note from this trace that the hysteresis element has four storage regions. Also note, however, the "blurring" of the

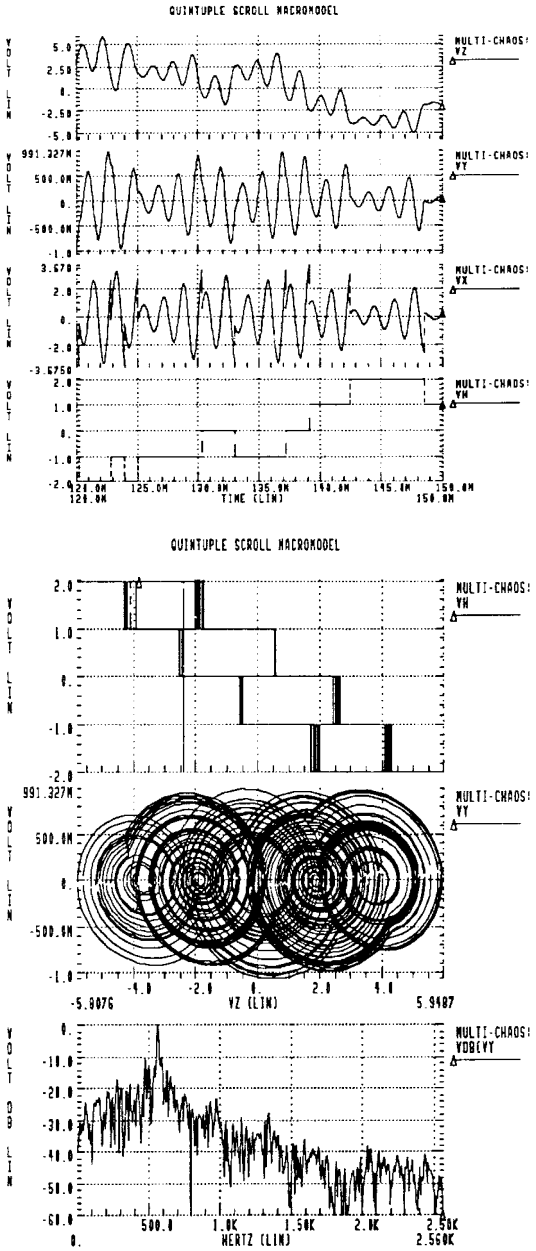

Fig. 7. Hspice simulation of 6-D chaotic oscillator.

switching transitions. This blurring is due to the sensitivity of the hysteresis elements $h_1(\cdot)$ in each of the differential hysteresis comparators $h_2(\cdot)$ to the speed of their input signals. As the speed of the input signal varies, the trigger voltage also varies, resulting in the blurring effect shown. The sixth trace of this figure gives the quintuple-scroll geometry of the chaotic response. Finally, using an FFT on the time response, we may observe the frequency spectrum of the signal $v_y(t)$ in the last trace of Fig. 7. Note that the natural oscillating frequency at 560 Hz and profile of the spectrum has changed little from the fourth-order system given in Fig. 5.

V. Practical Implementation

To verify the proposed design approach for higher order chaotic systems, an *RC*-opamp implementation of a 4-D

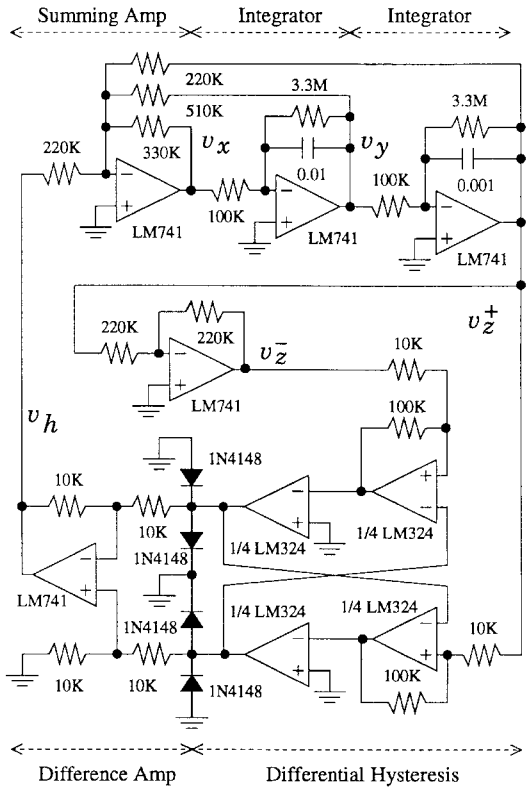

Fig. 8. *RC*-opamp implementation of 4-D chaotic oscillator.

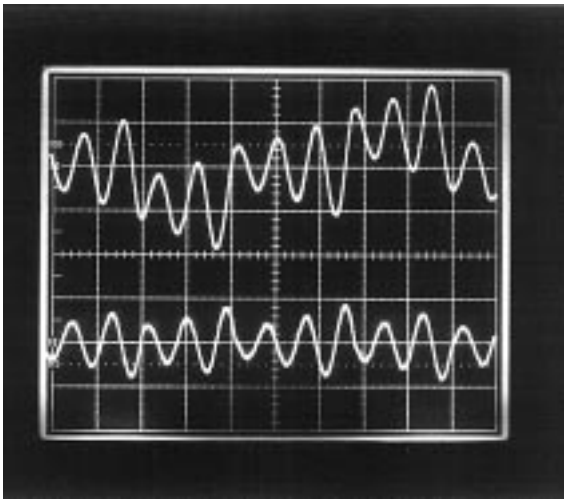

Fig. 9. Measured results from RC-opamp implementation: The top trace is $v_z(t)$ at 2 volts/div and the bottom trace is $v_y(t)$ at 1 V/div. Time scale is 2 ms/div.

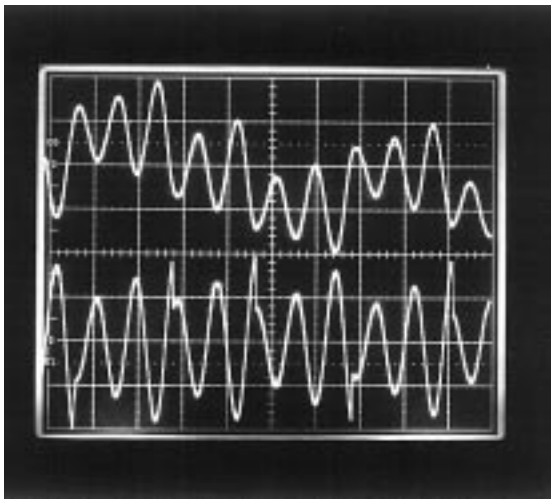

Fig. 10. Measured results from *RC*-opamp implementation: The top trace is $v_z(t)$ at 2 V/div and the bottom trace is $v_x(t)$ at 2 volts/div. Time scale is 2 ms/div.

chaotic system was constructed. The circuit schematic for the system appears in Fig. 8. The linear portion of the system is designed as for the macromodel presented above, and includes an inverting summing amplifier and two inverting integrators. Note that this linear portion is single-ended. The output of the second integrator $v_z(t)$ then passes through an inverting amplifier, so that this signal $v_z(t)$ is now fully-differential with a common-mode voltage at ground. The first integrator has an integrating constant $b_x = (0.01\ \mu\text{F} \cdot 100\ \text{k}\Omega)^{-1} = 1$ krad/s, and the second integrator has $b_y = (0.001\ \mu\text{F} \cdot 100\ \text{k}\Omega)^1 = 10$ krad/s. The voltage summer has inverted gains of $A = -330\ \text{k}\Omega/510\ \text{k}\Omega = -0.65$ V/V, $B = -330\ \text{k}\Omega/220\ \text{k}\Omega = -1.5$ V/V, and $D' = -330\ \text{k}\Omega/220\ \text{k}\Omega = -1.5$ V/V.

The differential hysteresis is then constructed from four opamps. Two opamps are connected with positive feedback to give single-ended hysteresis elements, and the other two are left in the open-loop configuration to provide the comparator functions as given in the macromodel above. If the voltage required to trigger an individual hysteresis element is normalized to unity, the gain C of the proposed chaotic system can be given as

$$C = \left[2 \cdot |v_D| \left(\frac{10\ \text{k}\Omega}{100\ \text{k}\Omega} + 1\right)\right]^{-1} = 0.57\ \text{V/V}$$

The outputs of the comparator opamps are clamped to approximately $|v_D| = \pm 0.8$ volts by the use of silicon diodes, while the outputs of the hysteresis elements are clamped to the supply voltages. Switching could be improved at the outputs of the comparator opamps by connecting a resistor from the outputs to the clamping diodes. The output of the differential hysteresis is converted back into a single-ended signal $v_h(\cdot)$ using an op-amp difference amplifier with unity gain. If we normalize the differential output of the hysteresis comparator, assuming that the outputs are clamped by the diodes to $|v_D| = \pm 0.8$ V, the gain of D can be computed as $D = D' \cdot (2|v_D|) = 2.4$ V/V.

The measured results from the opamp realization appear in Figs. 9–14. The photograph in Fig. 9 shows the signals $v_z(t)$ and $v_y(t)$, and can be compared with the traces from simulation shown in the top portion of Fig. 5. Similar results are shown in Figs. 10 and 11 for $v_z(t), v_x(t)$ and $v_z(t), v_h(v_z(t))$, respectively. The shape of the hysteresis in the opamp realization is illustrated in Fig. 12, where the signal $v_h(t)$ is measured against $v_z(t)$. This result compares closely to the simulation shown for the hysteresis in Fig. 5, and gives validity to the macromodel presented for the proposed differential hysteresis. Also, by measuring $v_y(t)$ against $v_z(t)$, we may observe the

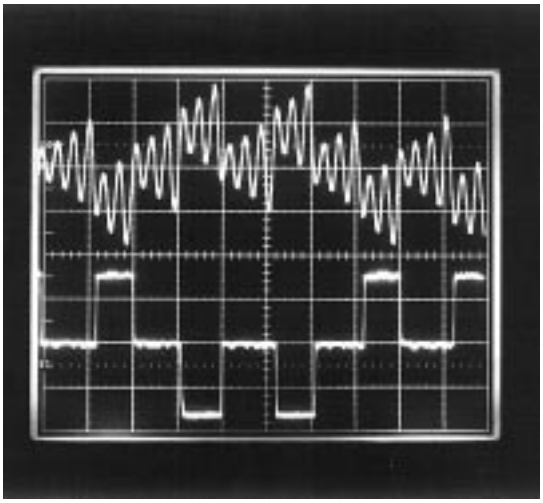

Fig. 11. Measured results from *RC*-opamp implementation: The top trace is $v_z(t)$ at 2 V/div and the bottom trace is $v_h(t)$ at 1 V/div. Time scale is 5 ms/div.

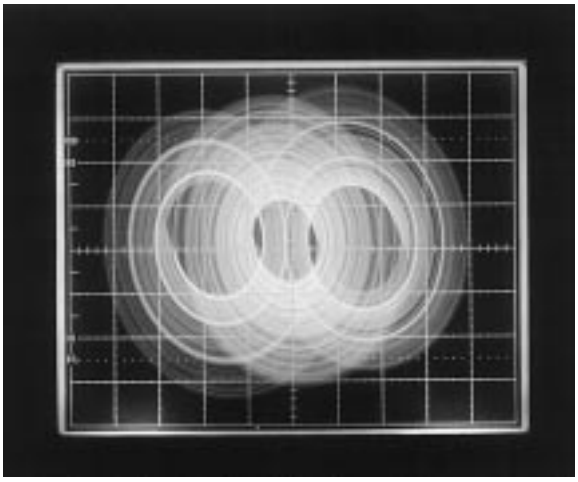

Fig. 13. Measured results from *RC*-opamp implementation: $v_y(t)$ versus $v_z(t)$. The vertical axis is $v_y(t)$ at 200 mV/div and the horizontal axis is $v_z(t)$ at 1 V/div.

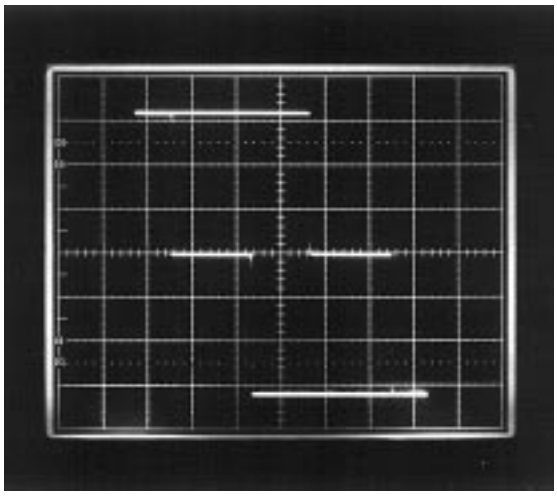

Fig. 12. Measured results from *RC*-opamp implementation: $v_h(t)$ versus $v_z(t)$. The vertical axis is $v_h(t)$ at 0.5 V/div and the horizontal axis is $v_z(t)$ at 1 V/div.

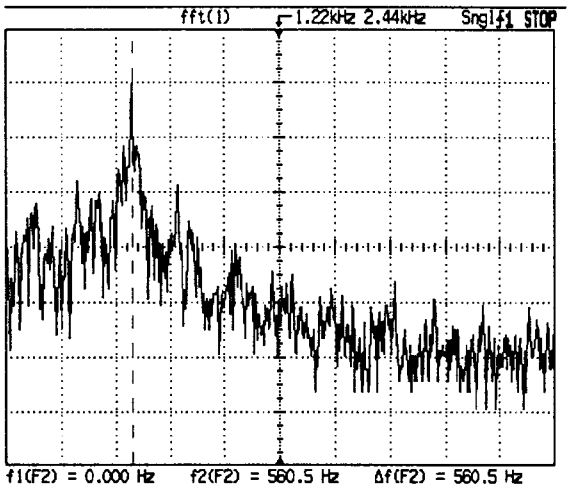

Fig. 14. Measured results from *RC*-opamp implementation: Frequency spectrum of $v_y(t)$.

triple scroll chaotic result shown in Fig. 13. Finally, we may observe the measured frequency spectrum of the signal $v_y(t)$ in Fig. 14, and note its similarity to the frequency spectrum given for the simulated macromodel, most notably the natural oscillating frequency at 560 Hz.

VI. Conclusions

We have presented a 4-D chaotic oscillator based on a differential hysteresis comparator. A macromodel of the proposed system was presented, and shows how the finite response times of hysteresis elements can be used to increase the order of differential hysteresis comparators. Simulation results for this model show a chaotic triple-scroll attractor. It was also shown how the proposed differential hysteresis comparator could be used to increase the order of the system further by using hysteresis comparators in parallel, then linearly combining their outputs to construct a higher order hysteresis. Simulation results using a fourth-order hysteresis comparator show a quintuple-scroll chaotic attractor. Finally, an *RC*-opamp implementation of the proposed system was presented, with measured results that show the functionality of the four-dimensional system.

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