ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

CMOS Ring Oscillator Gate Delay Lab

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11-15-16 CMOS_Ring_Oscillator_Lab.ppt

RISE TIME, FALL TIME AND PROPAGATION DELAY

The system speed is determined by many factors but the basic parameter that determines the speed of the system is the individual gate propagation delay, td. The propagation delay is often used as a figure of merit to compare different technologies. For example in 1997 IBM reported their measured ring oscillator propagation delay of 9.5ps the fastest reported to date for CMOS at room temperature.

The definition of propagation delay is the average of td_{LTH} and the td_{HTL} for the output of a gate (typically an inverter).

thus: $td = \frac{1}{2}(t_{LTH} + t_{HTL})$

These times are so fast they are hard to measure so td is typically extracted from the measured period of a ring oscillator. A ring oscillator is an odd number of inverters (N) in series with the output connected back to the input, which will oscillate with period T.

thus: $td = T/(2N)$

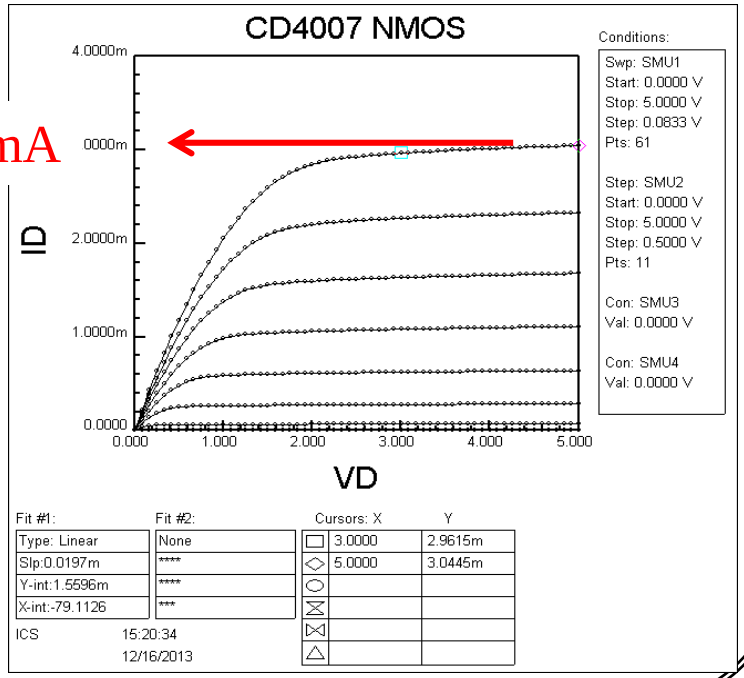
INTRODUCTION

In this lab we will investigate the propagation delay of CMOS inverters.

1. We will calculate inverter gate delay by hand using approximations for the internal capacitances and the charging/discharging of those capacitors.
2. We will use SPICE to obtain the inverter gate delay using models that represent the internal capacitances.
3. We will measure the gate delay by building a 5-stage ring oscillator and measuring the period of oscillation.
4. We will use SPICE to simulate the ring oscillator and compare our SPICE results to the measured results from the 5-stage oscillator.
5. Finally, we will determine the internal capacitance of the CMOS inverter from measured ring oscillator period by adding external capacitance to each stage in the oscillator and comparing the period to the ring oscillator period with no external capacitors

HAND CALCULATIONS

Lets assume the transistors charge an internal capacitance, Cint, consisting of the transistors self capacitance plus the gate capacitance of the input of a second inverter. We also assume that the current to charge or discharge these capacitors is a constant value appropriate for the gate voltage and supply voltage used. For example 5 or 0 volts on the inverter input, for supply voltage of 5 volts, will result in 3mA for CD4007 NMOS, when input is high, and 3mA for PMOS, when the input is low.



Q=CV and Q/t = I = CV/t

Combining gives t = CV/I

where C=Cint and V=Vs

If Cint=0.94pF (see next page) and

Vs=2.5volts (switching voltage)

Then the gate delay td = 3.84pF 2.5/3mA

=3200ps

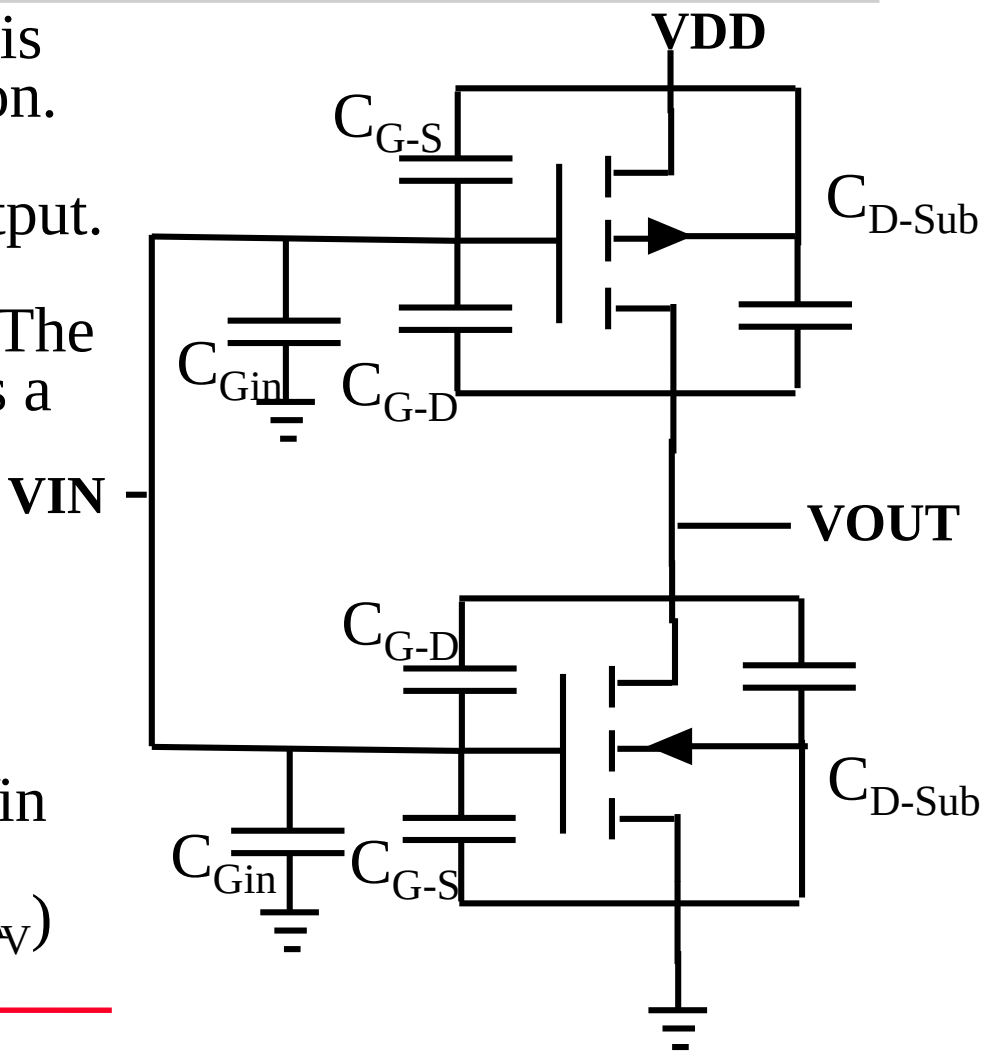
CMOS INVERTER SHOWING CAPACITANCE

During switching one transistor is off while the other is in saturation. The self capacitance is the capacitance connected to the output. One $C_{D\text{-}sub}$ and the overlap capacitance from gate to drain. The capacitance from gate to drain is a Miller capacitance and is $Cm' = C_{G\text{-}D}$

In this example:
$Cself = (C_{G\text{-}D} + C_{D\text{-}sub})$

C_{in} is everything connected to Vin Including miller effect

$$C_{in} = C_{Gin} + C_{G\text{-}S} + C_{G\text{-}D}(1 - A_V)$$



INTERNAL CAPACITANCE CALCULATION

	A	B	C	D	E	F	G	H	I	J
1	ROCHESTER INSTITUTE OF TECHNOLOGY							Capacitance_MOSFET.xks		
2	MICROELECTRONIC ENGINEERING							1/10/2015		
3										
4	CALCULATIONS FOR INTERNAL CAPACITORS IN A MOSFET							DR. LYNN FULLER		
5										
6	To use this spreadsheed change the values in the white boxes. The rest of the sheet is									
7	protected and should not be changed unless you are sure of the consequences. The									
8	calculated results are shown in the purple boxes.									
9										
10	CONSTANTS				VARIABLES					
11	K	1.38E-23	J/K							
12	q	1.60E-19	Coul		Temp=	300	°K			
13	Ego	1.12	eV							
14	εo	8.85E-14	F/cm							
15	εr (silicon)	11.7								
16	ni	1.45E+10	cm-3							
17	Breakdown E=	3.00E+05	V/cm							
18	er (Oxide)	3.90								
19	TECHNOLOGY DESCRIPTION							CALCULATIONS:		
20	VDD	5	Volts					DIODE CALCULATIONS		
21	L	10	um		Eg = Ego - (aT^2/(T+B)			1.075	eV	
22	W	170	um		ni^2 = A T^3 e^(-Eg/KT/q)			9.84E+20	cm-6	
23	well doping, Nsub	4.00E+15	cm-3		KT/q =			0.0259	Volts	
24	D/S doping, Nd	5.00E+17	cm-3		Vbi = (KT/q) ln (NaNd/ni2)			0.73	Volts	
25	D/S junction depth, Xj	0.5	um		WSC = [(2ε/q)(Vbi+Vr)(1/Na +1/Nd)]^0.5			1.37	µm	
26	Xox	600	Å		W1 =WSC[Nd/(Na+Nd)]			1.36	µm	
27	Fox	6500	Å		W2 =WSC[Na/(Na+Nd)]			0.01	µm	
28	Ad	8500	pm2		= -[(2q/eoer)(Vbi+Va)(NaNd/(Na+Nd)]^0.5			-3.00E+04	V/cm	
29	As	8500	pm2		Cj' = eoer/WSC			7.57E-05	F/m2 of D/S area	
30	Pd	440	um		Cjsw'=eoer Pd Xj/WSC			3.82E-11	F/m of D/S perimeter	
31	Ps	440	um		CGSO=eoer XL/Xox			5.75E-10	F/m of gate width	
32	WX Gate to FOX Overlap	10	um		CG-Bulk=eoerWX/Fox			5.31E-10	F/m of gate length	
33	XL D/S to Gate Overlap	1	um		OXIDE CAPACITOR CALCULATIONS					
34	Design Lambda	1	um		G-sub = C gate to bulk overlap=CG-Bulk*L			5.31E-15	F	
35	Av	15	V/V		CG-D=C gate to drain overlap			9.78E-14	F	
36					Cgin=C gate to channel			9.78E-13	F	
37					Cside=C drain junction side wall			1.68E-14	F	
38					Cbottom=C drain junction bottom			6.44E-13	F	
39					CD-sub=Cside+Cbottom			6.60E-13	F	
40					Cin=CGin+CGS+CGD(1-Av)			1.16E-12	F	
41					Cself=CD-sub + CG-D			7.58E-13	F	
42					Ctotal=			1.92E-12	F	

1.92pF

All the internal capacitances can be calculated from the equation, C=εoεr Area/d, where d is the oxide thickness or width of the space charge layer. This spreadsheet does the calculations for the capacitors shown on the previous page.

The total internal capacitance for the inverter (two transistors) with this technology (CD4007) is ~1.92pF x 2 = 3.84pF

INVERTER SPICE SIMULATION

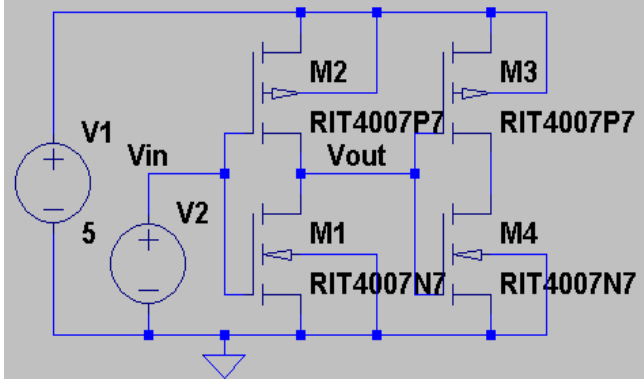
All NMOS L=10u W=170u Ad=8500p AS=8500p PD=440u PS=440u

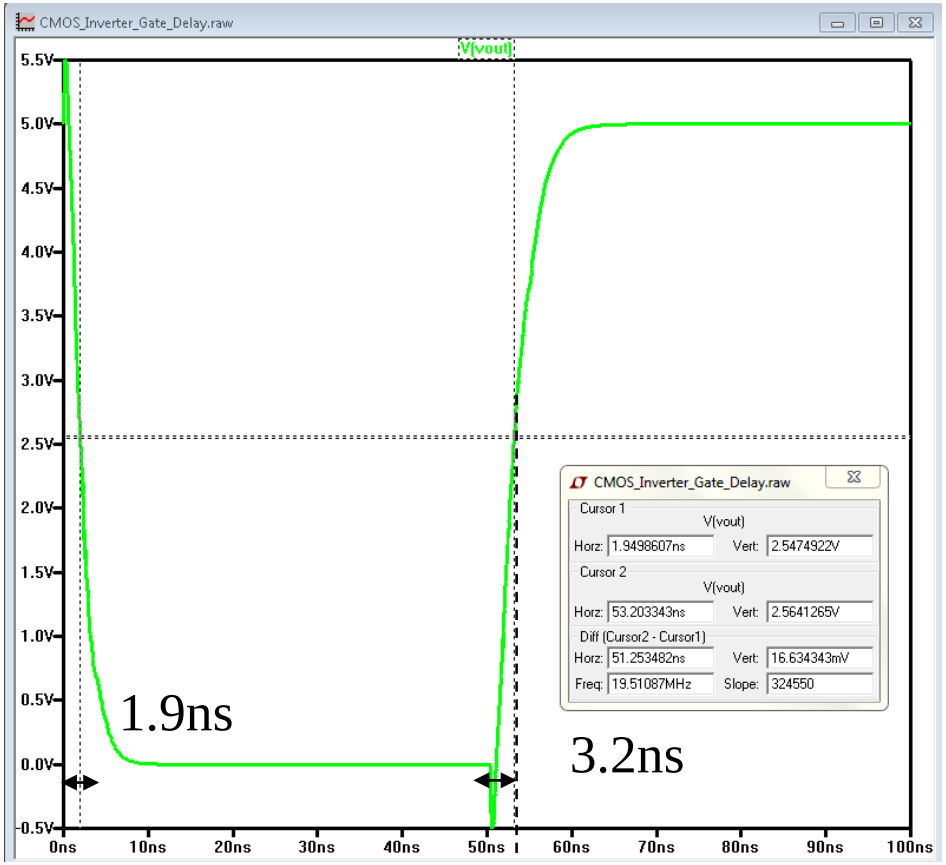
All PMOS L=10u W=360u Ad=18000p AS=18000p PD=820u PS=820u

.tran 0 100n 0 10p

PULSE(0 5 0 .37n .37n 50n 100n 2)

.include c:\SPICE\RIT_Models_For_LTSPICE.txt





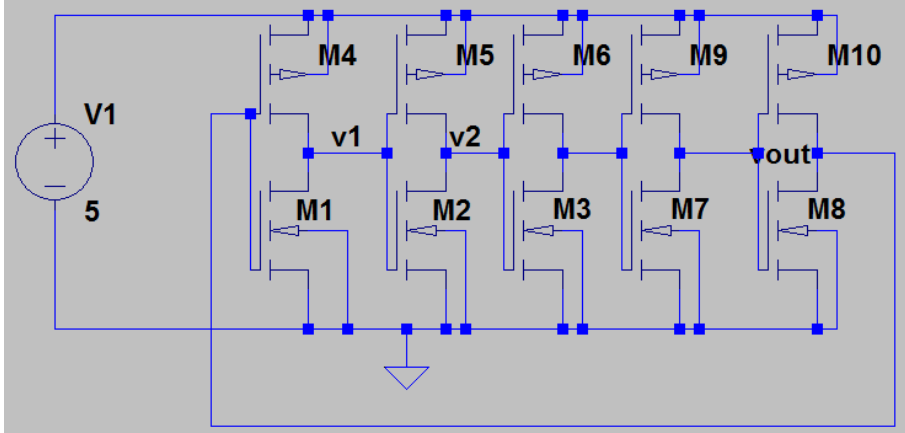
Using the RIT4007 spice models the gate delay td is found to be 2600ps.

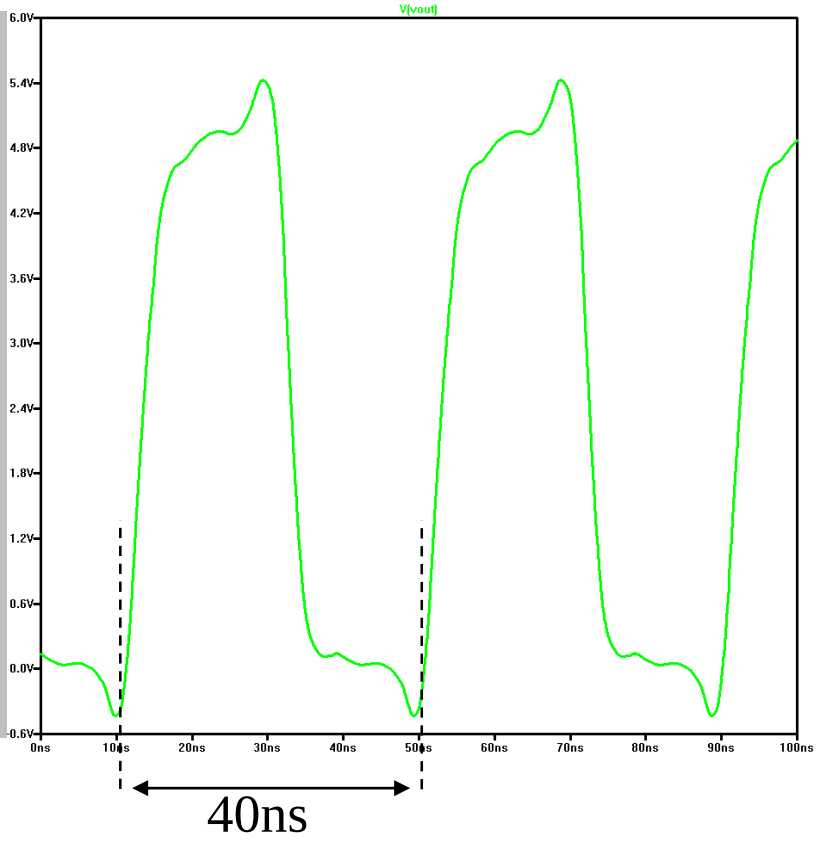
This uses very fast rise/fall time input voltage.

$$td = \tfrac{1}{2}(t_{HTL} + t_{LTH}) = 1/2\ (1.9n + 3.2n) = 2.6ns = 2600ps$$

FIVE STAGE RING OSCILLATOR SPICE SIMULATIONS

All PMOS L=10u W=360u Ad=18000p As=18000p Pd=820u Ps=820u
All NMOS L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=440u
PMOS SPICE MODEL = RIT4007P7
NMOS SPICE MODEL = RIT4007N7
.tran 0 200ns 100n .01ns
.include c:\SPICE\RIT_Models_For_LTSPICE.txt



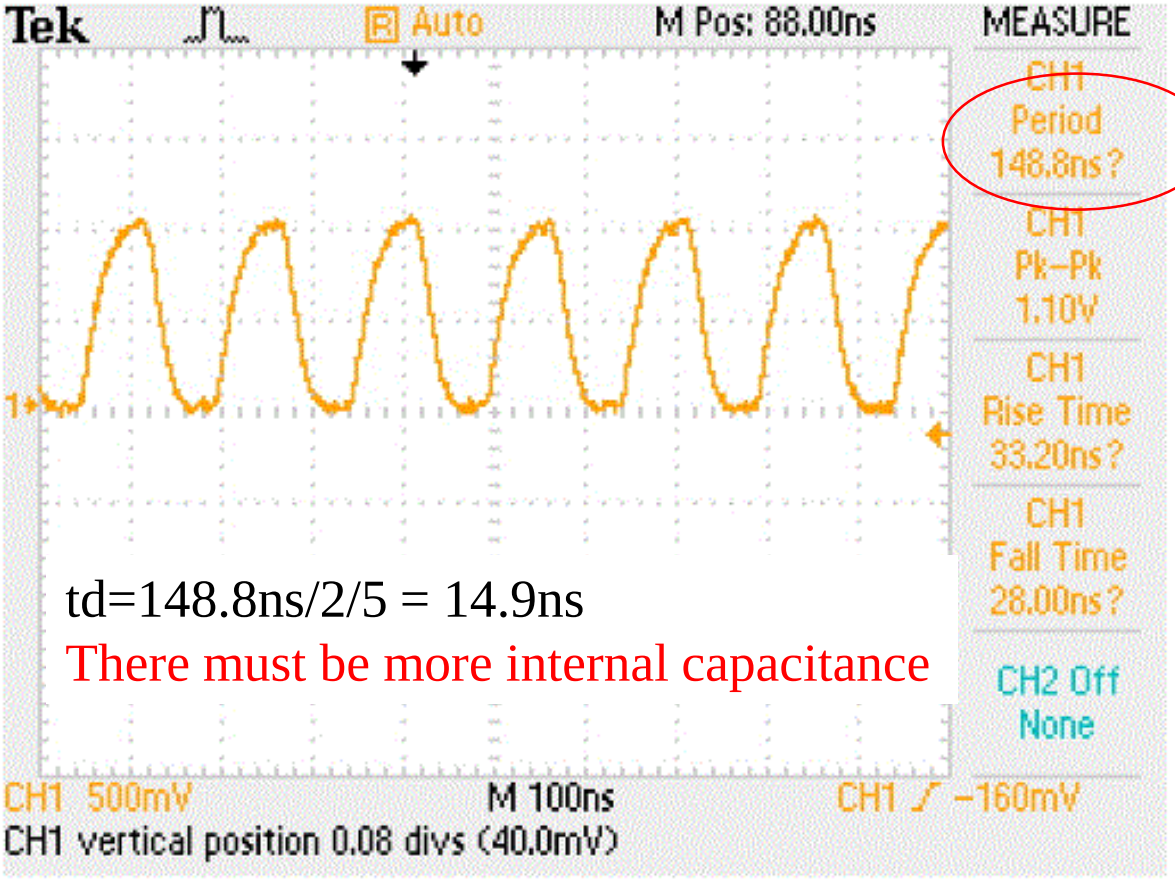


Using the RIT4007 spice models the gate delay td is found to be 4000ps

Input to each gate has slow rise/fall times and as a result is slower than td from the previous page

td=40ns/2/5 = 4ns = 4000ps

FIVE STAGE RING OSCILLATOR MEASUREMENTS



Plot 7. Vdd = 10V

CD4007 DATASHEET

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS018C – Revised September 2003

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

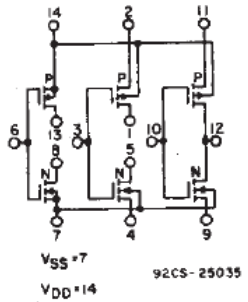
■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL}, t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative **Standard No. 13B, "Standard Specifications** for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

FUNCTIONAL DIAGRAM

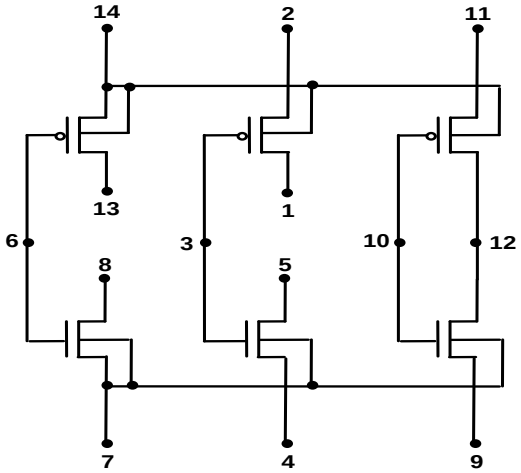
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

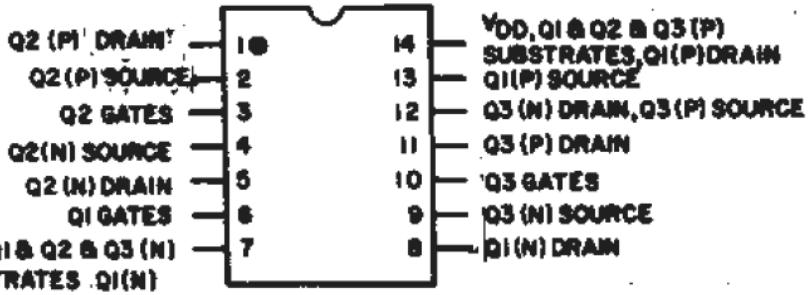
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

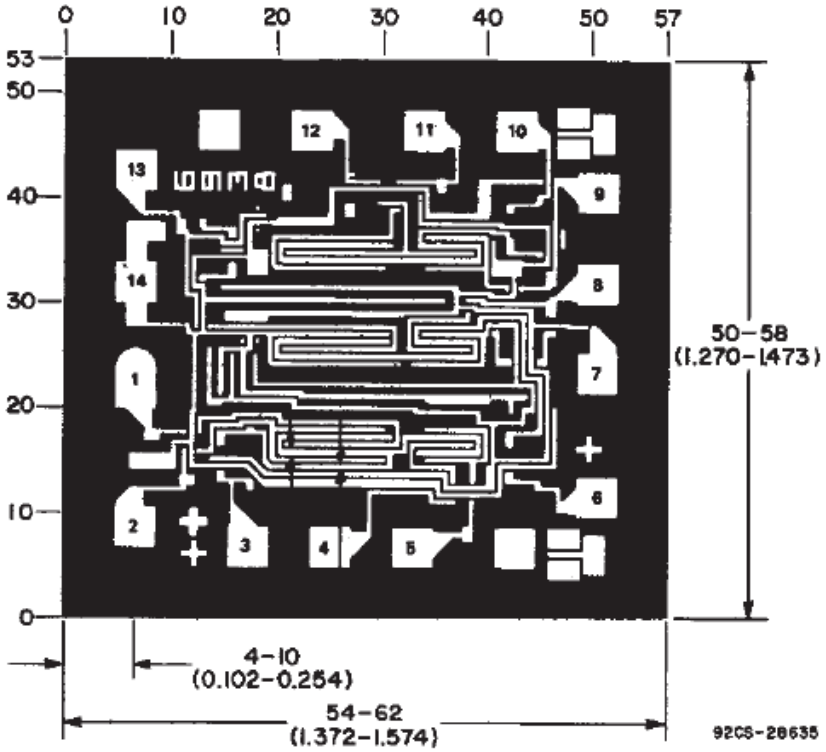
FROM THE CD4007 DATASHEET

Pin 14 goes to the n-type substrate of the PMOS devices and must go to most positive voltage. Pin 7 to the most negative.



TERMINAL DIAGRAM
Top View





DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in mils or 0.001 inch, in parentheses are dimensions in mm.
Note: PMOS are wider than NMOS

TRANSIENT DEVICE CHARACTERISTICS

The SPICE model for transient circuit analysis such as oscillator operation, gate delay investigations or other circuit timing require size information such AD, AS, PD, PS in addition to L and W.

Furthermore this package includes electrostatic protection devices on each gate pin which adds resistors and junction capacitance connected to the gate.

The SPICE models shown work well for DC analysis such as Voltage Transfer Curves (VTC). For Transient analysis the results are less accurate because of inaccurate knowledge of the ESD circuitry sizes and values. Adding a series resistors and capacitor to the circuit (in SPICE) to model the ESD circuitry is possible.

We can determine the total internal capacitance for each inverter experimentally.

OTHER COMPONENTS INSIDE THE CD4007 CHIP

This figure show the parasitic diodes in the CD4007 chip. Each diode represents a capacitance that should be included when doing SPICE transient analysis. The resistors along with the reverse biased diodes provide electrostatic discharge protection (ESD).

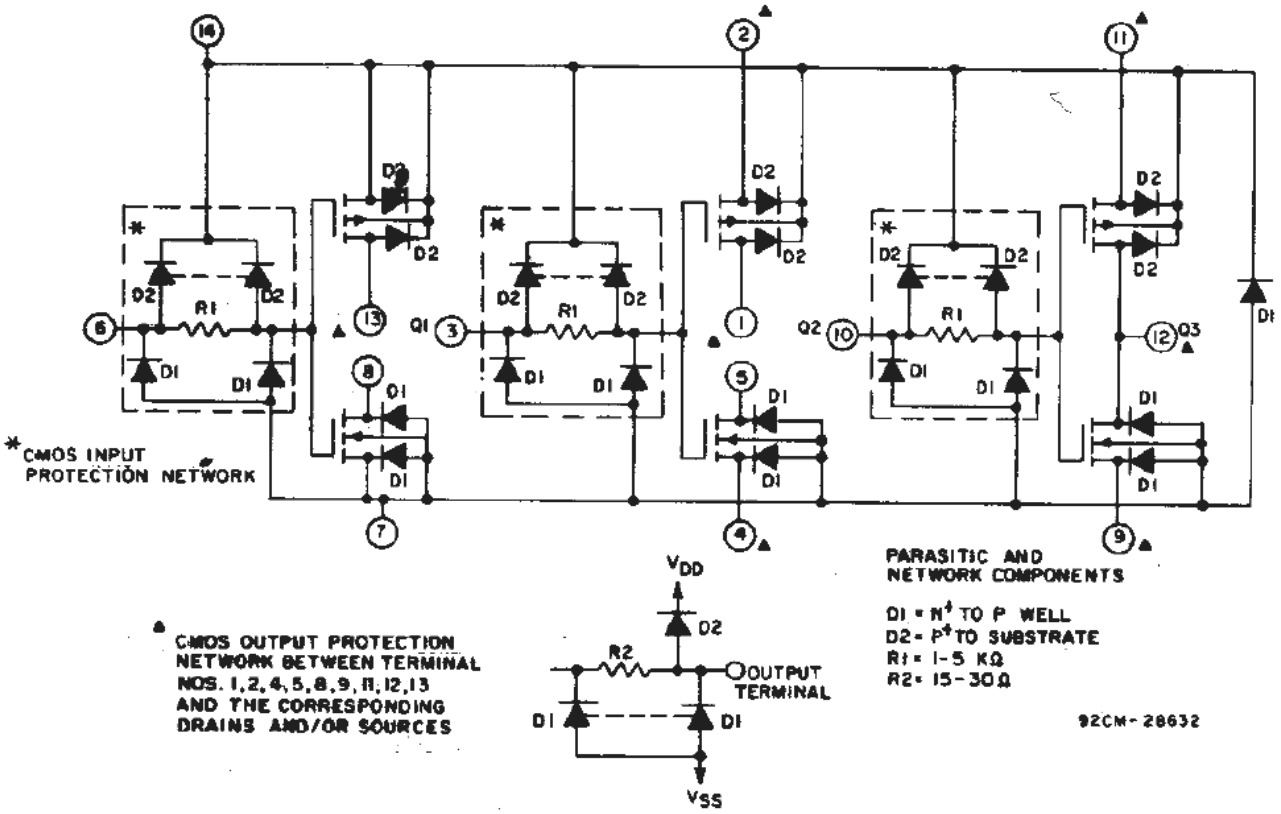


Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

TOTAL INTERNAL CAPACITANCE

We can experimentally determine the total internal capacitance for each inverter by measuring the gate delay with and without additional capacitance added to each inverter in the ring oscillator.

Gate Delay is proportional to C internal

With no external capacitors added

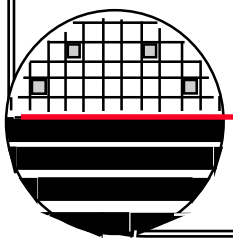
$t_{d1} \alpha C_{int}$ Eq. 1

With external capacitor added to each stage

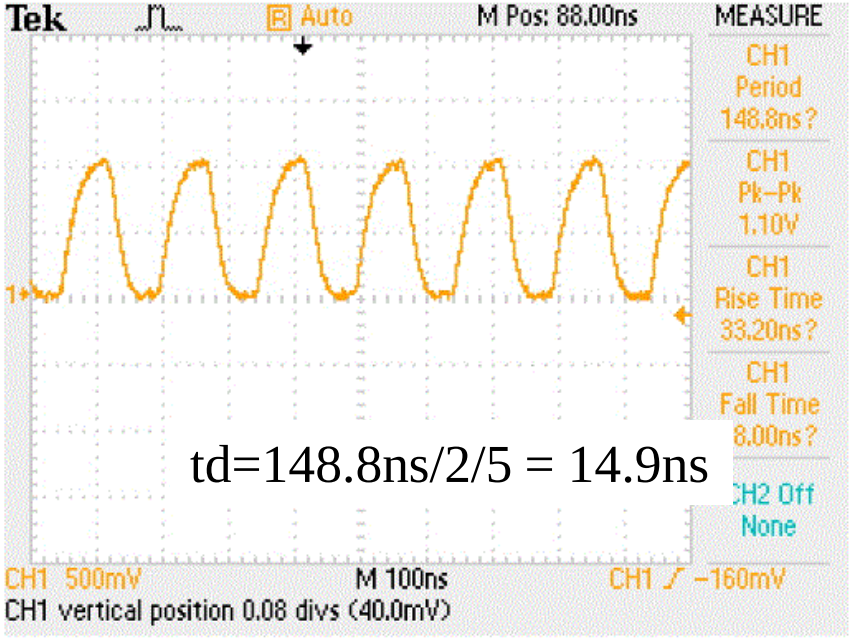
$t_{d2} \alpha C_{int} + C_{external}$ Eq. 2

Divide Eq 1 by Eq 2 solve for Cint

$t_{d1}/t_{d2} = C_{int}/(C_{int} + C_{ext})$

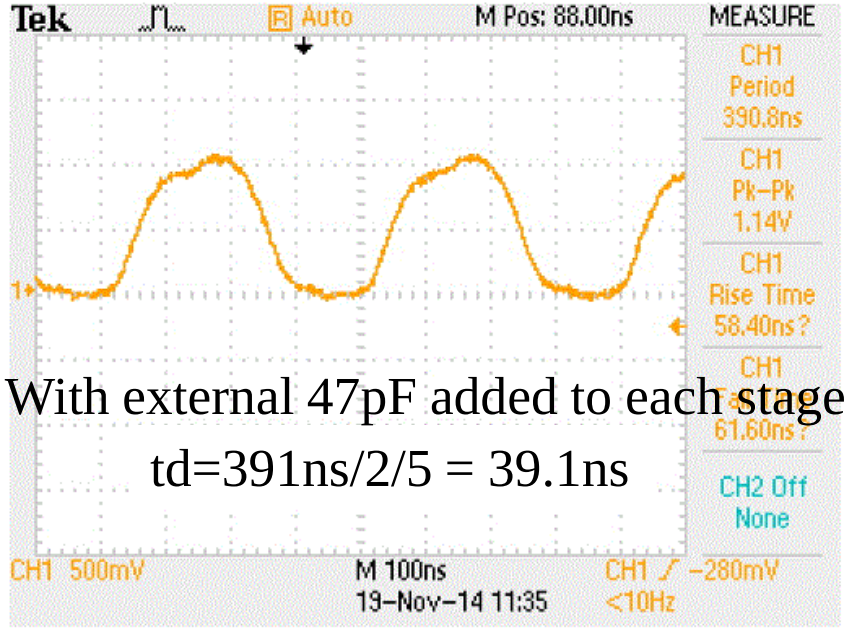


FIVE STAGE RING OSCILLATOR MEASUREMENTS



td=148.8ns/2/5 = 14.9ns

Plot 7. Vdd = 10V



With external 47pF added to each stage

td=391ns/2/5 = 39.1ns

Plot 8. Vdd = 10V, 47pf Capacitance

Measurement Example: 14.9ns/39.1ns = Cint/(Cint+47pF)

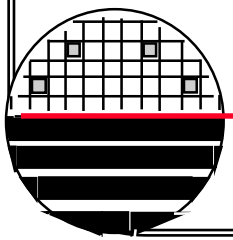
Cint = 11pF this includes inverter internal cap plus ESD, pads, probe

SUMMARY

Proper analysis of timing issues in logic requires proper SPICE models and knowledge of the transistor dimensions. Additional capacitances such as ESD protection circuitry, scope probe capacitance and resistances also influence the overall speed of operation.

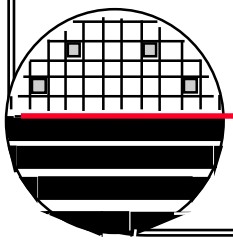
Hand Calculation	td = 3200ps
SPICE Step Response	td = 2600ps
Ring Oscillator	td = 4000ps
Measured	td = 14900ps

Measured total internal capacitance 11pF



REFERENCES

1. Sedra and Smith, 5.1-5.4
2. Device Electronics for Integrated Circuits, 2nd Edition, Kamins and Muller, John Wiley and Sons, 1986.
3. The Bipolar Junction Transistor, 2nd Edition, Gerald Neudeck, Addison-Wesley, 1989.



CD4007 SPICE MODEL

```
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=170u Ad=8500p As=8500p Pd=440u Ps=440u NRD=0.1 NRS=0.1
.MODEL RIT4007N7 NMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=4E-8 XJ=2.9E-7 NCH=4E15 NSUB=5.33E15 XT=8.66E-8
+VTH0=1.4 U0= 1300 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=300 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-8 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*Used in Electronics II for CD4007 inverter chip
*Note: Properties L=10u W=360u Ad=18000p As=18000p Pd=820u Ps=820u NRS=O.54 NRD=0.54
.MODEL RIT4007P7 PMOS (LEVEL=7
+VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=5E-8 XJ=2.26E-7 NCH=1E15 NSUB=8E14 XT=8.66E-8
+VTH0=-1.65 U0= 400 WINT=1.0E-6 LINT=1E-6
+NGATE=5E20 RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-8 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 PCLM=5
+CGSO=4.5E-10 CGDO=4.5E-10 CGBO=5.75E-10)
*--------------------------------------------------------------------
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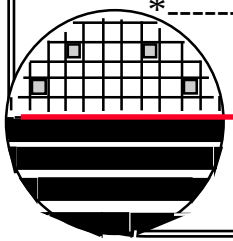
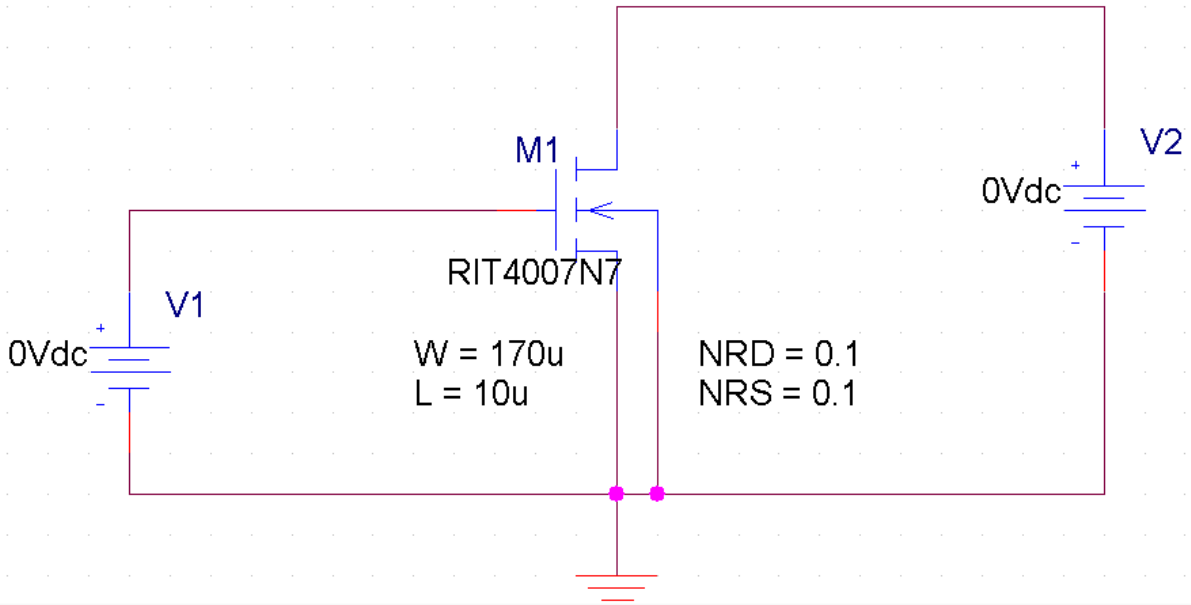


SPICE SCHEMATIC

PSPICE Circuit Schematic for Id-Vds Family of Curves
Note: Specification of Model RIT4007N7, L, W, NRD, NRS

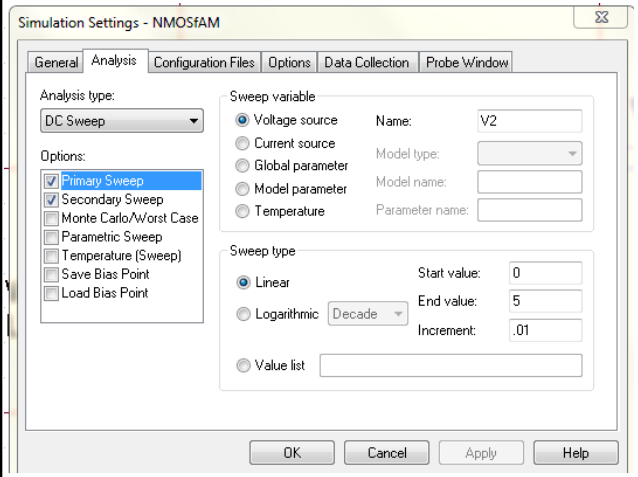


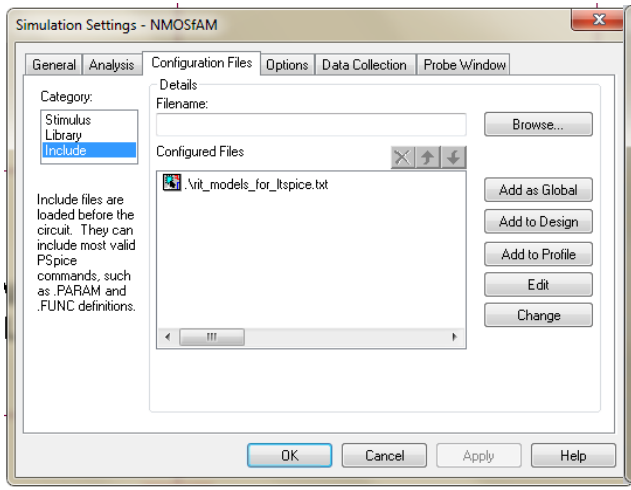
New Property... | Apply | Display... | Delete Proper

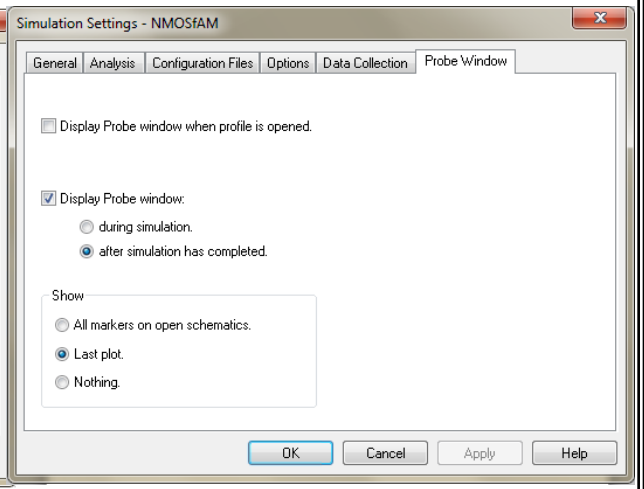
	A
	SCHEMATIC1 : PAGE1
Color	Default
Designator	
Graphic	MbreakN.Normal
ID	
Implementation	RIT4007N7
Implementation Path	
Implementation Type	PSpice Model
L	10u
Location X-Coordinate	460
Location Y-Coordinate	200
M	
Name	INS30
NRB	
NRD	0.1
NRG	
NRS	0.1
Part Reference	M1
PCB Footprint	
PD	
Power Pins Visible	
Primitive	DEFAULT
PS	
PSpiceOnly	TRUE
PSpiceTemplate	M^Y@REFDES %d %g %s %
Reference	M1
Source Library	C:\CADENCE\SPB_16.
Source Package	MbreakN
Source Part	MbreakN.Normal
Value	MbreakN
W	170u

SPICE SET UP

PSPICE Simulation Profile



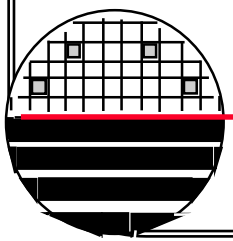




DC Sweep
V2 from 0 to 5 in 0.01 Volt steps
V1 from 0 to 5 in 0.5 Volt steps

Include text file with
SPICE model RIT4007N7

Set up plot to plot Id
Use same setup as Last plot
each time SPICE is run



SIMULATED I-V FAMILY OF CURVES

Overlay of PSPICE Simulated Id-Vds Curves and Measured Id-Vds Curves
Measured Curves made with Digilent Analog Discovery Module