Cancel PWM DAC ripple with analog subtraction

Stephen Woodward - November 28, 2017

Every PWM DAC design needs analog filtering to separate the desired PWM duty-cycle-proportional DC component from unwanted AC ripple. The simplest of these is the basic RC low-pass filter, which gives a peak-to-peak ripple amplitude (for the worst case of 50% PWM duty cycle, where T_{PWM} = PWM cycle time, and assuming RC > T_{PWM}) of:

$$V_{ripple} / V_{fullscale} = T_{PWM} / 4{\cdot}RC$$

The obvious design tradeoff is that while any desired degree of ripple attenuation can be achieved by choosing a large enough RC product, settling time will correspondingly suffer. For example, if we (fairly logically) choose a definition for the settling band as equal to ripple amplitude, then…

$$T_{settle} = RC{\cdot}ln(V_{fullscale} / V_{ripple})$$

$$= T_{PWM}{\cdot}V_{fullscale}{\cdot}ln(V_{fullscale} / V_{ripple}) / (4{\cdot}V_{ripple})$$

The consequences of this relationship can be illustrated by the 8-bit case:

$$Given: V_{ripple} / V_{fullscale} = 1/256;\ RC = 64{\cdot}T_{PWM}$$

$$T_{settle} = 64{\cdot}ln(256){\cdot}T_{PWM} = 355{\cdot}T_{PWM}$$

which, even for a fairly speedy 32 kHz (31µs T_{PWM}), predicts a positively *glacial* 11ms settling time.

Clearly, if settling time is a critical design parameter, we'll need to do better and find a less simplistic filtering scheme. The extreme possibilities that lie in this direction are illustrated by my previous DI, Fast-settling synchronous-PWM-DAC filter has almost no ripple.

But not every application that can't tolerate molasses-in-January $355{\cdot}T_{PWM}$ settling times need or can justify such a complex filtering solution. The **Design Idea** presented here addresses these middle-o--the-road applications. As shown in **Figure 1**, it augments the basic R1/C1 low-pass with an inverter, R2, and C2, which combine to negate and subtract (most of) the undesired AC component from the wanted DC signal, leaving a relatively clean analog output with settling time much less than a simple RC filter.

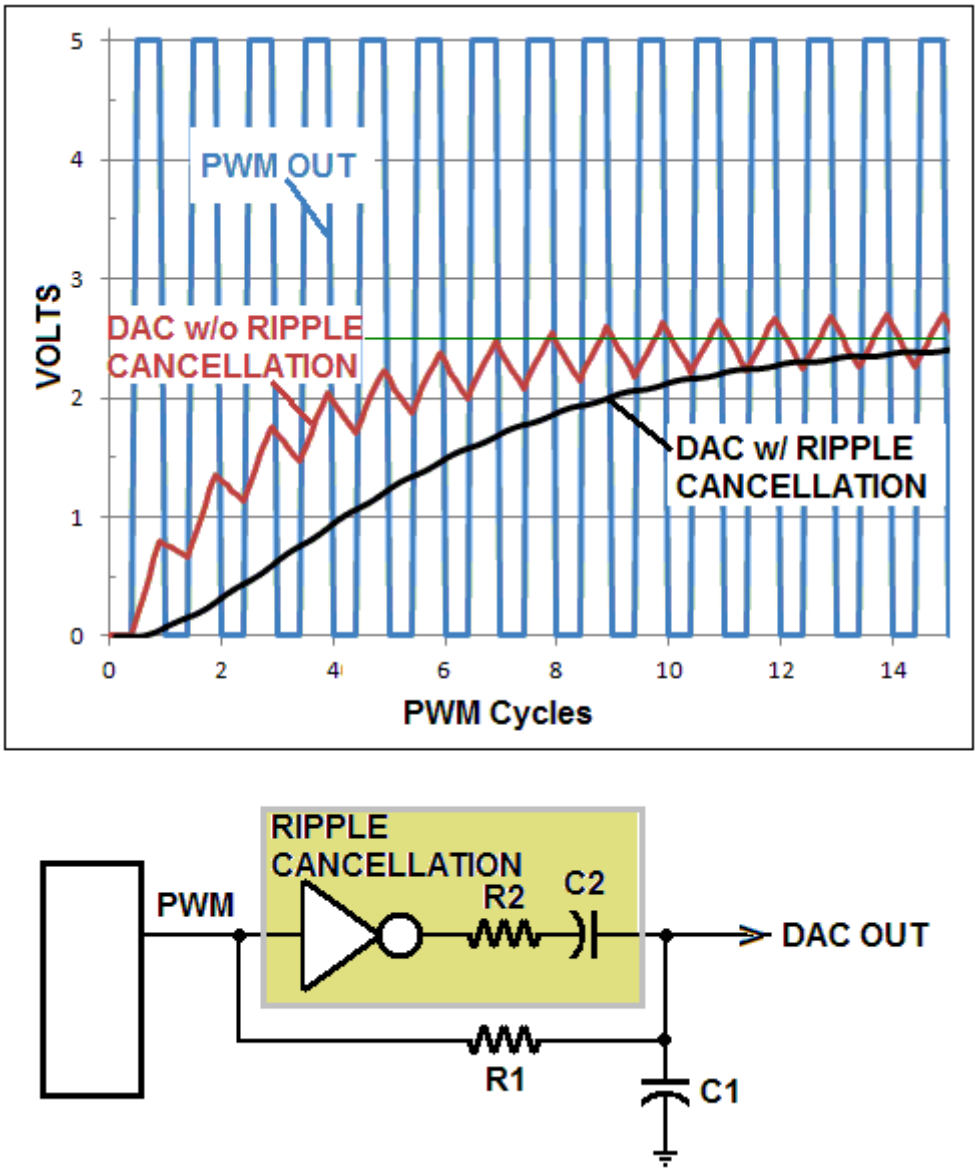

Figure 1 Waveforms & schematic of PWM DAC ripple canceller

But how pure is “relatively clean”, and how fast is “much less”? Setting R2=R1 and C2=C1, the ripple and settling time figures for the new circuit are:

$$V_{ripple} / V_{fullscale} = (T_{PWM} / 4 \cdot RC)^2$$

$$T_{settle} = T_{PWM} \cdot ln(V_{fullscale} / V_{ripple}) \cdot (V_{fullscale} / 16 \cdot V_{ripple})^{1/2}$$

Referring again to the 8-bit case (illustrated graphically in Figure 1):

Given: $RC = 4 \cdot T_{PWM}$

$T_{settle} = 22 \cdot T_{PWM} =$ 0.69 ms

with a 32 kHz cycle, it’s 16 times faster, with a squared ripple-amplitude ratio!

For many applications, this represents a very worthwhile tradeoff between a modest increase in circuit complexity and a significant increase in PWM DAC performance.

—W. Stephen Woodward is one of EDN's most prolific and innovative Design Ideas authors, with dozens of contributions to his credit.

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