Chapter 4

Junction Field Effect Transistor Theory and Applications

4.0 Introduction

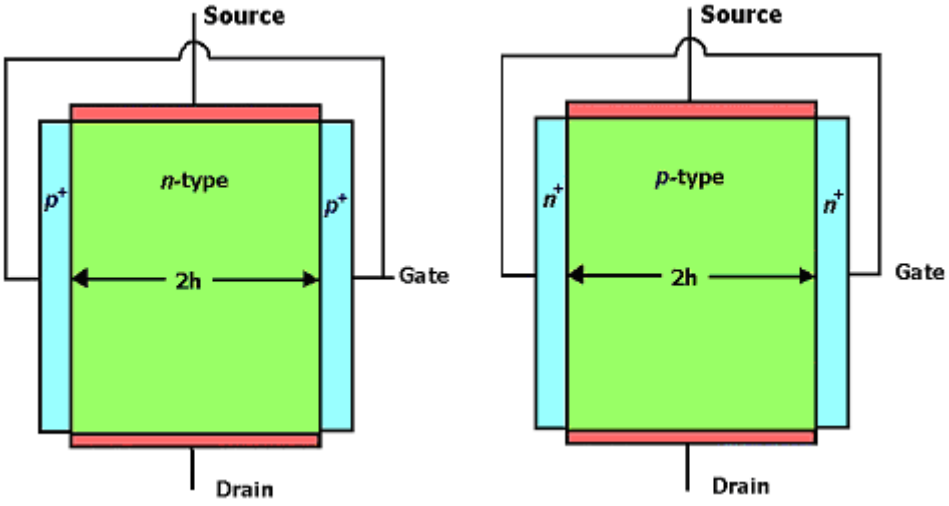
Like bipolar junction transistor, junction field effect transistor JFET is also a three-terminal device but it is a unipolar device, which shall mean that the current is made of either electron or hole carrier.

The operation of JFET is controlled by electric field effect. Thus, JFET is a voltage-controlled current source device, whereas BJT is a current-controlled source device.

There are two types of JFET namely *n*-channel and *p*-channel. *n*-channel type means the carrier type in the conducting channel is electron. Likewise, for *p*-channel type, the carrier type in conducting channel is hole.

JFET has three terminals, which are gate G, drain D and source S. The gate is used to control the flow of carrier from source to drain. Source is the terminal that emits carrier and the drain is the terminal that receives carrier.

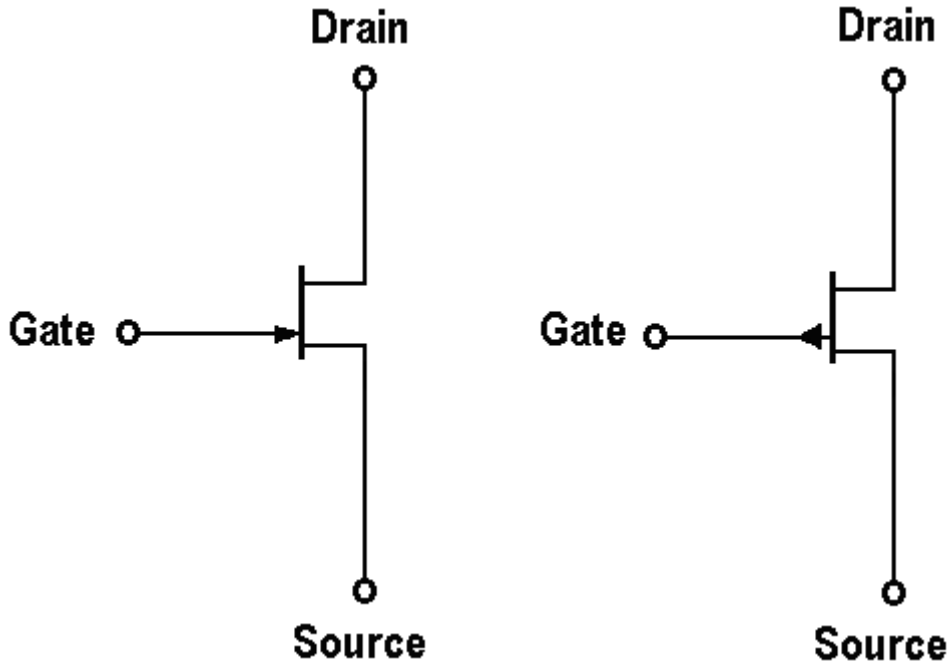
The structures of *n*-channel and *p*-channel JFET are shown in Fig. 4.1.



(a) *n*-channel JFET (b) *p*-channel JFET

Figure 4.1: The structures of *n*-channel and *p*-channel

The symbols of *n*-channel and *p*-channel JFETs are shown in Fig. 4.2.



(a) *n*-channel JFET (b) *p*-channel JFET

Figure 4.2: Symbols of *n*-channel and *p*-channel JFET

4.1 Biasing the JFET

In normal operation, the gate of JFET is always reverse-biased. Thus, an *n*-channel type, the gate is biased with negative voltage i.e. gate voltage is less than zero volt $V_G < 0$, whilst for *p*-channel type, the gate is biased with positive voltage i.e. gate voltage is greater than zero voltage $V_G > 0$.

The source and drain are biased according to the channel type or carrier type. If it is an *n*-channel JFET (electron as carrier), the source is biased with negative voltage while the drain is biased with positive voltage. Alternatively, it can be biased such that the drain voltage V_D is greater than the source voltage V_S. i.e. $V_D > V_S$.

If it is a *p*-channel JFET (hole as carrier), the source is biased with positive voltage while the drain is biased with negative voltage. Alternatively, it can be biased such that the drain voltage V_D is less than the source voltage V_S. i.e. $V_D < V_S$.

Figure 4.3 shows the bias condition for an *n*-channel JFET.

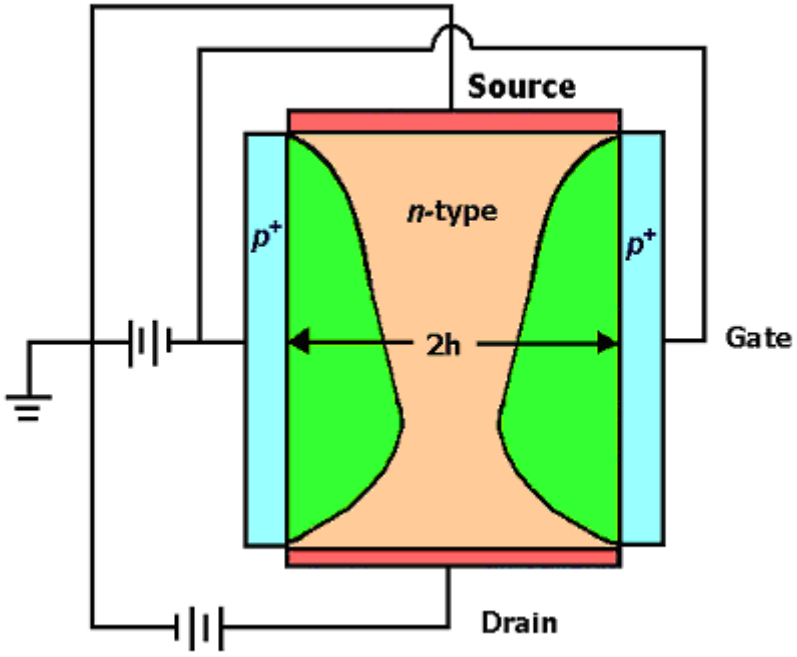


Figure 4.3: Bias connection for *n*-channel JFET

4.2 JFET Characteristics and Parameters

Figure 4.4 shows the drain current characteristics of a JFET for gate-to-source voltage equal to 0V. i.e. $V_{GS} = 0$.

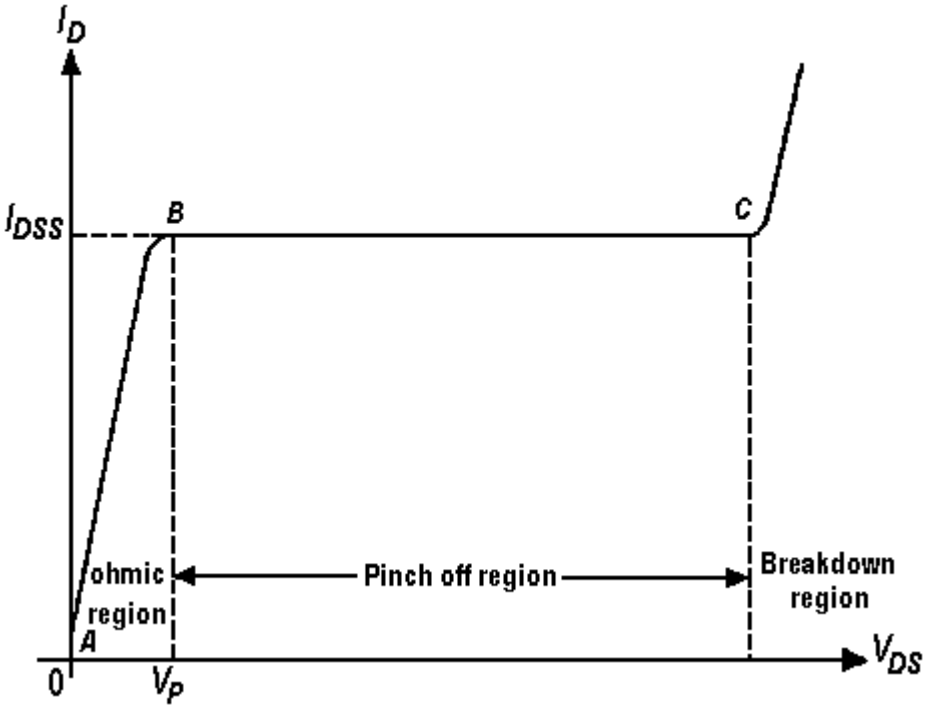


Figure 4.4: JFET drain characteristics curve for $V_{GS} = 0$

Between point A and B, it is the ohmic region of the JFET. It is the region where the voltage and current relationship follows ohm's law. At point B, the drain current is at maximum for $V_{GS} = 0$ condition and is defined as I_{DSS}. It is the pinch-off point, where there is no increase of current as drain-to-source voltage V_{DS} is further increased. The V_{DS} voltage at this point is called *pinch-off voltage* V_P. It is also the voltage point where drain-to-gate voltage V_{DG} produces enough depletion thickness to narrow the channel so that the resistance of the channel will increase significantly. Since $V_{GS} = 0$, V_{DS} is also equal to V_{DG}. Thus, in general the pinch-off voltage V_p is

$$V_p = V_{DS(P)} - V_{GS} \qquad (4.1)$$

where $V_{DS(P)}$ is the pinch-off drain-to-source voltage for a V_{GS} value. I_{DSS} and V_P are constant values listed by the manufacturer for a given JFET type, which are the drain current and pinch-off voltage at gate-to-source voltage $V_{GS} = 0$.

At point C, the JFET begins to breakdown where the I_D increases rapidly and it is an irreversible breakdown.

Different value of V_{GS} produces different drain characteristic curve. For *n*-channel JFET, as V_{GS} decreases, I_D current and $V_{DS(P)}$ decreases. There is a V_{GS} value that no drain current I_D is registered irrespective of the drain-source voltage V_{DS}. This gate-to-source voltage V_{GS} is the cutoff gate-to-source voltage $V_{GS(off)}$. Since there is no I_D current, V_{DS} must be zero. Thus, from equation (4.1) $V_{GS} = -V_P$. Equation (4.1) can also now be written as $V_{DS(P)} = V_{GS} - V_{GS(off)}$.

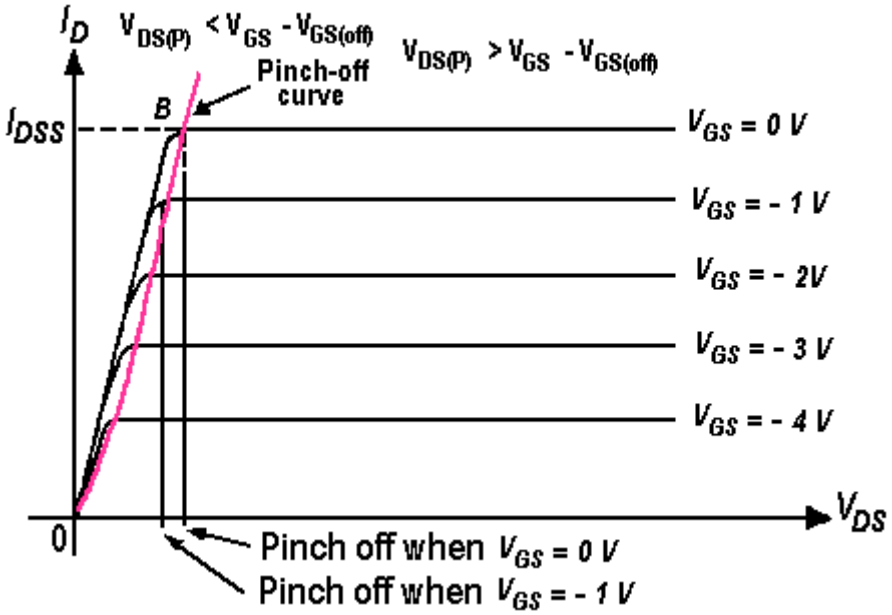


Figure 4.5: Drain characteristics of *n*-channel JFET of different V_{GS}

At ohmic region of the drain characteristic curve for *n*-channel type follows equation (4.2a), which is

$$I_D = AqN_D\mu_n E_X = 2bqN_D\mu_n\left(\frac{W}{L}\right)V_{DS} \qquad (4.2a)$$

where A is the effective cross sectional area of the channel for a given V_{GS} voltage and b is the effective channel width for a given gate-to-source voltage and zero drain current. At gate-to-source voltage equals to zero volt i.e. $V_{GS} = 0$ volt, the effective channel width b is equal to h. Thus, the *channel on-resistance* is defined as $r_{DS(on)} = \frac{1}{2hqN_D\mu_n}\cdot\frac{L}{W}$.

The pinch-off curve follows equation (4.2b), which is

$$I_D = I_{DSS}\left(1-\frac{V_{DS(P)}}{V_P}\right)^2 \qquad (4.2b)$$

Figure 4.6 shows the set-up for obtaining cut-off condition whereby the drain current I_D is equal to zero.

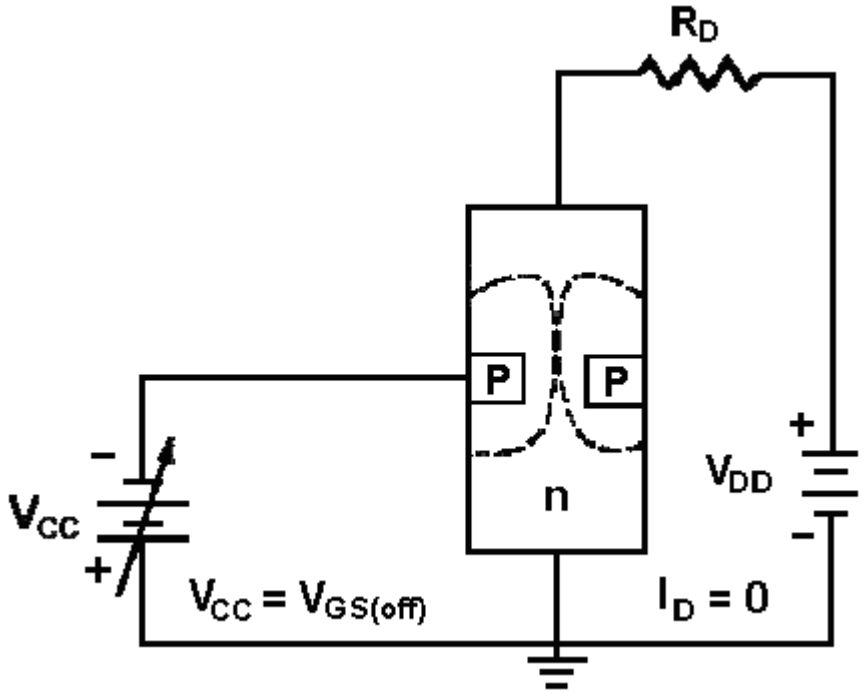
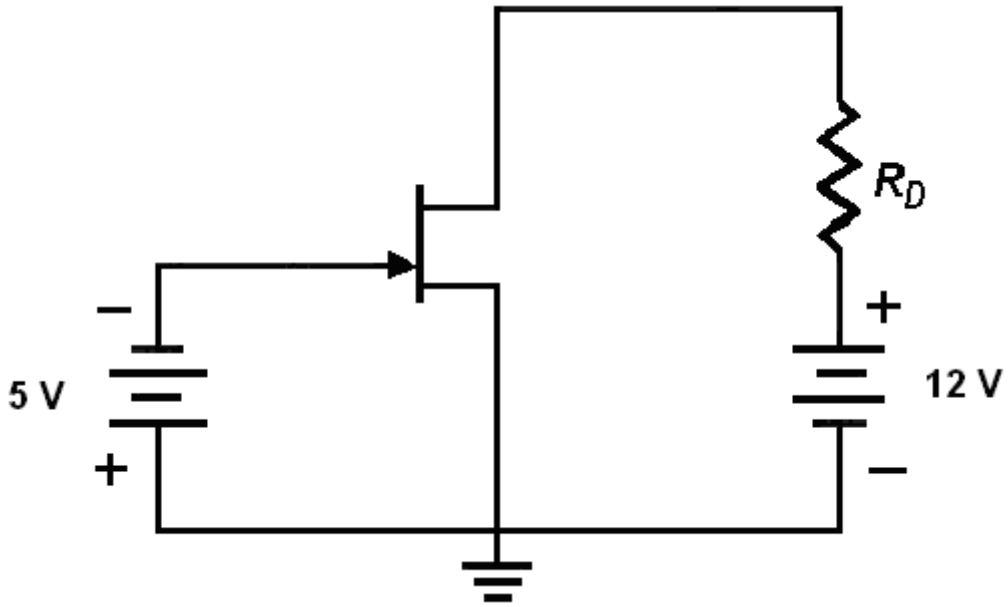


Figure 4.6: Condition for cutoff of an *n*-channel JFET

Example 4.1

For the JFET circuit shown in the figure, V_P = 8.0V and I_{DSS} = 12.0mA. (a) Determine the value of V_{DS} when pinch-off begins. (b) If the gate is grounded, what is the value of I_D for V_{DD} = 12.0V when V_{DS} is above pinch-off?



Solution

From the circuit, V_{GS} = -5V and apply equation (4.1),

$$\begin{aligned} V_{DS(P)} &= V_P + V_{GS} \\ &= 8V + (-5V) \\ &= 3V \end{aligned}$$

The V_{DS} voltage when pinch-off occurred is 3.0 V.

When the gate is grounded, V_{GS} = 0V, the drain current I_D is equal to I_{DSS} = 12mA. For any value of drain-to-source voltage V_{DS} above pinch-off voltage of 8V, the drain current I_D remains as I_{DSS} = 12.0mA. This is true as long as the drain-to-source voltage V_{DS} is below breakdown voltage.

4.2.1 Transfer Characteristics

The transfer characteristic of an *n*-channel JFET is shown in Fig. 4.7. At gate-to-source voltage V_{GS} = 0, the drain current I_D is equal to I_{DSS} and at gate-to-source voltage $V_{GS(off)}$, drain current I_D = 0.

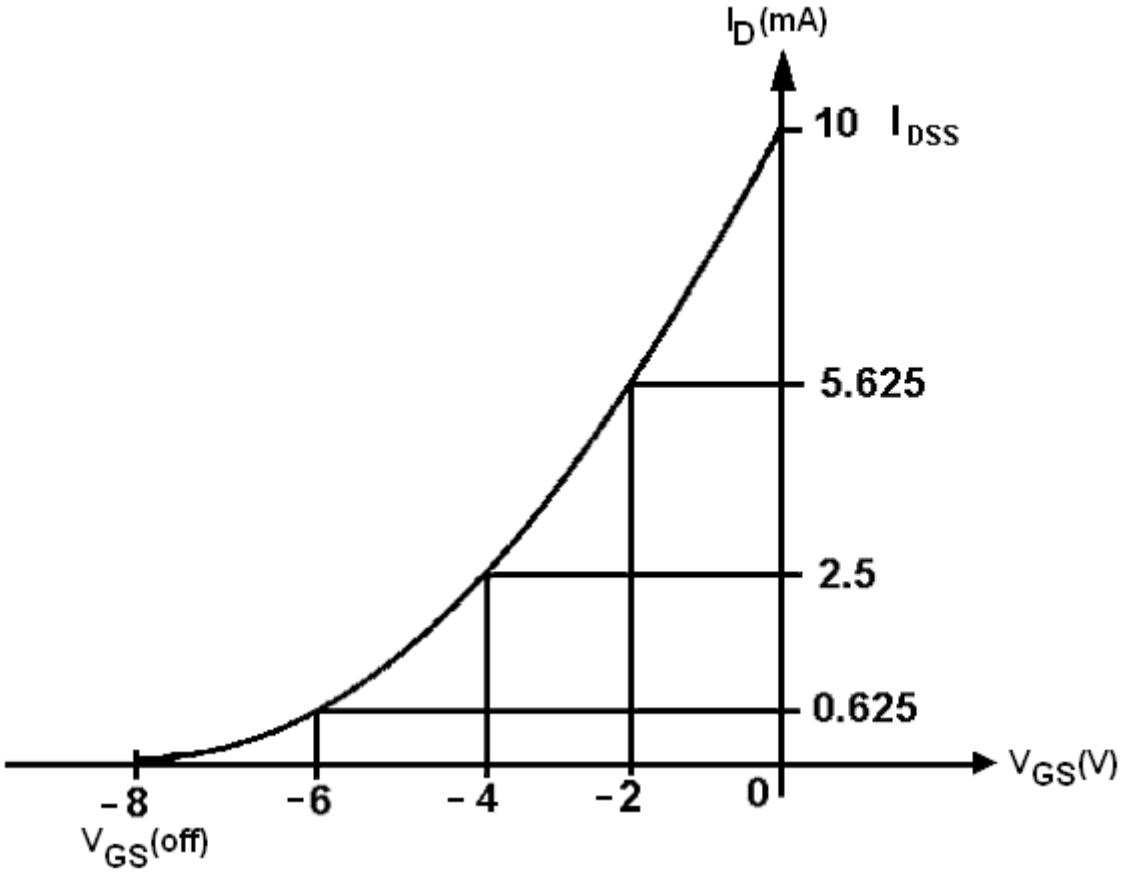


Figure 4.7: Transfer characteristics curve of an *n*-channel JFET

The curve is a parabolic curve, which can be expressed mathematically as

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \qquad (4.3)$$

4.2.2 Forward Transconductance

The forward transconductance g_m of the JFET is defined as the change of drain current for a given change in gate-source voltage V_{GS} and it is expressed as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (4.4)$$

From the transfer characteristic curve, one will realize that the transconductance of the device is at maximum when V_{GS} is at zero voltage. The value of g_m at V_{GS} = 0 is always given in the manufacturer data sheet of the device, which is denoted as g_{m0}. If g_{m0} is given, g_m for a given V_{GS} can be calculated from equation (4.5).

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \tag{4.5}$$

Equation (4.5) can be derived from equation (4.4) by differentiating drain current with respect to gate-to-source voltage i.e. dI_D/dV_{GS}.

$$g_m = \frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(Off)}}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \tag{4.6}$$

Comparing equation (4.5) and (4.6), g_{m0} shall be

$$g_{m0} = \left|-\frac{2I_{DSS}}{V_{GS(off)}}\right| \tag{4.7}$$

Thus, given the values of I_{DSS} and $V_{GS(off)}$, the transconductance of the device at $V_{GS} = 0$ can be determined.

From equation (4.3) and (4.5), transconductance g_m can be expressed as

$$g_m = g_{m0}\sqrt{I_D / I_{DSS}} \tag{4.8}$$

Thus, the transconductance g_m of JFET for a given drain current I_D value, can be obtained.

4.2.3 Input Impedance

Since the gate of JFET is reverse-biased, the input impedance is very high. This is one advantage of JFET over bipolar junction transistor. In JFET data sheet, the input impedance is given by gate reverse current I_{GSS} for a given gate-source voltage V_{GS}. Thus, input impedance can be expressed as

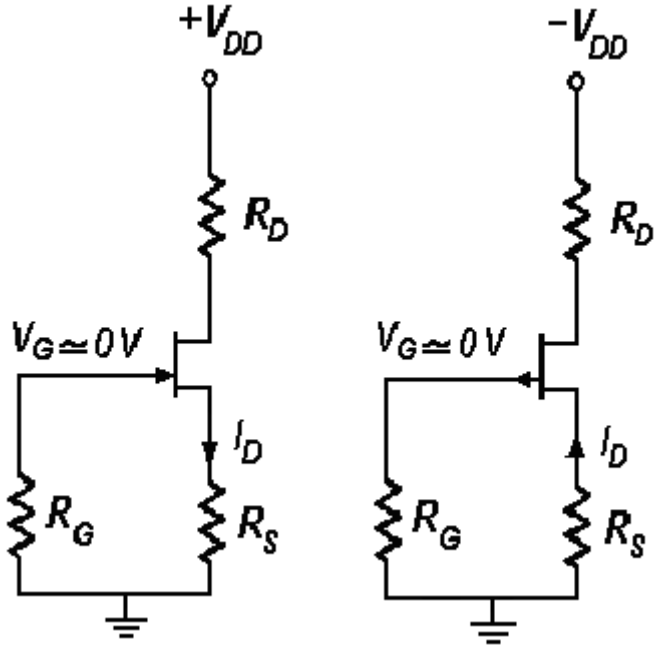
$$R_{IN(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right| \tag{4.9}$$

4.3 dc Biasing JFET

The purpose of biasing the device is to select the right dc gate-to-source voltage for the JFET in order to establish a desired value of drain current. Listed here are some standard methods.

4.3.1 Self-Biasing of JFET

The self-biasing circuits for *n*-channel and *p*-channel JFET are shown in Fig. 4.8. The gate of the JFET is connected to the ground via a gate resistor R_G.



(a) *n*-channel JFET (b) *p*-channel JFET

Figure 4.8: Self-biasing of JFET

The gate voltage V_G is closed to zero since the voltage dropped across R_G by I_{GSS} can be ignored. Thus,

$$V_{GS} = V_G - V_S \qquad (4.10)$$

From Fig. 4.8(a), $V_S = I_D R_S$ and $V_G = 0$

$$V_{GS} = 0V - I_D R_S$$

and

$$V_{GS} = + I_D R_S \text{ for } p\text{-channel JFET}$$

The drain-source voltage V_{DS} is

$$\begin{aligned} V_{DS} &= V_D - V_S \\ &= V_{DD} - I_D R_D - I_D R_S \\ &= V_{DD} - I_D(R_D + R_S) \end{aligned} \qquad (4.11)$$

As mentioned earlier, the purpose of biasing is to select the right dc gate-source voltage for the JFET to establish a desired value of drain current. Once it is established. The source resistance R_S can be calculated using equation (4.12).

$$R_S = \left|\frac{V_{GS}}{I_D}\right| \tag{4.12}$$

Example 4.2

Determine the value of R_S required to self-bias an *n*-channel JFET with I_{DSS} = 25mA, $V_{GS(off)}$ = -10V, V_{GS} = -5V and its transconductance g_m.

Solution

Drain current I_D at gate-to-source V_{GS} = -5V is

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2 = 25\text{mA}\left[1-\frac{-5\text{V}}{-10\text{V}}\right]^2 = 6.25\text{mA}$$

The source resistance R_S is

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \left|\frac{5\text{V}}{6.25\text{mA}}\right| = 800\Omega$$

Transconductance g_m at V_{GS} = 0, $g_{m0} = \left|-\frac{2I_{DSS}}{V_{GS(off)}}\right| = -\frac{2\text{x}25\text{mA}}{-10\text{V}} = 5\text{mA/V}$

Thus, the transconductance g_m at I_D = 6.25mA is,

$$g_m = g_{m0}\sqrt{I_D / I_{DSS}} = 5\text{mA/V}\sqrt{6.25\text{mA}/25\text{mA}} = 2.5\text{mA/V}$$

4.3.2 Mid-point Bias

The purpose of midpoint bias is to allow maximum drain current I_D swing. From the drain transfer characteristic curve, the midpoint bias occurred at drain current I_D corresponds to $I_{DSS}/2$ and at approximately gate-to-source voltage V_{GS} equals to $V_{GS(off)}/4$. Indeed when drain current equals to $I_D = I_{DSS}/2$, gate-to-source voltage is V_{GS} = 0.29 time of gate-to-source cutoff voltage $V_{GS(off)}$. The illustration is shown in Fig. 4.9.

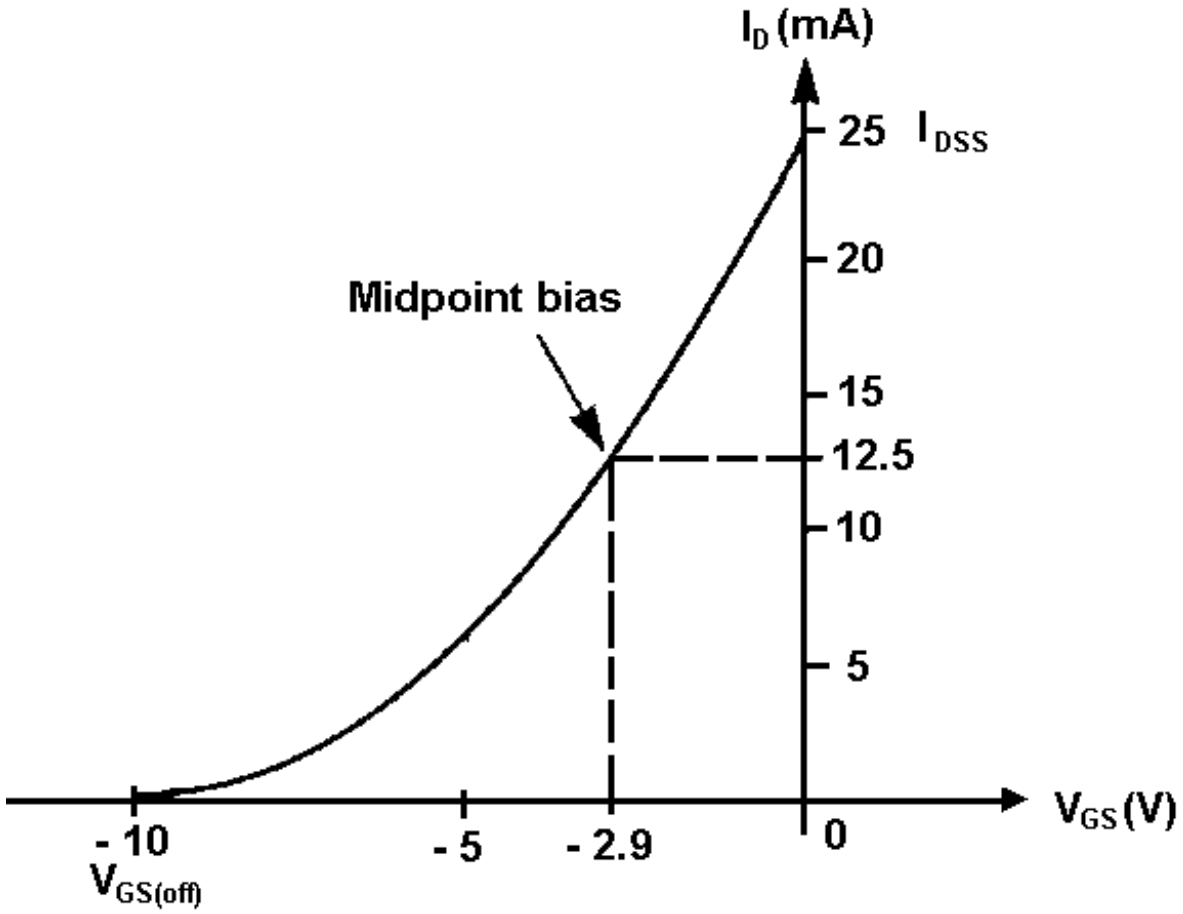


Figure 4.9: The transfer characteristic curve showing midpoint-bias values for JFET

4.3.3 Voltage Divider Bias

An *n*-channel JFET with voltage-divider bias is shown in Fig. 4.10. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

The source voltage V_S is

$$V_S = I_D R_S \tag{4.13}$$

The gate voltage V_G is set by resistors R_1 and R_2 and is expressed by the following equation using voltage-divider concept.

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} \tag{4.14}$$

The gate-to-source voltage V_{GS} is $V_{GS} = V_G - V_S$

Thus,

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} - I_D R_S \tag{4.15}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{4.16}$$

and

$$I_D = \frac{V_G - V_{GS}}{R_S} \tag{4.17}$$

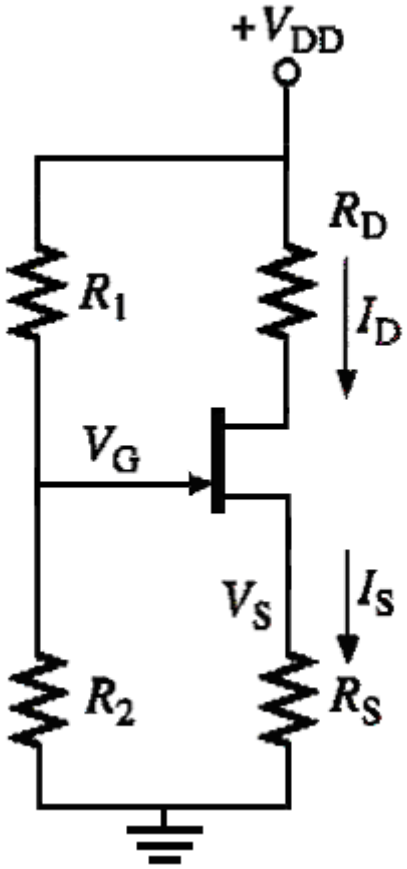
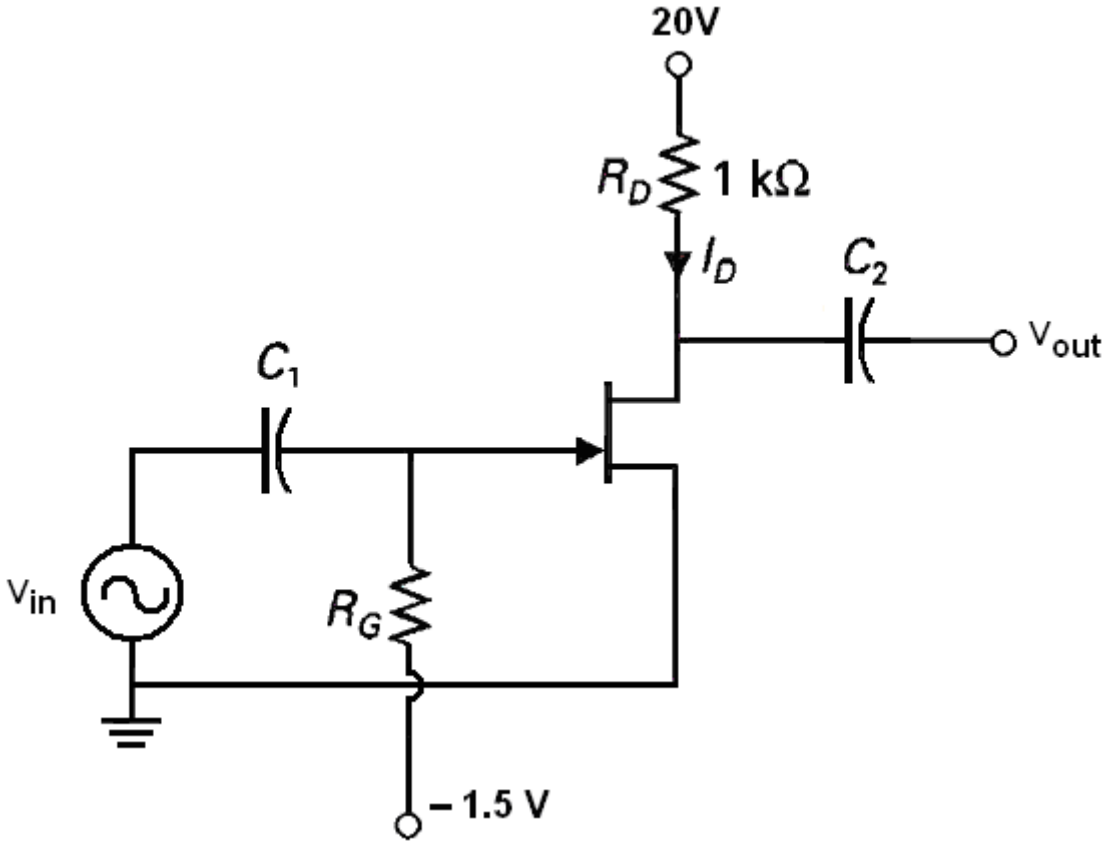


Figure 4.10: An *n*-channel JFET voltage-divider bias circuit

Example 4. 3

Determine the dc Q-point of the amplifier shown in figure and draw its dc load line. Given the I_{DSS} and $V_{GS(off)}$ of JFET are 20mA and - 4.0V respectively.



Solution

Since $R_{IN(gate)}$ is extremely large, it does not cause any significant effect to gate resistor R_G.

Using equation (4.3)

$$I_D = 20\text{mA}\left(1 - \frac{-1.5\text{V}}{-4\text{V}}\right)^2 = 7.8\text{mA}$$

Voltage drop across drain-source

$$V_{DS} = V_{DD} - I_D \text{ x } 1\text{k}\Omega = 20\text{V} - 1\text{k}\Omega \text{ x } 7.8\text{mA}$$
$$= 12.2\text{V}$$

Maximum $I_D = I_{DSS} = 20\text{mA}$ and V_{DS} at cutoff, $V_{DS(cutoff)} = 20\text{V}$.

From the results above, the Q (quiescent)-point and dc load line are drawn and shown in Fig. 4.11.

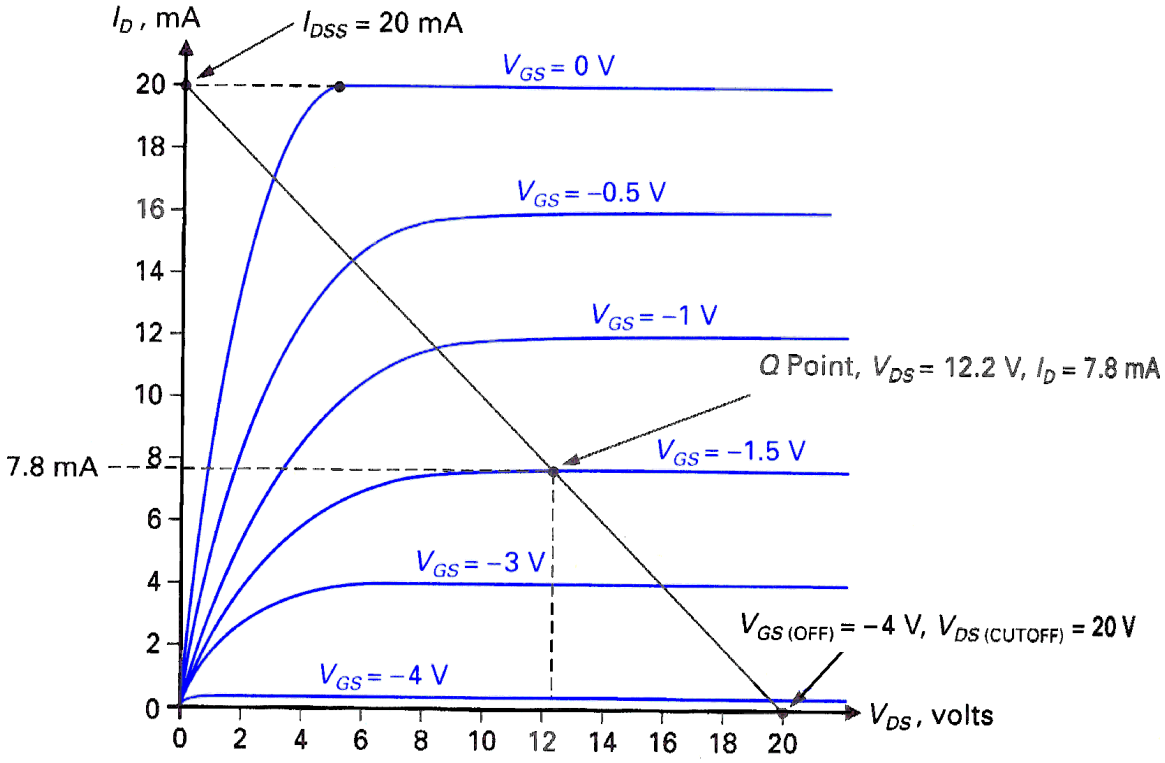


Figure 4.11: The graph shows the dc load line and Q-point of the amplifier shown in Fig. 4.10

Example 4.4

Determine the approximate Q-point for the JFET biased with a voltage divider circuit as shown in the figure, given that the particular device has transfer characteristic curve as shown.

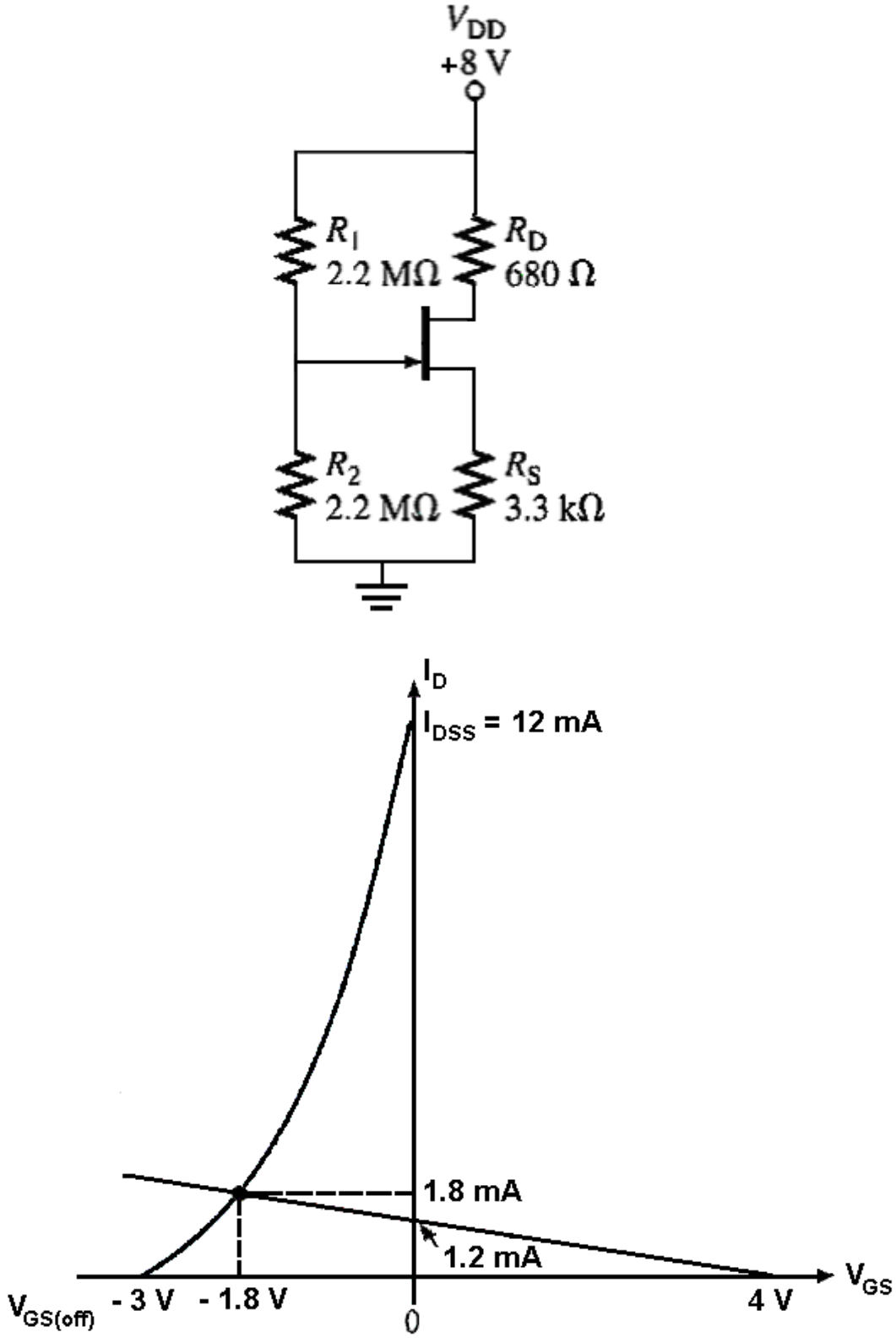
Solution

From equation (4.13), for drain current $I_D = 0A$, the gate-to-source voltage V_{GS} is

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{2.2M\Omega}{2.2M\Omega + 2.2M\Omega}\right)8V = 4.0V$$

From Equation (4.15), for $V_{GS} = 0V$, the drain current is

$$I_D = \frac{V_G}{R_S} = 4V/3.3k\Omega = 1.2mA$$



From graphic plot, I_D for Q-point is 1.8mA. Thus, from equation (4.14)

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$= 8V - 1.8mA(680\Omega + 3.3k\Omega)$
$= 0.83V$

4.4 Small Signal Amplifier

In this Section, the JFET is configured such that it works as a small-signal amplifier. Various methods of biasing configuration such common-drain, common-gate, and common-source configurations will be studied including its merit and demerit points.

The amplification can be achieved from *n*-channel JFET transfer characteristic and drain curves as they are shown in Fig. 4.12 and Fig. 4.13 respectively. Similarly, amplification can be achieved for *p*-channel JFET device.

As shown in Fig. 4.12, a small change of gate-to-source voltage V_{GS} can result a large change of drain current I_D.

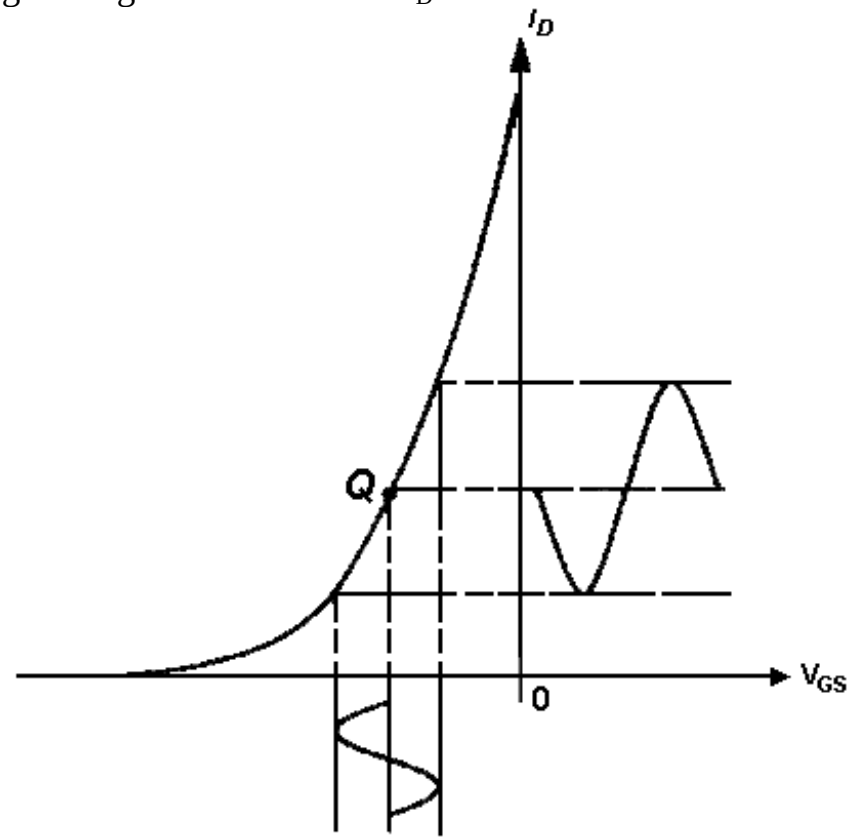


Figure 4.12: Transfer characteristic curve of *n*-channel JFET showing signal amplification

Similarly, once can see that the above-mentioned change would also show in the change of drain-to-source voltage V_{DS} as shown in Fig. 4.13.

Like in the case of bipolar junction transistor, the Q-point of the amplifier should be designed to set at the linear region of the transfer characteristic curve to avoid non-linearity distortion.

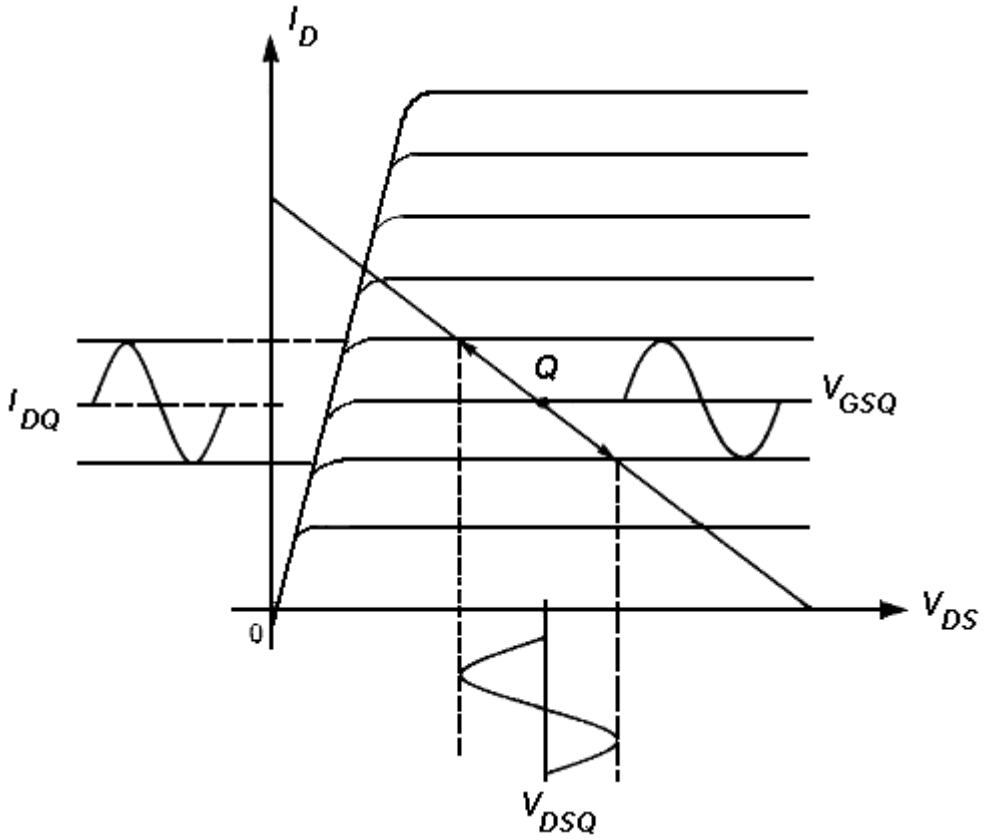


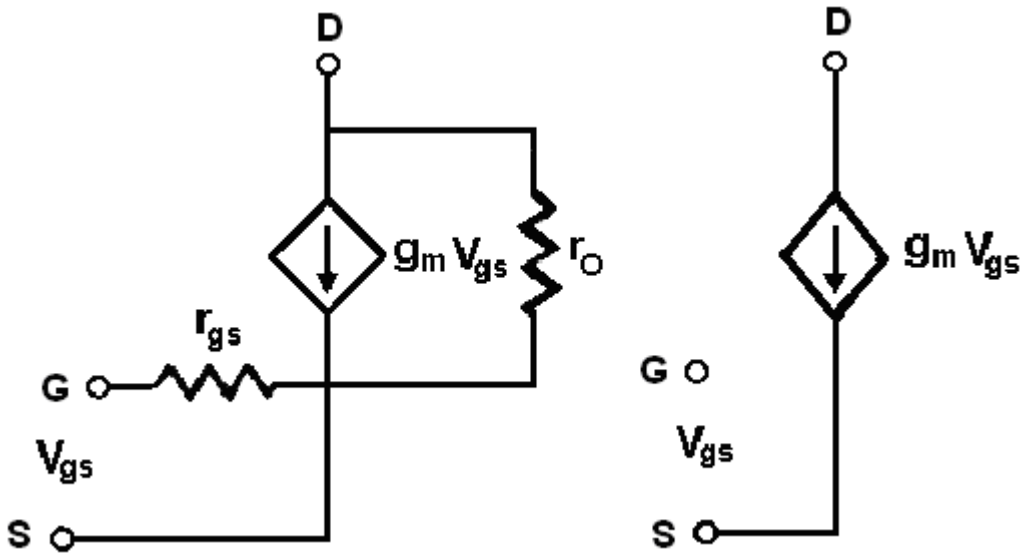
Figure 4.13: Drain curve of *n*-channel JFET showing signal amplification

Equation (4.4) defines dc transconductance as $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$. Thus, ac transconductance is defined as $g_m = \frac{I_d}{V_{gs}}$. By rearranging the equation, ac drain current is $I_d = g_m V_{gs}$.

4.4.1 Equivalent Circuits of FET

The hybrid π-model equivalent circuits of JFET are shown in Fig. 4.14. These circuits are applicable for JFET and MOSFET. The drain current I_d is equal to $g_m V_{gs}$ gate-source resistance r_{gs} and output impedance = r_o are introduced as shown in Fig. 4.14(a). If gate-to-source resistance r_{gs} is assumed to be infinitely large and r_O is large enough to be neglected, then the simplified equivalent circuit shall be Fig. 4.14(b). Output impedance r_o of the JFET can be determined

from the Early voltage V_M and drain current I_D using equation $r_0 = \frac{V_M + V_{DS}}{I_D} \cong \frac{V_M}{I_D}$.



(a) (b)

Figure 4.14: π-model of JFET/MOSFET ac equivalent circuit

The T-model of the JFET device, which is also the model for the MOSFET device, is shown in Fig. 4.15. The model is derived based on the fact the ac source resistance $R_{in(source)}$ of the JFET/MOSFET is equal to $R_{in(source)} = \frac{V_{gs}}{I_S} = \frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$.

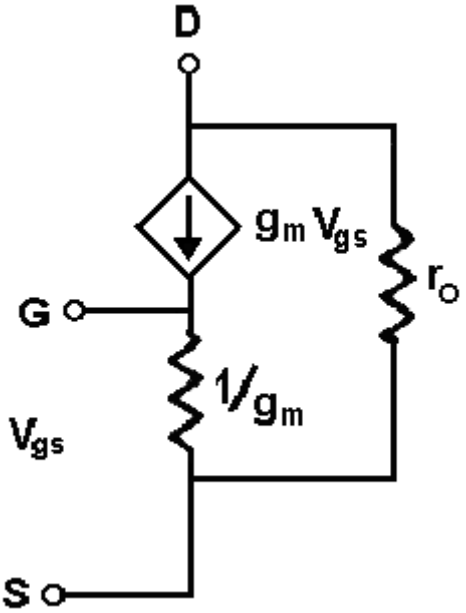


Figure 4.15: T-model of JFET/MOSFET ac equivalent circuit

4.4.2 Voltage Gain

The voltage gain A_V of the JFET with an external ac source as input is defined as $A_V = V_{out}/V_{in}$. For a self bias JFET amplifier, its ac equivalent circuit is shown in Fig. 4.16.

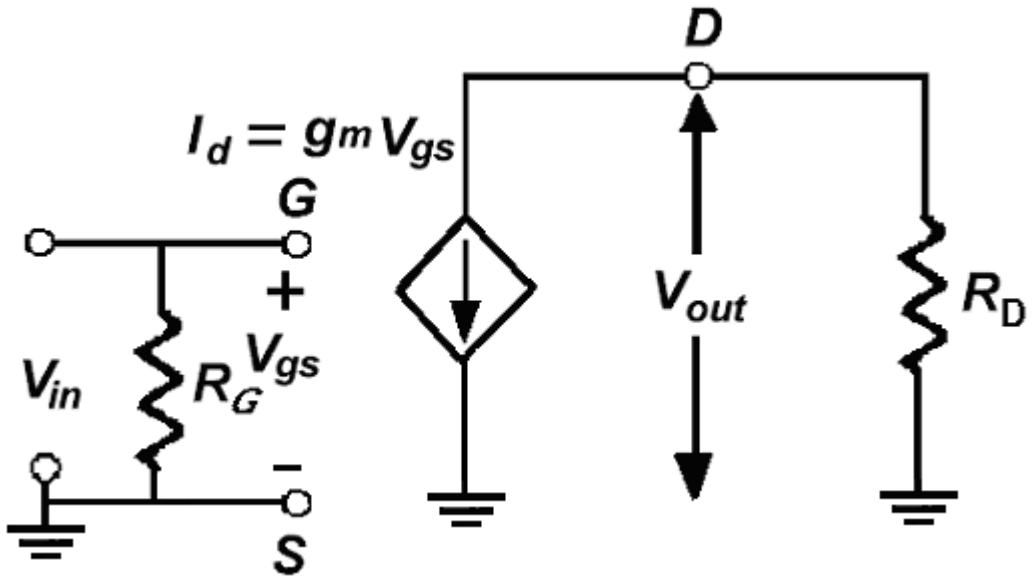


Figure 4.16: ac equivalent circuit

From the circuit, the output voltage V_{out} is $V_{out} = -V_{ds} = -I_dR_D$ and the input voltage V_{in} is $V_{in} = V_{gs} = I_d/g_m$. Thus, the voltage gain is equal to $A_V = V_{out}/V_{in}$ is

$$A_V = -\frac{I_d R_D}{I_d / g_m} = -g_m R_D \qquad (4.18)$$

4.4.3 Effect of r_o and R_S

If output impedance r_o of JFET is taken into consideration, the voltage gain A_V will be reduced to

$$A_V = -g_m \frac{R_D r_O}{R_D + r_O} \qquad (4.19)$$

If there is a source resistance R_S, where the ac equivalent circuit is shown in Fig. 4.17, voltage gain A_V is reduced further because input voltage V_{in} is not just equal to gate-to-source voltage V_{gs}. The input voltage V_{in} is $V_{in} = V_{gs} + V_{gs}g_mR_S = V_{gs}(1 + g_mR_S)$. Since output voltage V_{out} is $V_{out} = -g_mV_{gs}\frac{R_D r_O}{R_D + r_O}$. Therefore, the ac voltage gain A_V is

$$A_V = -\frac{g_m}{(1+g_m R_S)}\left(\frac{R_D r_O}{R_D + r_O}\right) \qquad (4.20)$$

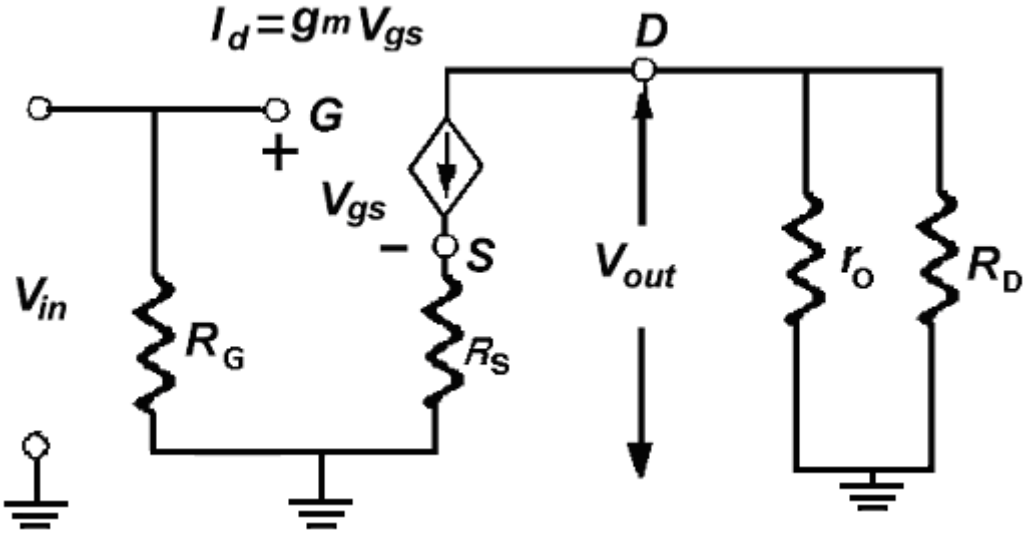


Figure 4.17: ac equivalent circuit with external source resistance R_s

4.4.4 Common-Source Amplifier

Figure 4.18 shows a common-source amplifier and its corresponding ac equivalent circuit is shown in Fig. 4.19.

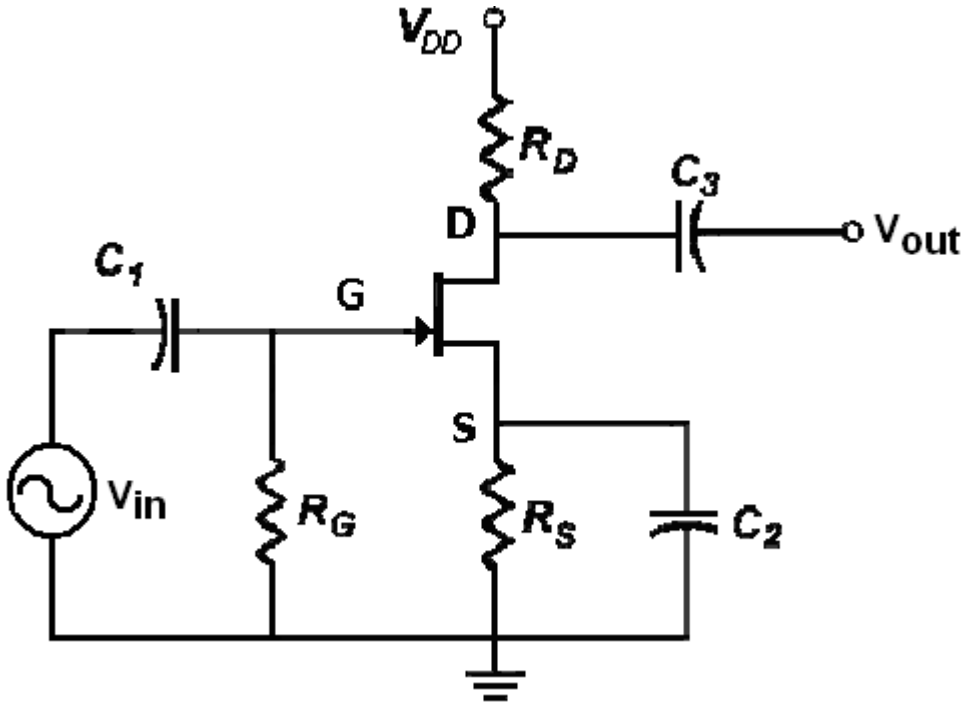


Figure 4.18: A common source JFET amplifier

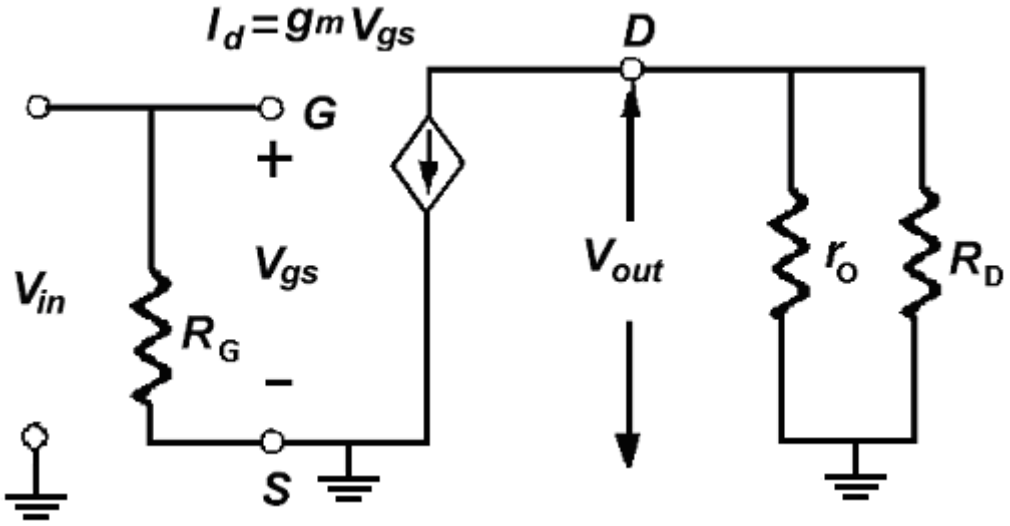


Figure 4.19: ac equivalent circuit of the common source JFET amplifier

If the dc circuit is biased at midpoint, then $I_D = I_{DSS}/2$. Otherwise, I_D needs to be known. Since it is self-bias then $V_{GS} = - I_D R_S$. Substitute V_{GS} into equation (4.3), it yields the drain current as $I_D = I_{DSS}\left[1+\frac{I_D R_S}{V_{GS(off)}}\right]^2$. Expanding the square term of the equation, it yields drain current $I_D = I_{DSS}\left[1+2\frac{I_D R_S}{V_{GS(off)}}+\frac{I_D^2 R_S^2}{V_{GS(off)}^2}\right]$. Rearrange this quadratic equation in the forms of $ax^2+bx+c=0$, it becomes $I_{DSS}+\left(\frac{2I_{DSS}R_S}{V_{GS(off)}}-1\right)I_D+\frac{I_{DSS}R_S^2}{V_{GS(off)}^2}I_D^2=0$, whereby the coefficients are $a = \frac{I_{DSS}R_S^2}{V_{GS(Off)}^2}$, b $=\left(\frac{2I_{DSS}R_S}{V_{GS(off)}}-1\right)$, and c = I_{DSS} respectively. Thus, drain-current I_D is obtained from $I_D = \frac{-b\pm\sqrt{b^2-4ac}}{2a}$. It yields two values for drain current I_D. One needs to consider the value of I_{DSS} before the right value of I_D to be chosen. The drain current shall not be greater than I_{DSS} current.

The drain-to-source voltage V_{DS} is obtained from equation (4.21).

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S \qquad (4.21)$$

The input impedance of the gate is extremely high so it can be neglected. However, if I_{GSS} and V_{GS} are given then it can be calculated using equation (4.9).

4.4.5 Common-Drain Amplifier

Figure 4.20 shows a common-drain amplifier. It is also called *source-follower*. Unlike the bipolar junction transistor common-collector amplifier, it is called *emitter-follower*. The ac equivalent circuit of the amplifier is shown in Fig. 4.21.

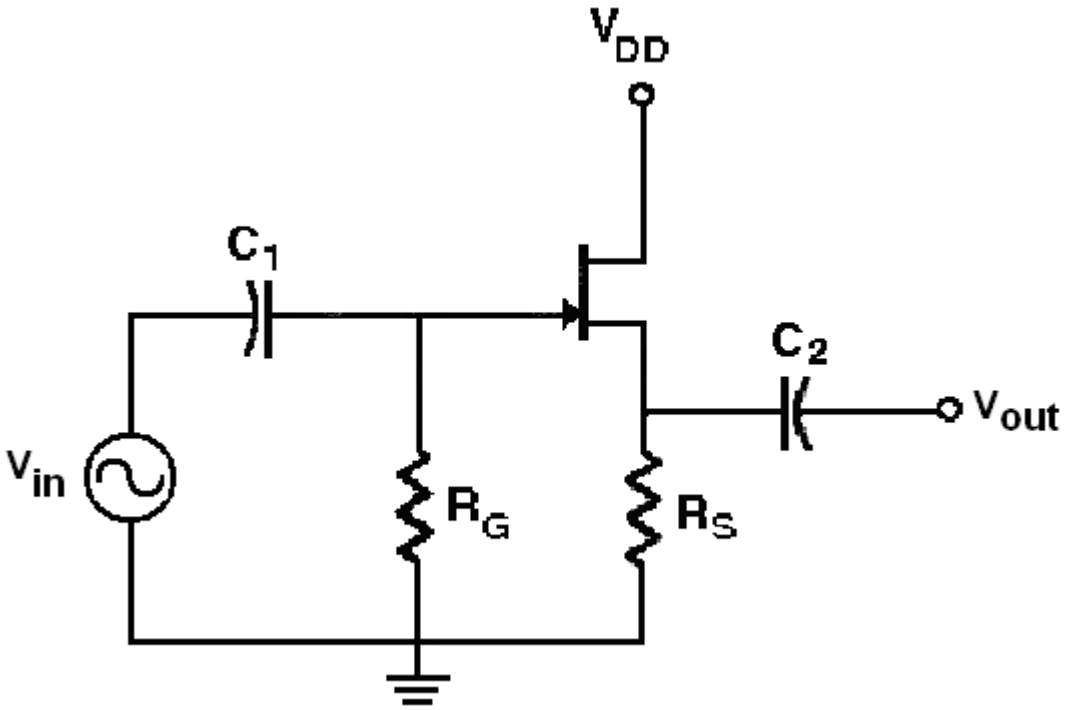


Figure 4.20: A common-drain amplifier

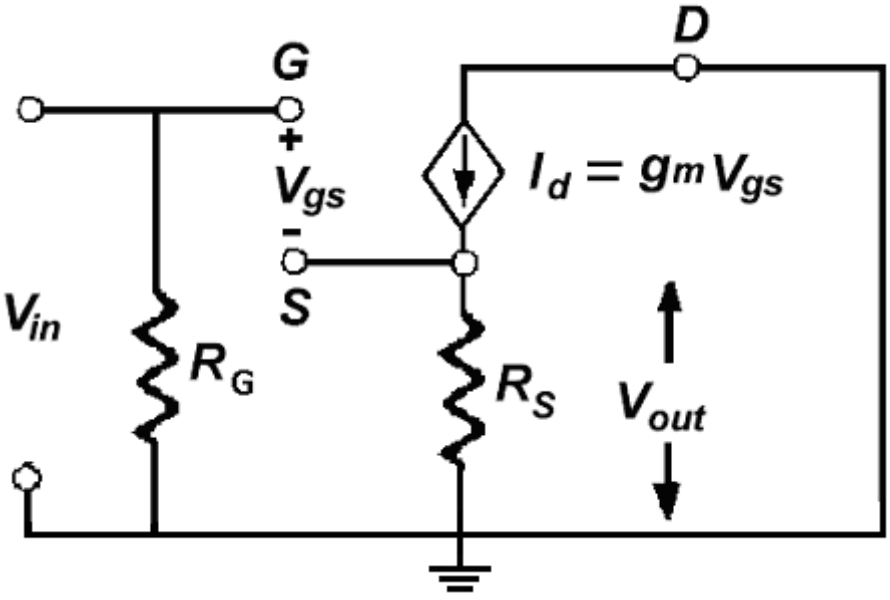


Figure 4.21: The ac equivalent circuit of the common-drain amplifier

As usual voltage gain A_V is $A_v = V_{out}/V_{in}$. The input voltage V_{in} is $V_{in} = V_{gs} + I_dR_S$. The output voltage V_{out} is $V_{out} = I_dR_S$. The voltage gain A_V shall then be equal to $A_V = I_dR_S/(V_{gs} + I_dR_S)$.

Recall that transconductance g_m is $g_m = I_d/V_{gs}$. Substituting drain current I_d equals to $I_d = g_mV_{gs}$, the voltage gain A_V shall be

$$\mathbf{A_V} = \frac{g_mR_S}{1+g_mR_S} \qquad (4.22)$$

Thus, one can see that the gain is always less than one. If $g_mR_s >> 1$ then $A_v \cong 1$.

The input impedance of the gate $R_{IN(gate)}$ is very high and it can be calculated from the gate reverse current I_{GSS} value for a specified V_{GS} value from data sheet of the JFET using equation (4.9). If these data are given for a specified JFET then the input impedance R_{IN} for the amplifier shall be $R_{IN(gate)}$ parallel with gate resistance R_G.

4.4.6 Common-Gate Amplifier

The common-gate amplifier is shown in Fig. 4.22 and its corresponding ac equivalent circuit is shown in Fig. 4.23.

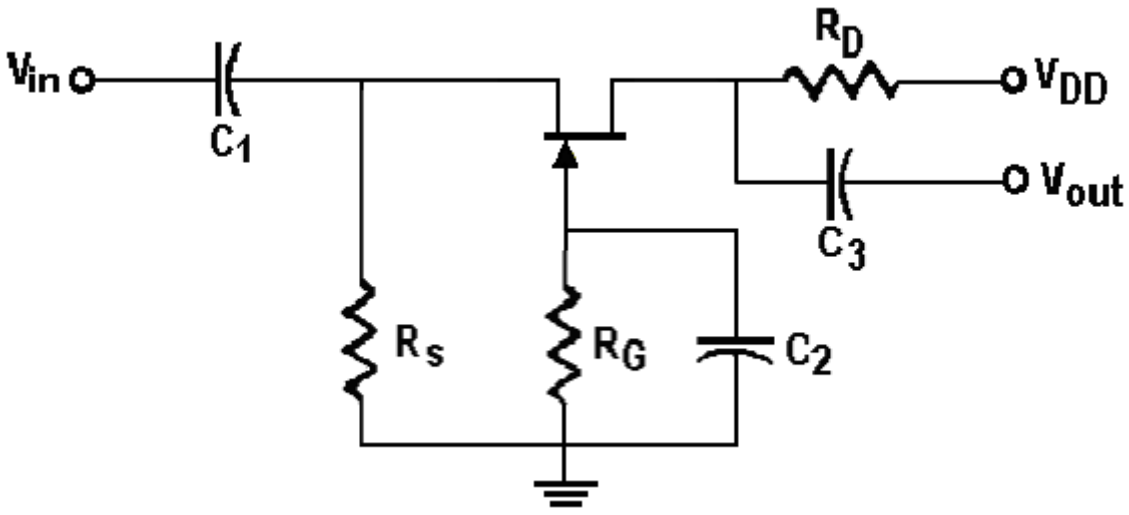


Figure 4.22: A common-gate amplifier

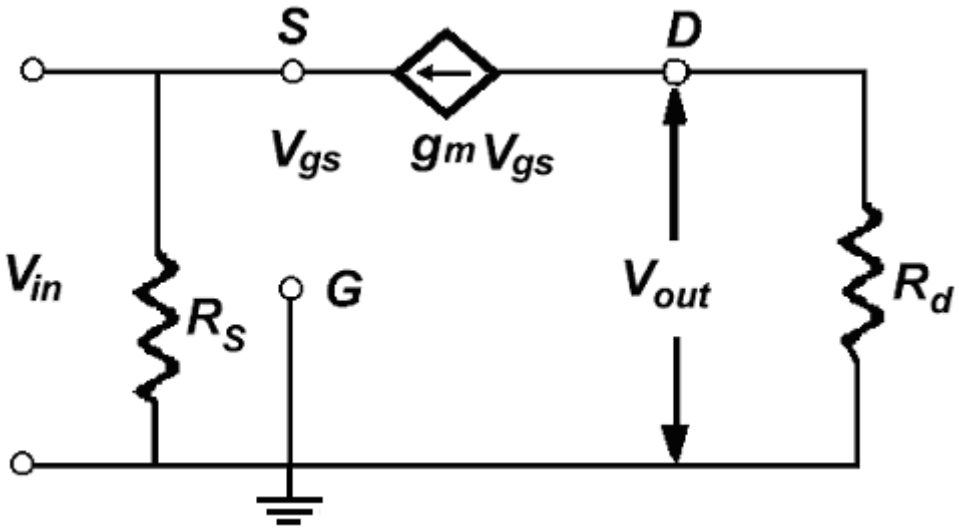


Figure 4.23: The equivalent circuit of the common-gate amplifier

The voltage gain A_V is $A_V = -V_{out}/V_{in}$ and taking equation (4.4) for the drain current I_d, which is equal to $g_m V_{gs}$. The voltage gain shall be

$$A_v = - V_{out}/V_{gs} = -I_d R_D/V_{gs} = g_m V_{gs} I_d R_D/V_{gs}$$
$$= - g_m R_d \qquad (4.23)$$

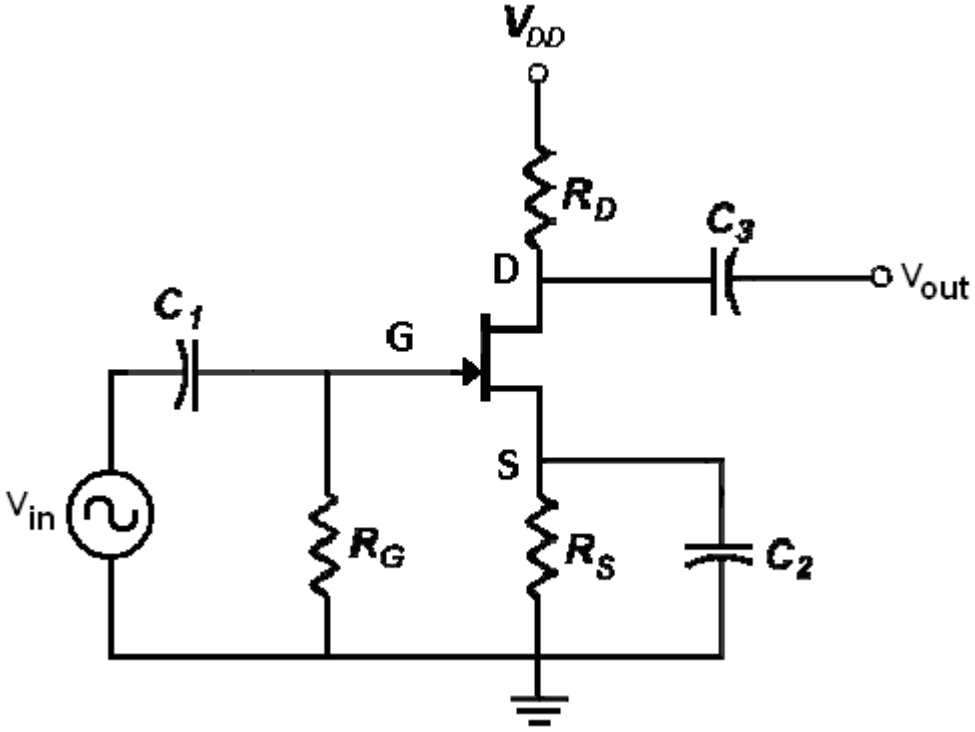
The input impedance $R_{in(source)} = V_{in}/I_{in}$. Since the input voltage V_{in} is $V_{in} = V_{gs}$ and $I_{in} = I_d = g_m V_{gs}$. The ac source resistance $R_{in(source)}$ shall be

$$R_{in(source)} = 1/g_m \qquad (4.24)$$

From equation (4.24), it tells us that the input impedance $R_{in(source)}$ is small, which true because the source should have low impedance.

Example 4.5

From the circuit of common source JFET amplifier shown in the figure, its has $V_{GS(off)} = -2.0V$, $I_{DSS} = 1.4mA$. If you need this amplifier to be biased with $I_D = 0.7mA$, $V_{DD} = 20V$, and voltage gain of 20dB, what is the value of R_S, and R_D?



Solution

Using equation (4.3), the drain current I_D is $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2 = 0.7\text{mA} = 1.4\text{mA}\left[1-\frac{V_{GS}}{2\text{V}}\right]^2$. Solving this equation for gate-to-source voltage V_{GS} is yield equal to - 0.59V.

From equation (4.7), the transconductance at gate-to-source voltage equal to zero volt. i.e. V_{GS} = 0 V is $g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}} = -\frac{2\text{x}1.4\text{mA}}{-2.0\text{V}} = 1.4\text{mA/V}$.

From equation (4.8), the transconductance g_m for drain current I_D = 0.7mA is $g_m = g_{m0}\sqrt{I_D / I_{DSS}} = 1.4\text{mA/V}\sqrt{0.7\text{mA}/1.4\text{mA}} = 0.99\text{mA/V}$.

From equation (4.12), the source resistance is $R_S = |V_{GS}/I_D| = |0.59\text{V}/0.7\text{mA}| = 842.8\Omega$.

Voltage gain A_V of 20dB corresponds to absolute voltage gain A_V equal to 10.

From equation (4.13), voltage gain A_V is $A_V = g_m R_D$, then drain resistance R_D is $R_D = A_V/g_m = 10/0.99\text{mA/V} = 10.1\text{k}\Omega$.

4.5 Multistage Amplifier

The two-stage *n*-channel JFET amplifier is shown in Fig. 4.24. Recall the multiple stage bipolar junction transistor amplifiers; the voltage gain of the first stage is decreased by the load effect created by the input impedance of the following stage.

However, the input impedance of each stage of multistage JFET amplifier is very high that it has little effect on the preceding stage and it can be neglected.

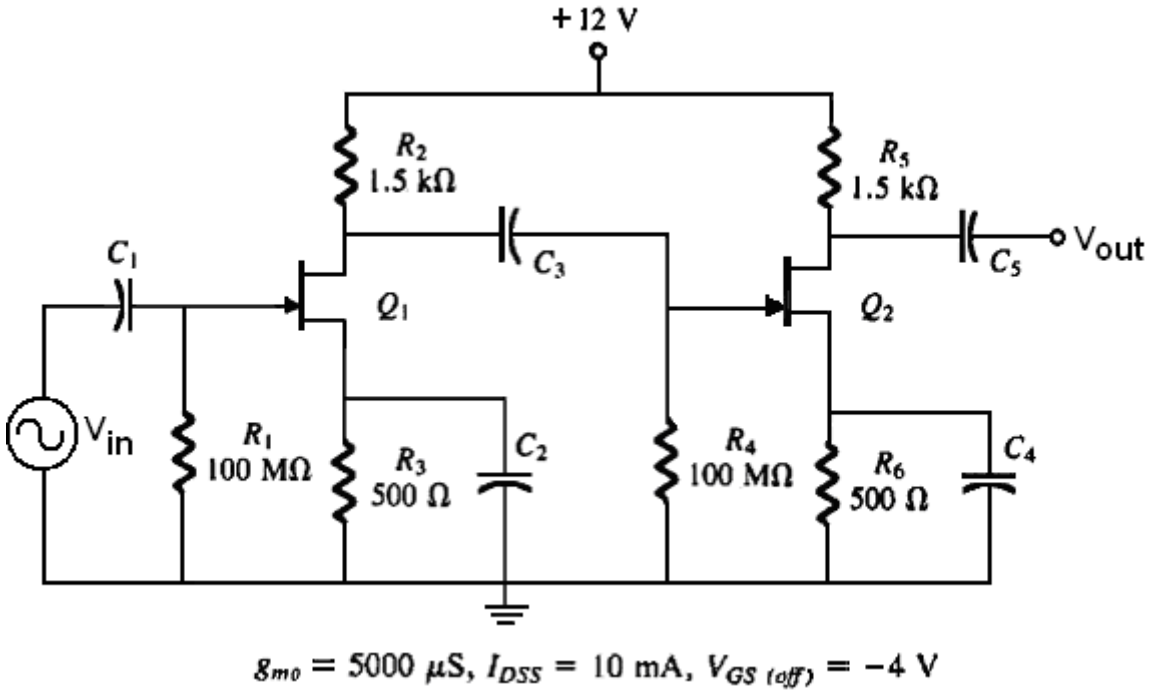


Figure 4.24: A two-stage JFET amplifier

The drain current is found to be 3.36mA. The transconductance shall then be 2.9mS. Thus, the overall gain of this two-stage amplifier is $A_V = A_{V1}A_{V2}$ which is equal to (2833μS)(1.5kΩ)(2833μS)(1.5kΩ) = 18.9.

In decibel it is A_V (dB) = 20log(18.9) = 25.5dB.

Tutorials

4.1. Describe and draw the diagrams to illustrate, how the *n*-channel and *p*-channel JFET should be biased for normal operation.

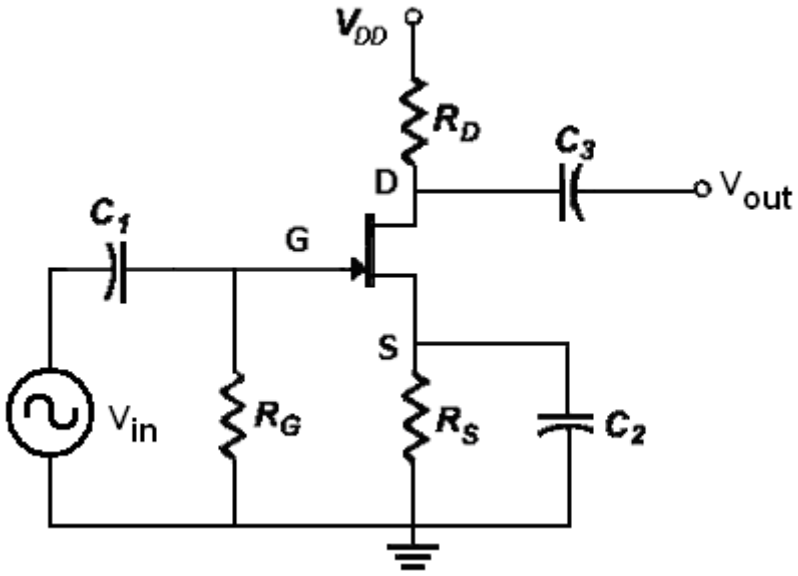
4.2. The data sheet for certain type of JFET indicates that I_{DSS} = 25mA, $V_{GS(off)}$ = -10V, and g_{m0} = 5000μS.

Determine
(i) The type of JFET
(ii) Drain current I_D at V_{GS} = 0
(iii) Drain current I_D and transconductance g_m at V_{GS} = - 4V.

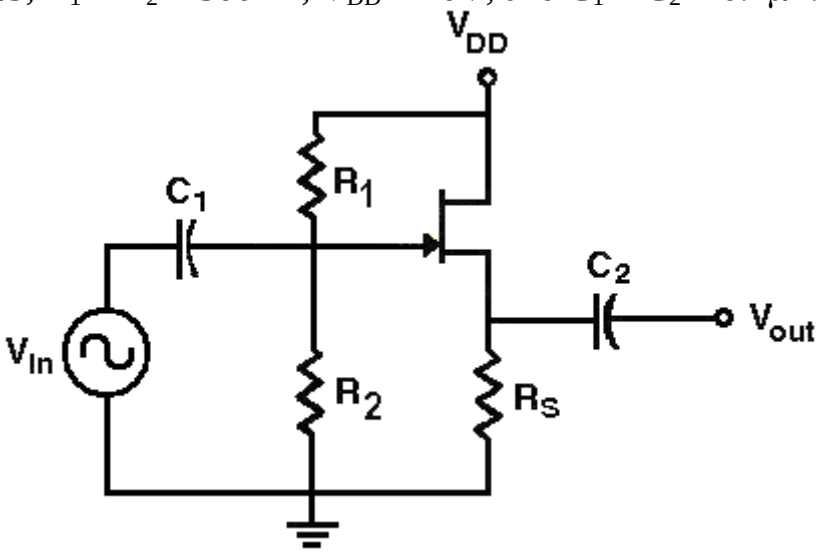
4.3. Given that $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2$, $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$, and $g_m = g_{m0}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]$, prove that $g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$ and $g_m = g_{m0}\sqrt{I_D / I_{DSS}}$.

4.4. An *n*-channel JFET has a pinch-off voltage V_P of – 4.5V and I_{DSS} = 9.0mA. At what value of V_{GS} in the pinch-off region will I_D equal to 3.0mA and what is the value of $V_{DS(P)}$ when I_D = 3.0mA?

4.5. From the circuit of common source JFET amplifier shown in figure, its has $V_{GS(off)}$ = -2.0V, I_{DSS} = 1.4mA. If you need this amplifier to be biased with I_D = 0.7mA, V_{DD} = 20V, and voltage gain of 20dB, what is the value of R_S, and R_D?



4.6. Given a common drain JFET amplifier has $V_{GS(off)}$ = -8.0V, g_{m0} = 6000μS, $R_1 = R_2$ = 500kΩ, V_{DD} = 20V, and $C_1 = C_2$ = 0.1μF.



(i) Calculate the values of output impedance and input impedance of the amplifier when gate-to-source voltage V_{GS} are -1.0V and -0.5V?
(ii) Calculate the drain-to-source current I_{DS} when V_{GS} is -1.5V?
(iii) What is the ac voltage gain A_V of this amplifier when a load R_L of 15.0kΩ is connected at V_{GS} = -1.5V?

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