Circuit maximizes pulse-width-modulated DAC throughput

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Simple DACs realized by lowpass filtering microcontroller-generated pulse-width-modulated (PWM) signals have a response that is typically a tenth of the PWM frequency. This Design Idea is a novel implementation of a previously published method[1] employing a reference ramp whose output is sampled and held by the PWM signal. This approach results in a throughput rate equal to the PWM frequency.

You can use the circuit in **Figure 1** to implement a ±10V 10-bit DAC with a throughput of 20 kHz. A DSPIC30F4011 microcontroller (not shown) is operated at a clock frequency of 96 MHz to generate the capture signals OC_1 and OC_4. Clock/4 is fed to an internal 16-bit timer whose period is set for a count of 1200 corresponding to a PWM frequency of 20 kHz. Signal OC_4 is mostly high and goes low at a fixed count of 1170 as a reference for ramp generation. IC_{1A}, along with Q_1, forms a precision constant-current source that linearly charges capacitor C_2 when Q_2 is off. This signal inverted by IC_{3A} switches Q_2 on for a period of 30 counts to discharge C_2 for the start of the next ramp. IC_{1B} buffers, amplifies, and offsets the ramp; potentiometers R_2 and R_5 adjust the offset and gain.

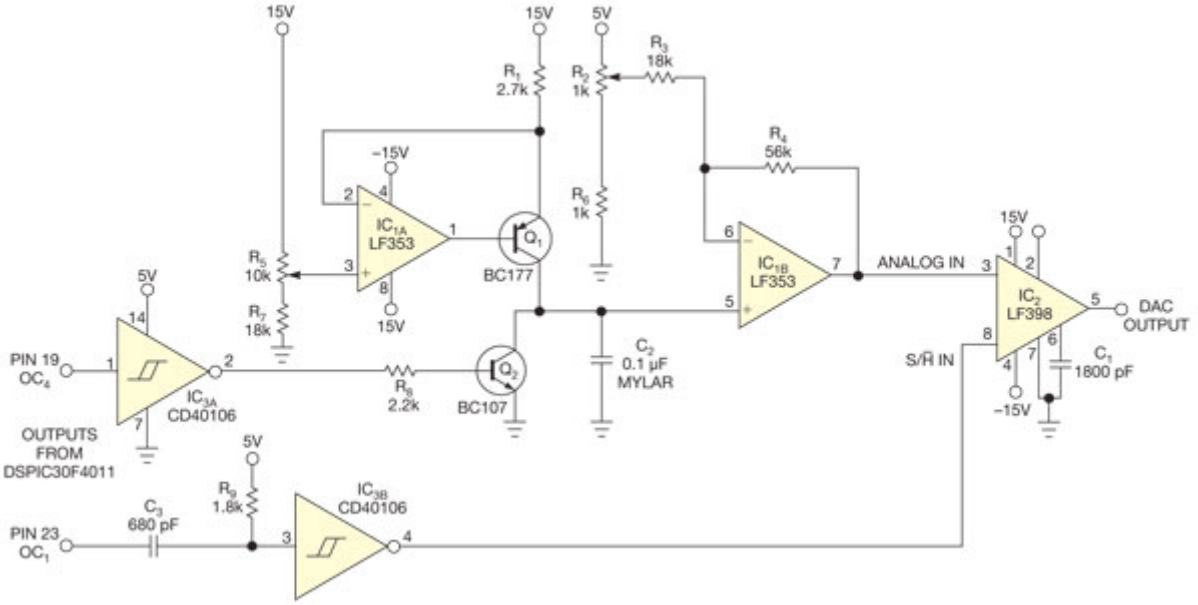

Figure 1 The off-page microcontroller generates signals for ramp control (OC_4) and sample timing (OC_1).

The OC_1 falling edge controls the PWM DAC sample timing relative to the ramp voltage. The data word to be converted determines the OC_1 duty cycle by comparing it internally in the microcontroller with the internal 16-bit timer. C_3 and R_9 differentiate the resulting PWM signal; IC_{3B} then inverts it,

forming a 1-µsec sample signal for the sample-and-hold IC_2. Pin 5 of IC_2 forms the DAC output and is adjusted to −10, 0, and +10V for OC_1 PWM counts of 88, 600, and 1112, respectively, corresponding to a 10-bit count of 1024.

The count offset of 88 helps to avoid the initial nonlinear region of the ramp so that the PWM DAC shows good linearity with a LSB of 20 mV and an accuracy of ±40 mV. Additional PWM DACs could also be implemented using capture PWM outputs OC_2 and OC_3.

Figure 2 shows the waveforms to be expected for a DAC output corresponding to 256 on a 10-bit scale of 1024. OC_4 forms the PWM reference based on which a 20-kHz bipolar ramp signal is output at Pin 7 of IC_{1B}. This ramp is sampled and held at a count of 256+88=344, corresponding to a DAC output of −5V.

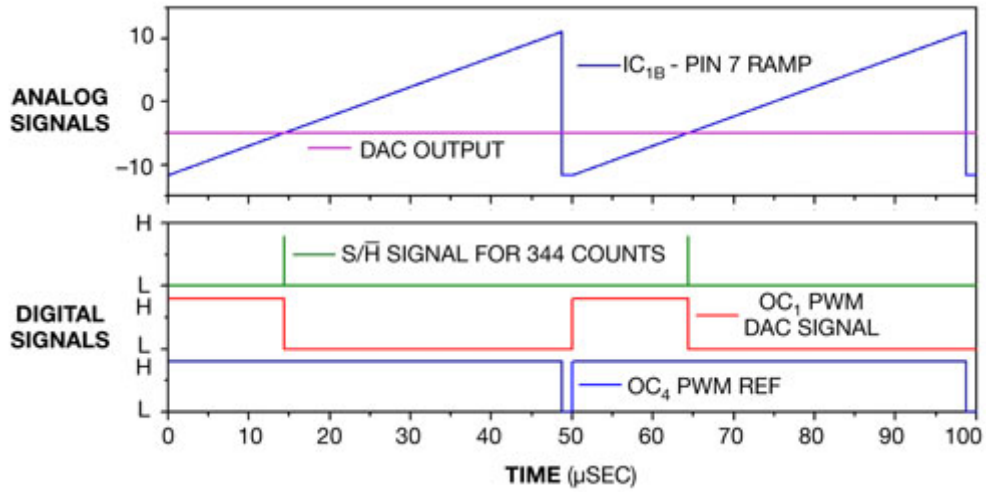

Figure 2 The differentiated OC_1 falling edge generates the S/H sample pulse at the ramp −5V point.

References

1. Kester, Walt (editor), The DataConversion Handbook, section 3-1, pg 3-28, Newnes, 2005.
2. Raman, Ajoy, "Universal Analog Hardware Testbench."