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"Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS *Technology*"

Er. Rajni

Abstract This paper presents a design of the Folded-cascode operational amplifier using 1.25µm CMOS technology, which leads to high gain as compared to a normal cascode circuit. The simulation of the cascode and folded cascode circuits is done using TSPICE simulation tool and the LEVEL–2, 1.25 µm parameters are used. A complete analysis of the circuit is presented in this paper which shows how this circuit leads to a high gain and resistance at output. A comparison between the cascode and Folded-Cascode op amps is described. We have also described their simulated and calculated results comparison individually. This paper provides a considerable insight into the overall operation and advantages of the folded-cascode circuit. This design overcomes some limitations and drawbacks of the various previously presented described architectures.

Index Terms Operational amplifier, complementary metal-oxide semiconductor, common-mode range, input common-mode range, power-supply rejection ratio.

1 Introduction

The design of op amps continues to pose a challenge as the supply voltage and transistor channel length scale down with each generation of CMOS technologies. Operational amplifiers are the amplifier (controlled sources) that has sufficiently high gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of the op amp. This principle has been exploited to develop many useful analog circuits and systems. The primary requirement of an op amp is to have an open-loop gain that is sufficiently large to implement the negative feedback concept.
Different architectures have been used [10],[11],[12],[13] to obtain high gain bandwidth, output resistance and power-supply rejection. Two-stage Cascode op amps circuits are widely used in circuit designs at places where high gain and high output impedances are required. Folded cascade gives better performance even than the cascode op amp circuit. These architectures have been compared, using TSPICE simulations, in this paper along with drawbacks and advantages of each.

The difference between an Operational Transconductance Amplifier (OTA) and an Operational Amplifier (Op-Amp) is that the op-amp has got an output buffer so that it is able to drive resistive loads. An OTA can only drive capacitive loads.

Our goal is the design analysis and simulation of a High Gain Folded-Cascode Op Amp using CMOS process in order to use it in wide applications ([7],[14],[17],18]) like in the design of high-order filters, signal amplifiers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, input and output signal buffers, and many more, and to compare its some of the performance parameters with the two-stage cascode op-amp by designing cascode op-amp for the almost same specifications.

The paper is organized as follows: in section-2 we present all the configurations for simulating and measuring the above specified and many other characteristics. The section-3 gives conclusion of this paper.

2 Cascode Stage

As we know the input signal of a common-gate stage may be a current and also that in the common-source arrangement a transistor converts a voltage signal to a current signal. **The cascade of a CS stage and a CG stage is called a 'cascode' topology,** which provides many useful properties. Fig.2.1 shows the basic configuration: M1 generates a small signal drain current that is proportional to V_{in} and M2 simply routes the current to R_D. We call M1 the input device and M2 the cascode device. Note that in this example, M1 and M2 carry equal currents. As we describe the attributes of the circuit in this section, many advantages of the cascode topology over a simple Common-Source stage become evident. [Razavi, design of Analog CMOS Integrated Circuits]

• *Author is currently working as Assistant Professor at JCDM college of Engg., Sirsa(Hry), India. E-mail: er.rajni08@gmail.com*

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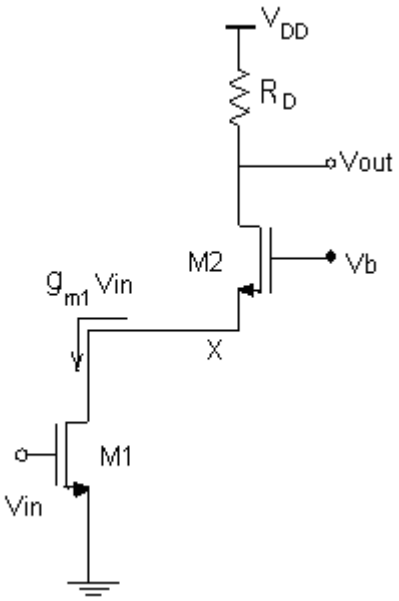

Figure.2.1 Cascode stage

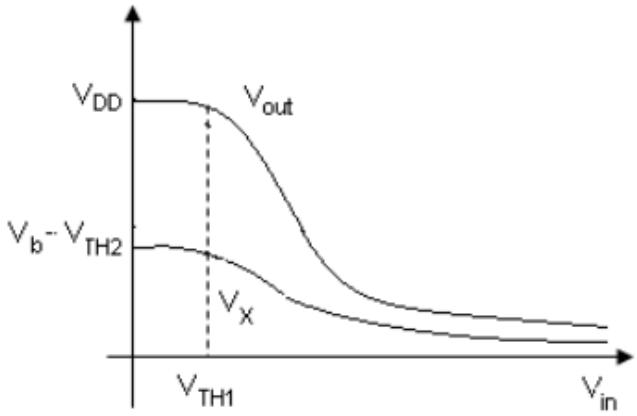

Figure.2.2 Input-output characteristics of a cascode stage

3 Design Approach of The Two-Stage Cascode Op-Amp

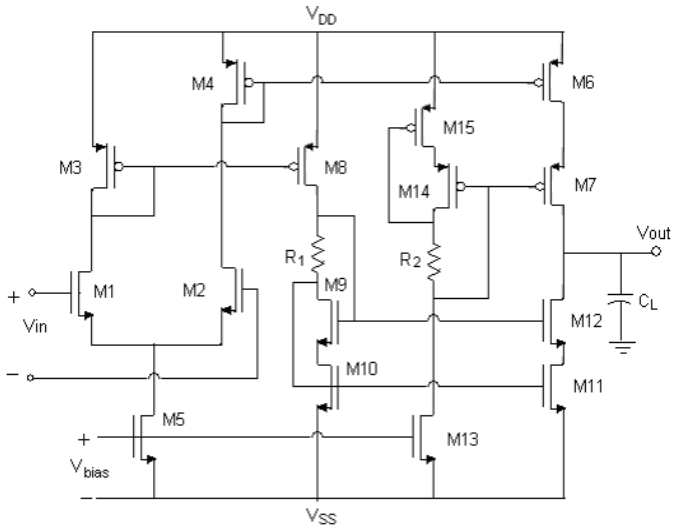

Figure.3.1 Two-stage Cascode op amp

3.1 Specifications

1. $V_{DD} = V_{SS}$ =2.5V
2. Slew rate = 5V/ μs with a 50 pF load
3. GB = 10MHZ with a 10 pF load
4. $A_v \geq 5000 V/V$
5. ICMR = -1 to +1.5V
6. Output swing = $\pm$ 1.5 V

3.2 Design Equations to be used:

1. Slew rate = $\frac{I_{out}}{C_L}$ (1)

2. $GB = \frac{g_{m1}(g_{m6} + g_{m8})}{2g_{m3}C_L}$ (2)

3. $A_v = \frac{g_{m1}}{g_{m3}}\left(\frac{g_{m6} + g_{m8}}{2}\right)R_{II}$ (3)

4. Positive CMR

$$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right]|V_{TO3}|(\max) + V_{T1}(\min) \quad (4)$$

5. Negative CMR

$$V_{in}(\min) = V_{SS} + V_{DS5}(sat) + \left[\frac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\max) \quad (5)$$

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6. $g_m = \sqrt{2 \times K'_{N,P} \times S_{N,P} \times I_D}$ (6)

7. $g_{ds} = \lambda I_D$ (7)

8. $r_{ds} = 1/\lambda I_D$ (8)

9. $V_{DS}(sat) = \sqrt{\frac{2I_{DS}}{\beta}}$ (9)

10. The overall gain of the input stage is

$$A_{vI} = g_{m2}/g_{m4} = g_{m1}/g_{m3} \quad (10)$$

11. The gain of second stage is

$$A_{vII} = \left(\frac{g_{m6} + g_{m8}}{2}\right) R_{II} \quad (11)$$

Where R_{II} is given by

$$R_{II} = (g_{m7} r_{ds7} r_{ds6}) \| (g_{m12} r_{ds12} r_{ds11}) \quad (12)$$

therefore

$$A_v = (g_{m1}/2g_{m4})(g_{m6} + g_{m8}) k R_{II} \quad (13)$$

TABLE 4.1. TRANSISTOR SIZING OF THE TWO-STAGE CASCODE OP AMP CIRCUIT OF FIG.4.3

Sr. No.	(W/L) ratios	Transistor widths
1.	$S_1 = S_2 = 25$	$W_1 = W_2 = 31.25$
2.	$S_3 = S_4 = 30.36$	$W_3 = W_4 = 38$
3.	$S_5 = 15$	$W_5 = 18.75$
4	$S_6 = S_7 = S_8 = 76$	$W_6 = W_7 = W_8 = 95$
5.	$S_9 = S_{10} = S_{11} = S_{12} = 31.61$	$W_9 = W_{10} = W_{11} = W_{12} = 39.51$
6.	$S_{13} = 20$	$W_{13} = 25$
7.	$S_{14} = S_{15} = 76$	$W_{14} = W_{15} = 95$

4 DESIGN APPROACH FOR THE FOLDED-CASCODE OP-AMP

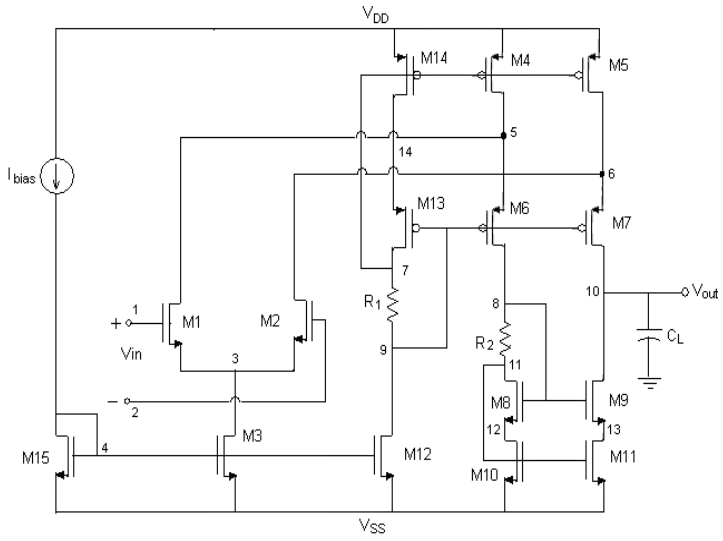

Figure 4.1 Proposed folded cascode op amp

4.1 Spesifications For the Design:

1. Power Supply, $V_{DD} = V_{SS} = \pm 2.5V$
2. Slew rate (SR) = 10V/μS
3. Load capacitance, C_L = 10pF
4. Output Voltage Swing (V_{out}(swing)) = $\pm$ 2V
5. Gain Bandwidth (GB) = 10MHz
6. Input Common-Mode Voltage Range (ICMR) = -1.5V to +2.5V
7. Differential Voltage Gain (A_v) $\geq$ 5000V/V
8. Power Dissipation $\leq$ 5mW

4.2 Design Equations to be used:

1. Slew rate = $\frac{I_3}{C_L}$

2. Bias currents in output cascodes, avoiding zero currents in cascodes

$$I_4 = I_5 = 1.2I_3 to 1.5I_3$$

3. Using maximum output voltage, $v_{out}(\max)$

$$S_5 = \frac{2I_5}{K'_P V^2_{SD5}}, S_7 = \frac{2I_7}{K'_P V^2_{SD7}} \quad (14)$$

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$$V_{SD5}(sat) = V_{SD7}(sat) = \frac{V_{DD} - V_{out}(\min)}{2} \quad (15)$$

$$Let S_4 = S_{14} = S_5 \text{ and } S_{13} = S_6 = S_7 \quad (16)$$

4. Using minimum output voltage, $V_{out}(\min)$

$$V_{DS9}(sat) = V_{DS11}(sat) = \frac{V_{out}(\min) - |V_{SS}|}{2} \quad (17)$$

$$S_{11} = \frac{2I_{11}}{K'_N V^2_{DS11}}, \quad S_9 = \frac{2I_9}{K'_N V^2_{DS9}} \quad (18)$$

Let $S_{10} = S_{11}$ and $S_8 = S_9$ (19)

5. Self-bias cascade

$$R_1 = V_{SD14}(sat) \setminus I_{14} \text{ and } R_2 = V_{DS8}(sat) \setminus I_6 \quad (20)$$

6. $GB = \frac{g_{ml}}{C_L}$

$$S_1 = S_2 = \frac{g^2_{ml}}{K'_N I_3} = \frac{GB^2 C^2_L}{K'_N I_3} \quad (21)$$

7. Using minimum input CM

$$S_3 = \frac{2I_3}{K'_N}\left[V_{in}(\min) - V_{SS} - \sqrt{\frac{I_3}{K'_N S_1}} - V_{T1}\right]^2 \quad (22)$$

8. Using maximum input CM

S_4 and S_5 must meet or exceed the requirement of step 3

$$S_4 = S_5 = \frac{2I_4}{K'_P(V_{DD} - V_{in}(\max) + V_{T1})} \quad (23)$$

9. Differential voltage gain

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right)R_{II} = \left(\frac{2+k}{2+2k}\right)g_{m1}R_{II} \quad (24)$$

10. Power dissipation

$$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{12} + I_{10} + I_{11}) \quad (25)$$

11. Positive CMR

$$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right]|V_{TO3}|(\max) + V_{T1}(\min)$$

12. Negative CMR

$$V_{in}(\min) = V_{SS} + V_{DS5}(sat) + \left[\frac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\max)$$

13. $R_9 \approx g_{m9} r_{ds9} r_{ds11}$ (26)

14. The second stage resistance is

$$R_{II} = R_9 \left\| g_{m7} \frac{1}{g_{ds7}} \left(\frac{1}{g_{ds2}} \right\| \frac{1}{g_{ds5}} \right) \quad (27)$$

$$R_{II} = g_{m9} r_{ds9} r_{ds11} \left\| g_{m7} \frac{1}{g_{ds7}} \left(\frac{1}{g_{ds2}} \right\| \frac{1}{g_{ds5}} \right) \quad (28)$$

15. The small-signal voltage gain is given by

$$A_v = \left(\frac{2+k}{2+2k}\right) g_{ml} R_{II} \quad (29)$$

where $k = \frac{R_9(g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}}$

16. $g_m = \sqrt{2 \times K'_{N,P} \times S_{N,P} \times I_D}$

17. $g_{ds} = \lambda I_D$

18. $r_{ds} = 1/\lambda I_D$

19. $V_{DS}(sat) = \sqrt{\frac{2I_{DS}}{\beta}}$

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TABLE 4.2.1 TRANSISTOR SIZING OF THE PROPOSED FOLDED CASCODE OP AMP CIRCUIT OF FIG. 4.1

Sr. No	(W/L) ratios ($V/\mu m$)	Transistor widths (μm)
1.	$S_1 = S_2 = 62.45$	$W_1 = W_2 = 78.1$
2.	$S_3 = 140.5$	$W_3 = 175.6$
3.	$S_4 = S_5 = S_{14}$=152	$W_4 = W_5 = W_{14} = 23.75$
4.	$S_6 = S_7 = S_{13} =$ 30.36	$W_6 = W_7 = W_{13} = 38$
5.	$S_8 = S_9 = S_{10} = S_{11}$ =63.22	$W_8 = W_9 = W_{10} = W_{11} =$ =79.025
6.	S_{12}= 175.63	$W_{12} = 219.53$
7.	S_{15} = 62.45	$W_{15} = 78.1$

5 SIMULATION RESULTS

For simulating the proposed cascode and the folded cascode Op-Amp topologies in TSPICE, $1.25\mu m$ CMOS technology parameters [TSPICE model ml2_125] taken for NMOS and PMOS transistors are as mentioned in Table.5.1 and Table.5.2.

TABLE.5.1 PARAMETERS OF NMOS

Parameter	Value
VTO	0.622490
Kn	63.266
GAMMA	0.639243
PHI	0.31
LAMBDA	0.02

TABLE.5.2 PARAMETERS OF PMOS

Parameter	Value
VTO	-0.63025
Kp	26.354
GAMMA	0.618101
PHI	0.541
LAMBDA	0.02

The following table shows the comparison between the performance parameters taken in specifications for the design and that resulted after simulations of the Folded Cascode Op Amp.

TABLE.5.4. RESULTS FOR THE FOLDED CASCODE OP-AMP

Sr.No.	Performance parameters	Specifications	Simulated Results
1.	Voltage Gain (V/V)	>5000	6053
2.	Unity Gain Frequency (MHz)	10 MHz	8 MHz
3.	ICMR (V)	-1.5V to +2.5V	-1.0V to 2.5V
4.	PSRR (dB)	60dB	55dB
5.	Output Swing (V)	$\pm$ 2V	-2.3V to +2.0V
6.	Slew Rate (V/us)	10 V/us	8.55V/us

5.1 Simulated Waveforms of Folded Cascode Op Amp

The performance evaluation of the cascode and folded cascode op amps has been carried out, with the proposed circuits, having the loading capacitance of $10pF$, dual voltage supply of $\pm 2.5V$ and using the CMOS $1.25\mu m$ technology. For comparison, the transistors used in op amps have been sized for almost same specifications.

Simulated results show that this op amp exhibits high DC gain, improved ICMR. The typical values for DC gain is of the order of $6.035KV/V$, ICMR is of the order of -1.0V to 2.5Vand unity gain bandwidth of the order of 8MHz have been obtained.

Simulated results waveforms

1 ICMR MEASUREMENT:

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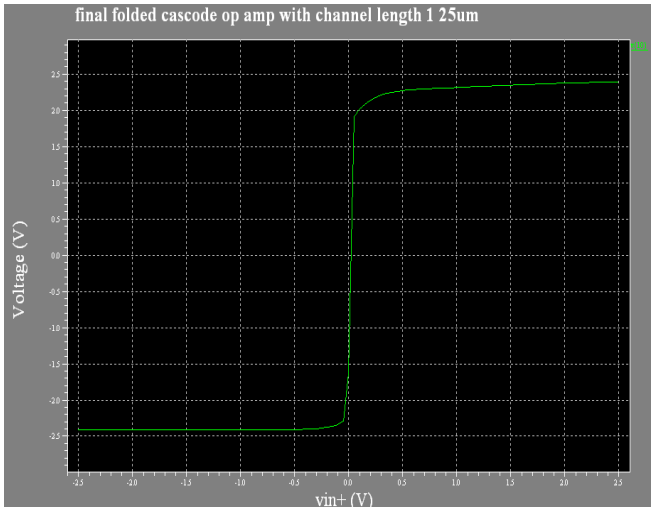
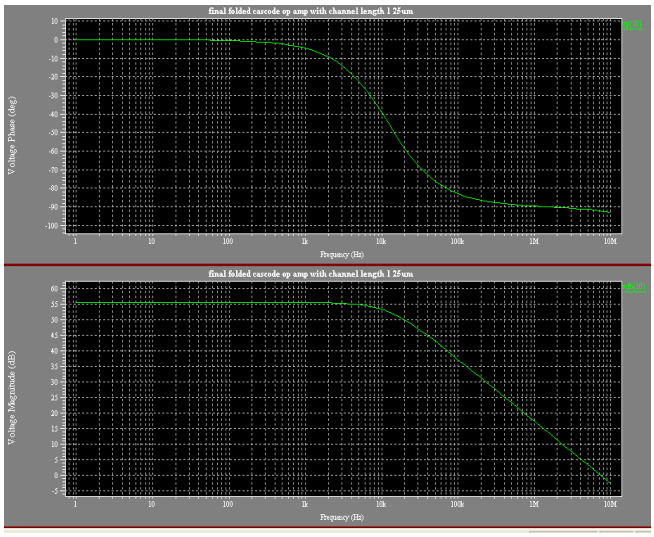


(1)

2. AC RESPONSE MEASUREMENT:

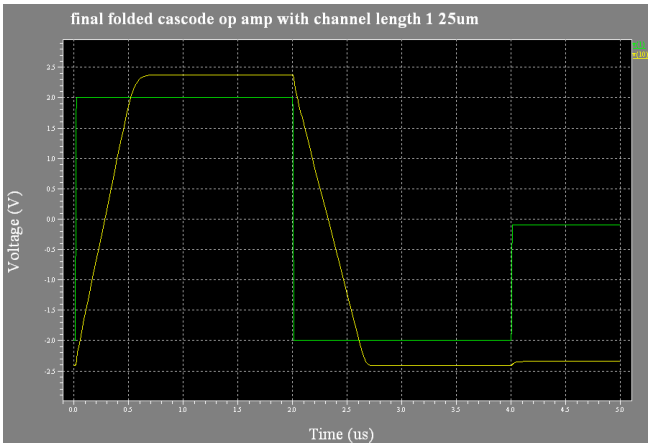


(2)

3. SLEW RATE MEASUREMENT:

The slew rate is calculated by changing the inputs of the op amp to pulsed, and measuring the slope at the differential output of the op amp. The slope of the output at the rising edge gives the positive slew rate of the amplifier, and the slope of the output at the falling edge gives the negative slew rate of the amplifier. The positive slew rate of the designed amplifier is 8.55 $V/\mu s$ and the negative slew rate is 6.72 $V/\mu s$

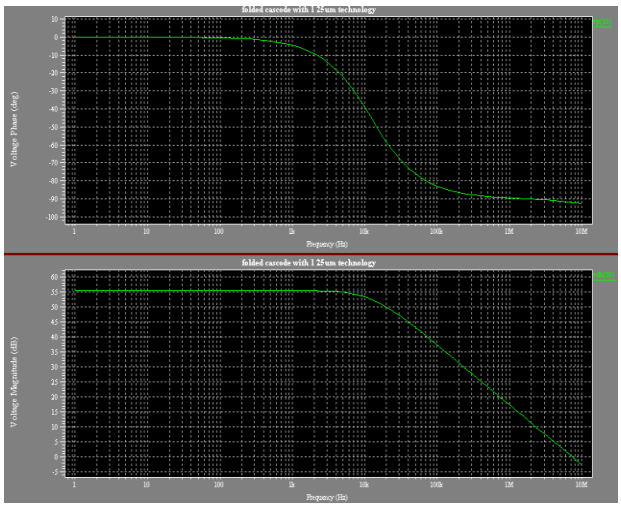
.



(3)

4. PSRR MEASUREMENT:

A small sinusoidal voltage is inserted in series with $V_{DD}(V_{SS})$ to measure PSRR+ (PSRR-). Here we are inserting a small ac voltage of 1V. We get PSRR of 55dB.



(4)

Figure 5.1 Simulated Waveforms of Folded Cascode Op Amp

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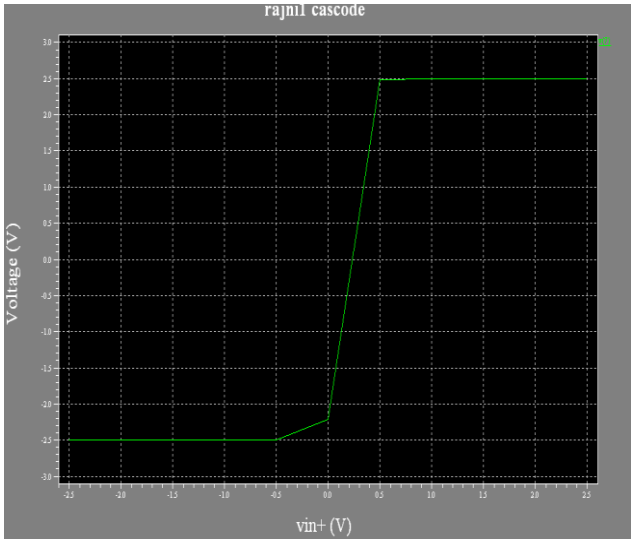
5.2 Simulated Results and Waveforms of Cascode Op-Amp

TABLE 5.5. RESULTS FOR THE TWO STAGE CASCODE OP-AMP

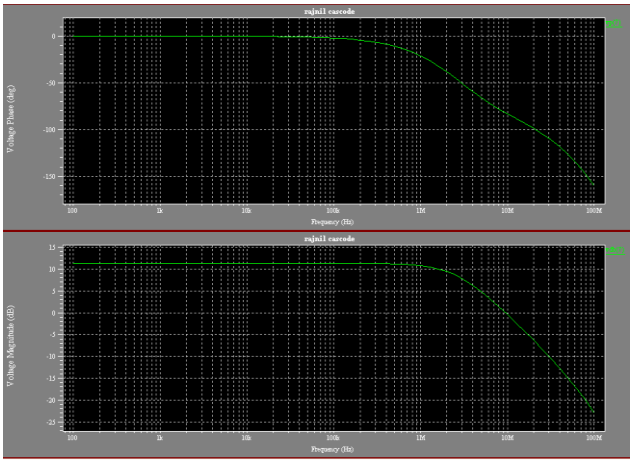
Sr.No.	Performance parameters	Specifications	Simulated Results
1.	Voltage Gain (V/V)	>5000 V/V	4800 V/V
2.	Unity Gain Bandwidth (MHz)	10 MHz	9.5 MHz
3.	ICMR (V)	-1.0V to +1.5V	-0.0 to 0.5V
4.	PSRR (dB)	60dB	25dB
5.	Output Swing (V)	$\pm$ 2V	-2.5V to +2.4V
6.	Slew Rate (V/us)	10 V/us	8.33V/us

1. INPUT COMMON MODE RANGE MEASUREMENT:



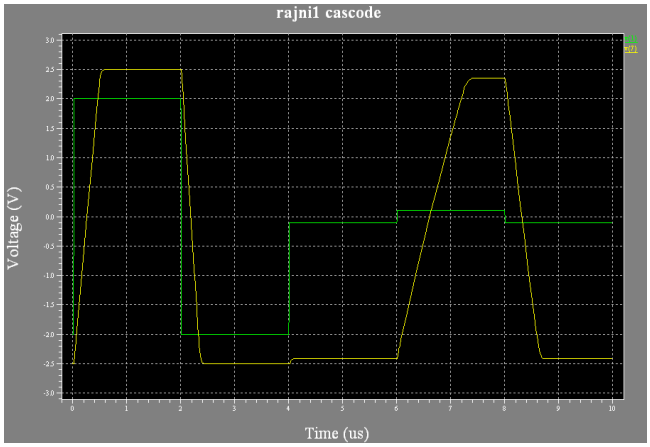
(1)

2. AC RESPONSE MEASUREMENT:



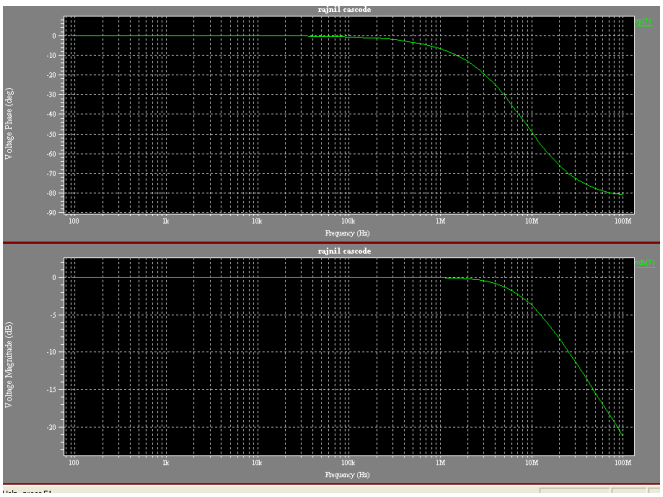
(2)

3. TRANSIENT RESPONSE MEASUREMENT:



(3)

4. PSRR MEASUREMENT:



(4)

Figure 5.1 Simulated Waveforms of Cascode Op Amp

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5.3 Comparison

The comparison of the design and simulations of the two-stage cascode and the folded cascode op amps can be sum up in the table below.

TABLE 5.3. COMPARISON RESULTS BETWEEN CASCODE AND FOLDED CASCODE OP-AMPS

S.No.	Parameter	Two-stage cascode op-amp	Folded cascode op-amp
1.	Voltage Gain	Low (4721 V/V)	High (6053V/V)
2.	ICMR	Low (-0.0 to 0.5V)	Very High (-1.0V to 2.5V)
3.	PSRR	Very Low (25dB)	High (60dB)
4.	Output Resistance	Low (8.5 $M\Omega$)	High (130 $M\Omega$)

6 CONCLUSION

This paper presents design analysis of the Folded-cascode amplifier using 1.25 µm CMOS technology. Initially our work describes the design of two-stage cascode op amp using the same i.e. 1.25 µm technology and then to overcome some of the limitations of the cascode op amp we have designed a high gain folded-cascode op amp which provides a high output resistance which leads to high gain as compared to a normal cascode circuit. The simulation of the cascode and folded cascode circuits is done using TSPICE simulation tool and the LEVEL–2, 1.25 µm parameters are used. A complete analysis of the circuit is presented in this thesis which shows how this circuit leads to a high gain and high resistance at output. A comparison between the cascode and Folded-Cascode op amps is described. We have also described their simulated and calculated results comparison individually. This paper provides a considerable insight into the overall operation and advantages of the folded-cascode circuit. This design overcomes various limitations and drawbacks of the various previously presented described architectures.

In this paper, a folded cascode op amp has been designed in $1.25\mu m$ CMOS technology. This op amp structure is used for many applications. Simulated results show that this op amp exhibits high DC gain, improved PSRR and ICMR and large output voltage swing. The typical values for DC gain is of the order of $6.035KV/V$, ICMR is of the order of -1.0V to 2.5V, PSRR is $\approx 55dB$, output swing is of the order of -2.3V to +2.0V, unity gain bandwidth of the order of 8MHz and slew-rate of $8.55V/\mu s$ have been obtained. Most difficult part in this design was optimization of NMOS and PMOS for proper operation and also finding different gains, currents in all the branches, resistances shown in circuits. But after careful analysis of simulation and designing at different points, the goal was achieved. The op amp fulfills all the other requirements with a good margin and has been simulated for worst cases.

Therefore the proposed folded cascode op amp exhibits the following advantages over the two-stage cascode op amps:

- Improved DC gain
- Improved ICMR
- Better PSRR

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