HDMI Made Easy: HDMI-to-VGA and VGA-to-HDMI Converters

By Witold Kaczurba and Brett Li

The consumer market has adopted High-Definition Multimedia Interface (HDMI®) technology in TVs, projectors, and other multimedia devices, making HDMI a globally recognized interface that will soon be required in all multimedia devices. Already popular in home entertainment, HDMI interfaces are becoming increasingly prevalent in portable devices and automotive infotainment systems.

Implementation of a standardized multimedia interface was driven by a highly competitive consumer market where time to market is a critical factor. In addition to improved market acceptance, using a standard interface greatly improves compatibility between projectors, DVD players, HDTVs, and other equipment produced by various manufacturers.

In some industrial applications, however, the transition from analog video to digital video is taking longer than in the consumer market, and many devices have not yet moved to the new digital approach of sending integrated video, audio, and data. These devices still use analog signaling as their only means of transmitting video, possibly due to specific requirements of a particular market or application. For example, some customers still prefer to use *video graphics array* (VGA) cables for projectors, while others use an *audio/video receiver* (AVR) or media box as a hub, connecting a single HDMI cable to the TV instead of a batch of unaesthetic cables, as outlined in Figure 1.

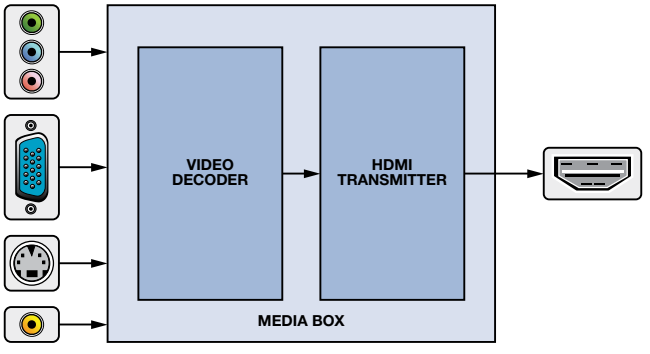

Figure 1. Media box converts analog signal to HDMI.

New adopters may see HDMI as a relatively complicated standard to implement, requiring a validated software driver, interoperability checks, and compliance testing to guarantee proper behavior of one device with various other devices. This might seem a bit overwhelming—as is often the case with new technology.

However, advanced silicon solutions are increasingly available to tackle the problem of implementation complexity, achieving improvement in both analog and digital domains; they include higher performance blocks to equalize poor differential signals and more complex algorithms to reduce software overhead and correct bit errors.

This article shows how advanced silicon solutions and smartly implemented software can facilitate HDMI implementation. Two basic devices—HDMI-to-VGA ("HDMI2VGA") and VGA-to-HDMI ("VGA2HDMI") converters—provide engineers familiar with video applications with an easy way to transition between analog video and digital video.

While HDMI has become a defacto interface for HD video, VGA is still the most common interface on a laptop. This article also shows how to interconnect these video technologies.

Introduction to HDMI Application and Video Standards

HDMI interfaces use *transition-minimized differential signaling* (TMDS) lines to carry video, audio, and data in the form of packets. In addition to these multimedia signals, the interface includes *display data channel* (DDC) signals for exchanging *extended display identification data* (EDID) and for *high-bandwidth digital content protection* (HDCP).

Additionally, HDMI interfaces can be equipped with *consumer electronics control* (CEC), *audio return channel* (ARC), and *home Ethernet channel* (HEC). Since these are not essential to the application described here, they are not discussed in this article.

EDID data comprises a 128-byte long (VESA—Video Equipment Standards Association) or 256-byte long (CEA-861—Consumer Electronics Association) data block that describes the video and (optionally) audio capabilities of the video receiver (*Rx*). EDID is read by a video *source* (player) from the video *sink* over DDC lines using an I^2C protocol. A video source must send the preferred or the best video mode supported and listed in EDID by a video sink. EDID may also contain information about the audio capabilities of the video sink and a list of the supported audio modes and their respective frequencies.

Both VGA and HDMI have the DDC connection to support the communication between source and sink. The first 128 bytes of EDID can be shared between VGA and HDMI. From the experience of the HDMI compliance test (CT) lab at Analog Devices, Inc. (ADI), the first 128 bytes of EDID are more prone to error, since some designers are not familiar with the strict requirements of the HDMI specification, and most articles focus on EDID extension blocks.

Table 1 shows the portion of the first 128 bytes of EDID that is prone to error. The CEA-861 specification can be referenced for details of the CEA extension block design that may follow the first 128 bytes of the EDID.

Table 1. EDID Basic Introduction

Address	Bytes	Description	Comments
00h	8	Header: (00 FF FF FF FF FF FF 00)h	Mandatory fixed block header
08h	10	Vendor and product identification	
08h	2	ID manufacturer name	Three compressed ASCII character code issued by Microsoft®
12h	2	EDID structure version and revision	
12h	1	Version number: 01h	Fixed
13h	1	Revision number: 03h	Fixed
18h	1	Feature support	Features such as power management and color type. Bit 1 should be set to 1.
36h	72	18 byte data blocks	
36h	18	Preferred timing mode	Indicates one supported timing that can produce best quality on-screen images. For most flat panels, the preferred timing mode is the native timing of panel.
48h	18	Detailed timing #2 or display descriptor	Indicates detailed timing, or can be used as display descriptor. Two words should be used as the display descriptor, one as the monitor range limit, and one as the monitor name. Detailed timing block should precede display descriptor block.
5Ah	18	Detailed timing #3 or display descriptor	
6Ch	18	Detailed timing #4 or display descriptor	
7Eh	1	Extension block count N	Number of 128-byte EDID extension blocks to follow.
7Fh	1	Checksum	1-byte sum of all 128 bytes in this EDID block shall equal zero.
80…		Block map or CEA extension	

The timing formats for VGA and HDMI are defined separately by the two standard-setting groups mentioned above: VESA and CEA/EIA. The VESA timing formats can be found in the VESA *Monitor Timing and Coordinate Video Timings Standard*; the HDMI timing formats are defined in *CEA-861*. The VESA timing format covers standards, such as VGA, XGA, SXGA, that are used mainly for PCs and laptops. CEA-861 describes the standards, such as 480p, 576p, 720p, and 1080p, that are used in TV and ED/HD displays. Among the timing formats, only one format, *640 × 480p @ 60 Hz*, is mandatory and common for both VESA and CEA-861 standards. Both PCs and TVs have to support this particular mode, so it is used in this example. Table 2 shows a comparison between commonly supported video standards. Detailed data can be found in the appropriate specifications.

Table 2. Most Popular VESA and CEA-861 Standards (p = progressive, i = interlaced)

VESA (Display Monitor Timing)	CEA-861
640 × 350p @ 85 MHz	720 × 576i @ 50 Hz
640 × 400p @ 85 Hz	720 × 576p @ 50/100 Hz
720 × 400p @ 85 Hz	640 × 480p @ 59.94/60 Hz
640 × 480p @ 60/72/75/85 Hz	720 × 480i @ 59.94/60 Hz
800 × 600p @ 56/60/72/75/85 Hz	720 × 480p @ 59.94/60/119.88/120 Hz
1024 × 768i @ 43 Hz	1280 × 720p @ 50/59.94/60/100/119.88/120 Hz
1024 × 768p @ 60/70/75/85 Hz	1920 × 1080i @ 50/59.94/60/100/200 Hz
1152 × 864p @ 75 Hz	1920 × 1080p @ 59.94/60 Hz
1280 × 960p @ 60/85 Hz	1440 × 480p @ 59.94/60 Hz
1280 × 1024p @ 60/75/85 Hz	1440 × 576p @ 50 Hz
1600×1200p@60/65/70/75/85Hz	720(1440) × 240p @ 59.94/60 Hz
1920 × 1440p @ 60/75 Hz	720(1440) × 288p @ 50 Hz

Brief Introduction to Application and Section Requirements

The key element of HDMI2VGA and VGA2HDMI converters is to ensure that the video source sends a signal conforming to proper video standards. This is done by providing a video source with the appropriate EDID content. Once received, the proper video standard can be converted to the final HDMI or VGA standard.

The functional block diagrams in Figure 2 and Figure 3 outline the respective processes of HDMI2VGA and VGA2HDMI conversion. The HDMI2VGA converter assumes that the HDMI Rx contains an internal EDID.

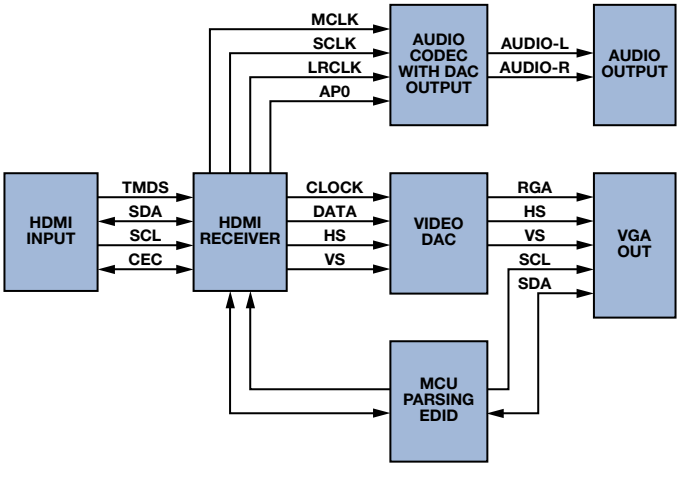

Figure 2. HDMI2VGA converter with audio extraction.

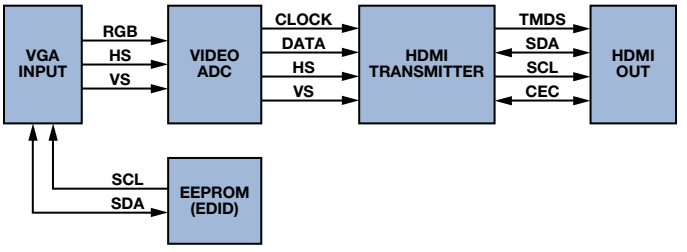

Figure 3. VGA2HDMI converter.

Theory of Operation

VGA2HDMI: a VGA source reads the EDID content from the sink to get the supported timing list using the DDC lines channel, and then the video source starts sending the video stream. The VGA cable has RGB signals and separate horizontal (HSYNC) and vertical (VSYNC) synchronization signals. The downstream VGA ADC locks to HSYNC to reproduce the sampling clock. The incoming sync signals are aligned to the clock by the VGA decoder.

The *data enable* (DE) signal indicates an active region of video. The VGA ADC does not output this signal, which is mandatory for HDMI signal encoding. The logic-high part of DE indicates the active pixels, or the visual part of the video signal. A logic-low on DE indicates the blanking period of the video signal.

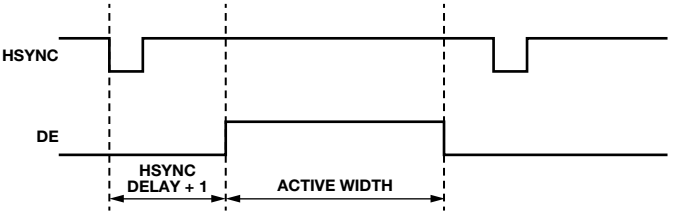

Figure 4. Horizontal DE generation.

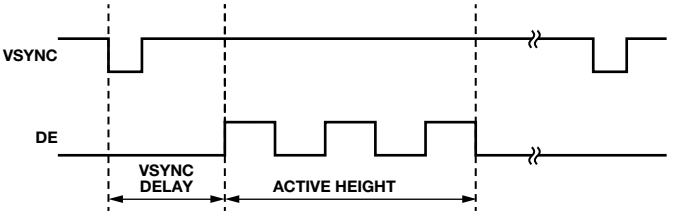

Figure 5. Vertical DE generation.

The DE signal is critical in order to produce a valid HDMI stream. The lack of a DE signal can be compensated for by the HDMI transmitter (Tx), which has the capability to regenerate DE. Modern HDMI transmitters can generate a DE signal from the HSYNC and VSYNC inputs using a few parameter settings, such as HSYNC delay, VSYNC delay, active width, and active height—as shown in Figure 4 and Figure 5—ensuring compatibility for HDMI signal transmission.

The HSYNC delay defines the number of pixels from the HSYNC leading edge to the DE leading edge. The VSYNC delay is the number of HSYNC pulses between the leading edge of VSYNC and DE. Active width indicates the number of active horizontal pixels, and active height is the number of lines of active video. The DE generation function can also be useful for display functions such as centering the active video area in the middle of the screen.

Display position adjustment is mandatory for VGA inputs. The first and last pixel of the digitized analog input signal must not coincide with or be close to any HSYNC or VSYNC pulses. The period when the DE signal is low (such as the vertical or horizontal blanking interval) is used for transmitting additional HDMI data and audio packets and, therefore, cannot be violated. The ADC sampling phase can cause this kind of misalignment. An active region misalignment may be suggested by a black stripe on the visual area of the screen. For a composite video broadcast signal (CVBS), this phenomenon can be corrected by overscanning by 5% to 10%.

VGA is designed to display the whole active region without eliminating any area. The picture is not overscanned, so the display position adjustment is important for VGA to HDMI conversion. In a best-case scenario, the black stripe can be automatically recognized, and the image can be automatically adjusted to the middle of the final screen—or manually adjusted according to the readback information. If the VGA ADC is connected to the back-end scaler, the active video can be properly realigned to the whole visible area.

However, using the scaler to fix an active video region misalignment increases the cost of the design and the associated risks. With a scaler and a video pattern, for example, a black area surrounding a small white box inside the active region could be recognized as a useless bar and removed. The white box would become a pure white background when the black area was removed. On the other hand, an image with half white and half black would result in distortion. Some prevention mechanism must be integrated to prevent this kind of incorrect detection.

Once the HDMI Tx locks and regenerates the DE signal, it starts sending the video stream to an HDMI sink, such as a TV. In the meantime, the on-board audio components, such as the audio codec, can also send the audio stream by I^2S, S/PDIF, or DSD to the HDMI Tx. One of the advantages of HDMI is that it can send video and audio at the same time.

When a VGA2HDMI conversion board powers up and the source and sink are connected, the MCU should read back the EDID content of the HDMI sink via the HDMI Tx DDC lines. The MCU should copy the first 128 bytes of EDID to the EEPROM for the VGA DDC channel with minor modification since the VGA DDC channel does not usually support the CEA extension used for HDMI. Table 3 provides a list of required modifications.

Table 3. List of Modifications Needed for a VGA2HDMI Converter

Modification	Reason
Change EDID 0x14[7] from 1 to 0	Indicates analog VGA input
Modify established timing, standard timing, preferred timing, and detailed timing	Timing beyond the maximum supported by the VGA converter and HDMI Tx must be changed to maximum timing or below
Set 0x7E to 00	No EDID extension block
Change 0x7F	Checksum has to be recalculated based on above changes

HDMI2VGA: the HDMI2VGA converter has to first provide proper EDID content to the HDMI source prior to receiving the desired 640 × 480p signal—or other standard commonly supported by the video source and display. An HDMI Rx usually stores the EDID content internally, handles the *hot plug detect* line (indicating that a display is connected), and receives, decodes, and interprets incoming video and audio streams.

Since the HDMI stream combines audio, video, and data, the HDMI Rx must also allow readback of auxiliary information such as color space, video standards, and audio mode. Most HDMI receivers adapt to the received stream, automatically converting any color space (YCbCr 4:4:4, YCbCr 4:2:2, RGB 4:4:4) to the RGB 4:4:4 color space required by the video DAC. Automatic *color space conversion* (CSC) ensures that the correct color space is sent to a backend device.

Once an incoming HDMI stream is processed and decoded to the desired standard, it is output via pixel bus lines to video DACs and audio codecs. The video DACs usually have RGB pixel bus and clock inputs without sync signals. HSYNC and VSYNC signals can be output through the buffer to the VGA output and finally to the monitor or other display.

An HDMI audio stream can carry various standards, such as L-PCM, DSD, DST, DTS, *high-bit-rate audio,* AC3, and other compressed bit streams. Most HDMI receivers do not have a problem extracting any audio standard, but the further processing might. Depending on the backend device, it may be preferable to use a simple standard rather than a complex one to allow easy conversion to the analog output for speakers. HDMI specifications ensure that all devices support at least 32 kHz, 44.1 kHz, and 48 kHz LPCM.

It is, thus, important to produce EDID that matches both the audio capability of the HDMI2VGA converter that extracts the audio and the original capabilities of the VGA display. This can be done by using a simple algorithm that retrieves EDID content from the VGA display via DDC lines. The readback data should be parsed and verified to ensure that the monitor does not allow higher frequencies than those supported by the HDMI Rx or video DAC (refer to Table 4). An EDID image can be extended with an additional CEA block that lists audio capabilities to reflect that the HDMI2VGA converter supports audio only in its linear PCM standard. The prepared EDID data containing all the blocks can, therefore, be provided to the HDMI source. The HDMI source should reread EDID from the converter after pulsing the *hot plug detect* line (part of the HDMI cabling).

A simple microcontroller or CPU can be used to control the whole circuit by reading the VGA EDID and programming the HDMI Rx and audio DAC/codec. Control of the video DACs is usually not required, as they do not feature control ports such as I^2C or SPI.

Table 4. List of Modifications Needed for an HDMI2VGA Converter

Modification	Reason
Change 0x14[7] from 0 to 1	Indicates digital input
Check standard timing information and modify if necessary (bytes 0x26 to 0x35)	Timing beyond the maximum supported by the converter and HDMI Rx must be changed to maximum timing or below
Check DTD (detailed timing descriptors) (bytes 0x36 to 0x47)	Timing beyond the maximum supported by the converter and HDMI Rx must be changed to maximum timing or below (to 640 × 480p, for example)
Set 0x7E to 1	One additional block must be added at end of EDID
Change 0x7F	Checksum must be recalculated from bytes 0 to 0x7E
Add extra CEA-861 block	
0x80 to 0xFF describing audio	Add CEA-861 block to indicate audio converter capabilities

Content Protection Considerations

Since typical analog VGA does not provide content protection, standalone converters should not allow for the decryption of content-protected data that would enable the end user to access raw digital data. On the other hand, if the circuit is integral to the

larger device, it can be used as long as it does not allow the user to access an unencrypted video stream.

Example Circuitry

An example VGA-to-HDMI board can use the AD9983A high-performance 8-bit display interface, which supports up to UXGA timing and RGB/YPbPr inputs, and the ADV7513 high-performance 165-MHz HDMI transmitter, which supports a 24-bit TTL input, 3D video, and variable input formats. It is quick and convenient to build up a VGA2HDMI converter using these devices. The ADV7513 also features a built-in DE generation block, so no external FPGA is required to generate the missing DE signal. The ADV7513 also has an embedded EDID processing block and can automatically read back the EDID information from the HDMI Rx or be forced to read back manually.

Similarly, building an HDMI2VGA converter is not overly complicated; a highly integrated video path can be built with the ADV7611 low-power, 165-MHz HDMI receiver and the ADV7125 triple, 8-bit, 330-MHz video DAC. The Rx comes with built-in internal EDID, circuitry for handling *hot plug assert*, an automatic CSC that can output RGB 4:4:4, regardless of the received color space, and a component processing block that allows for brightness and contrast adjustment, as well as sync signal realignment. An SSM2604 low-power audio codec allows the stereo I²S stream to be decoded and output with an arbitrary volume through the DAC. The audio codec does not require an external crystal, as the clock source can be taken from the ADV7611 MCLK line, and only a couple of writes are required for configuration.

A simple MCU, such as the ADuC7020 precision analog microcontroller with a built-in oscillator, can control the whole system, including EDID handling, color enhancement, and a simple user interface with buttons, sliders, and knobs.

Figure 6 and Figure 7 provide example schematics for the video digitizer (AD9983A) and HDMI Tx (ADV7513) essential for a VGA2HDMI converter. MCU circuitry is not included.

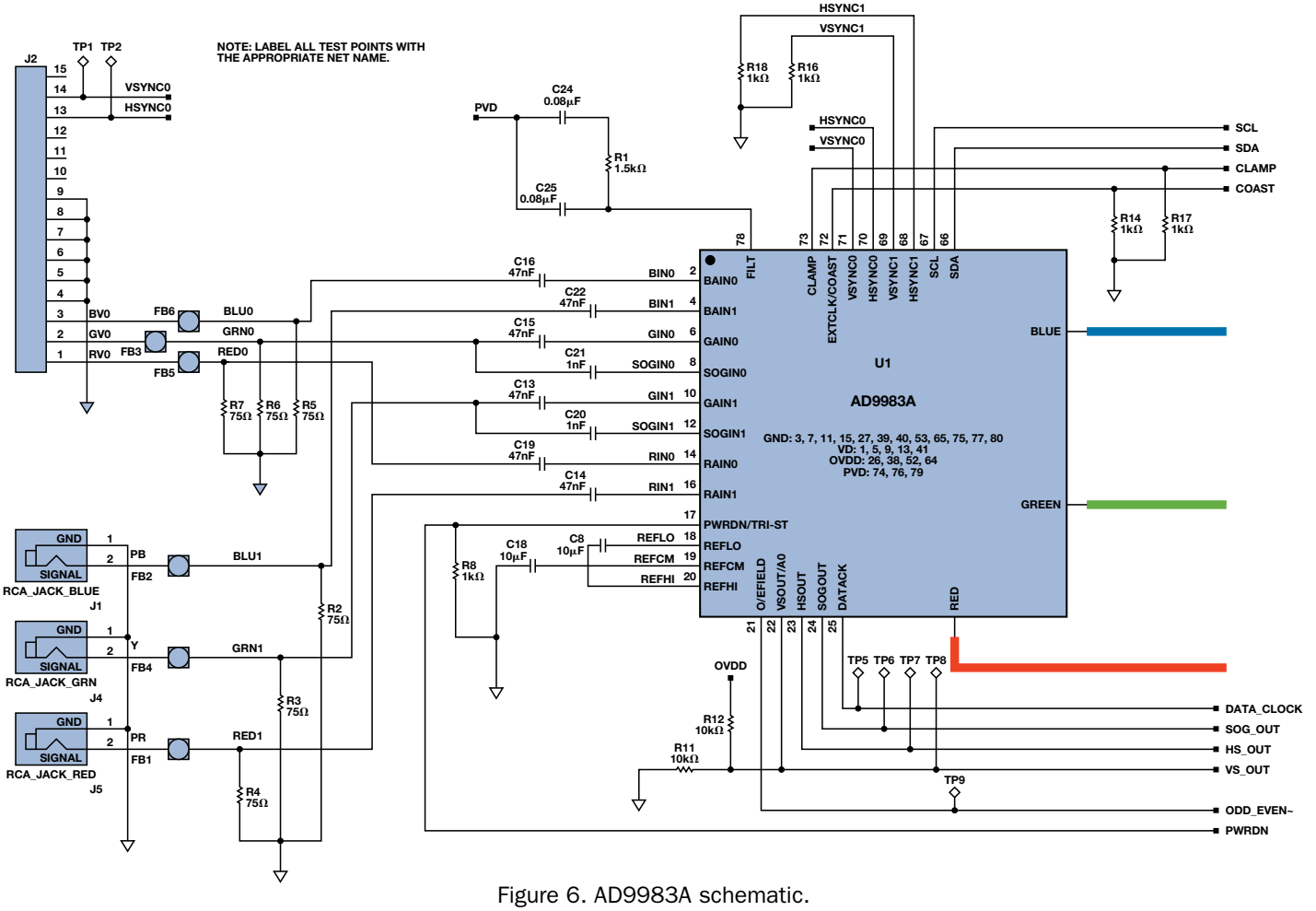

Figure 6. AD9983A schematic.

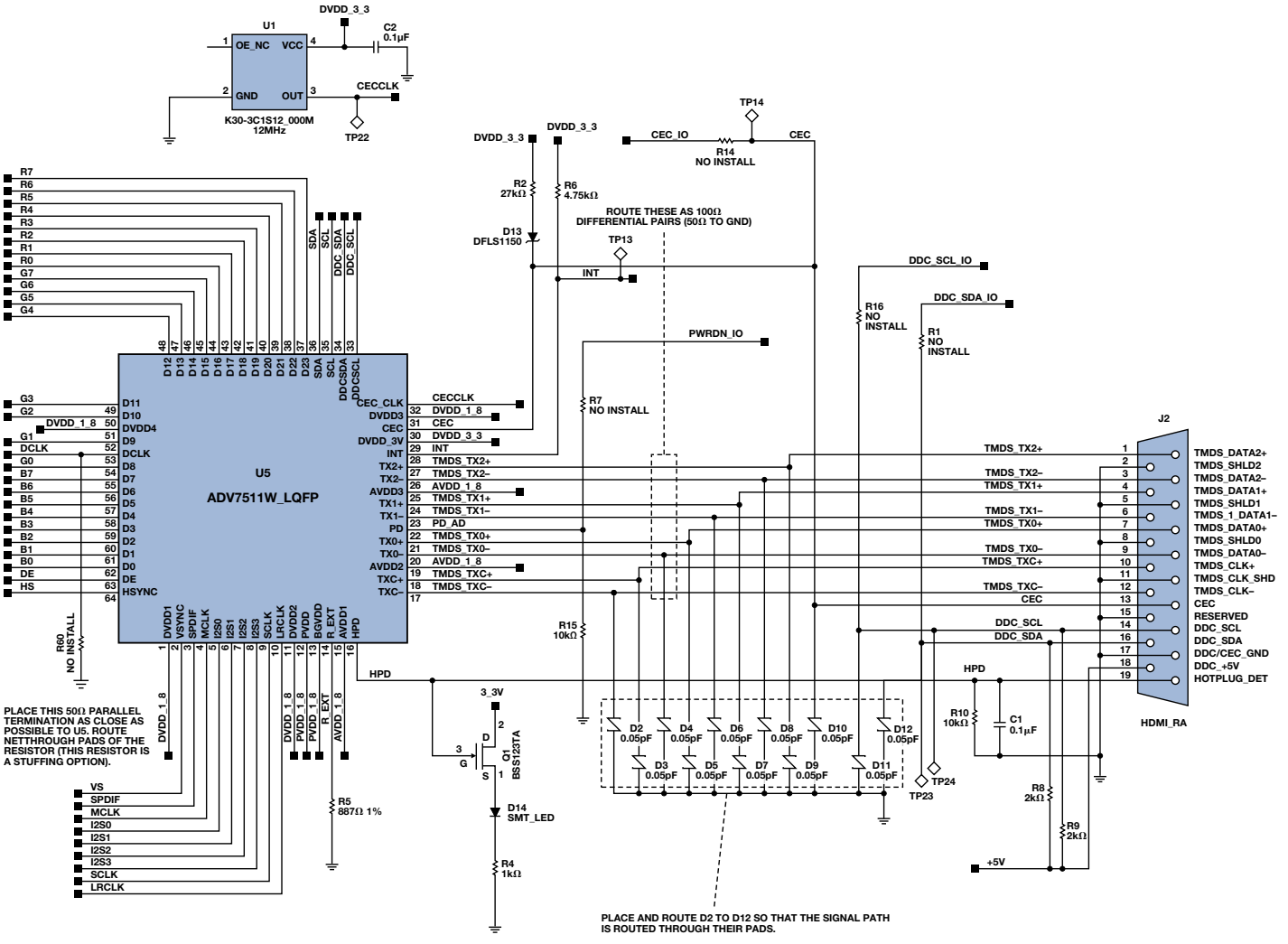

Figure 7. ADV7513 schematic.

Conclusion

Analog Devices audio, video, and microcontroller components can implement highly integrated HDMI2VGA or VGA2HDMI converters that can be powered with the small amount of power provided by a USB connector.

Both converters show that applications using HDMI technology are easy to apply with ADI components. HDMI system complexity increases for devices that are supposed to work in an HDMI repeater configuration, as this requires handling the HDCP protocol along with the whole HDMI tree. Neither converter uses an HDMI repeater configuration.

Applications such as video receivers (displays), video generators (sources), and video converters require a relatively small software stack and, therefore, can be implemented in a fast and easy way. For more details and schematics, refer to ADI's EngineerZone Web pages.

References

A DTV Profile for Uncompressed High Speed Digital Interfaces (CEA-861-E).

Display Monitor Timing (DMT), Coordinated Video Timings (CVT), and Enhanced Extended Display Identification Data (E-EDID) standards are available from VESA.

Authors

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