SID 1991

TESTING TFT-LCD SUBSTRATES WITH A TRANSFER ADMITTANCE METHOD

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Introduction

Presently, the yield of large-sized, active-matrix, thin-film-transistor, liquid crystal (TFT-LCD) substrates is very low. Faults are not precisely detected and located until these substrates are further processed to form completed panels which then can be tested visually. This means that much value is added to the high percentage of panels that eventually will be rejected, thus effectively throwing away millions of dollars. If panels could be adequately tested at the substrate level, this added value would not be wasted and, moreover, many bad panels could be repaired if their faults could be located and identified as to type.

Most manufacturers do some testing of substrates, usually simple dc resistance measurements which can detect only a few types of faults. They generally measure the gross characteristics of whole gate or drain lines or even whole panels, so that a fault, if detected, cannot be precisely located unless it can be found with a microscope.

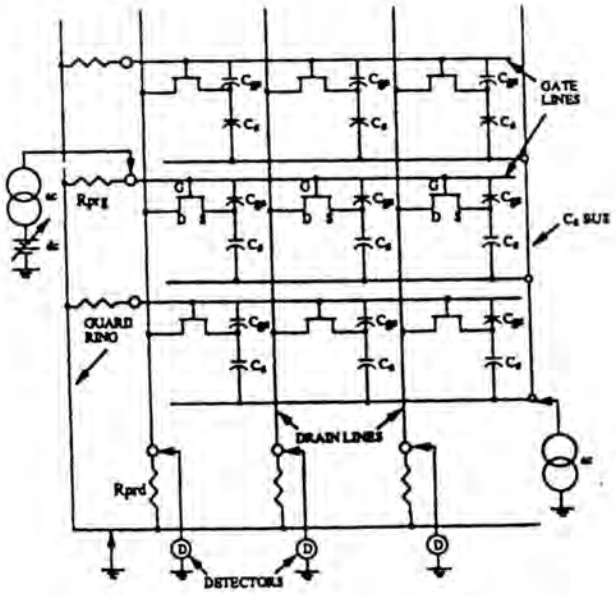
One method that does measure individual pixels has been described (see reference). This uses a broad-band pulse method that charges the capacitance of each pixel separately and measures the current discharged. This method is very fast and has certain advantages, but it appears that it may be susceptible to noise and therefore difficult to develop into a practical system.

This paper describes a technique of applying narrow-band, impedance measuring methods to solve this test problem.

The Transfer Admittance Method

A. Basic Method

The method is illustrated in figure 1 for the type of substrate that has storage capacitances, Cs, connected together by a separate bus. A combined ac test signal and dc bias voltage is applied to each gate (select) line and an ac signal to the common Cs bus. The resulting currents are measured simultaneously by detectors connected to many drain (data) lines. The transfer ratio is admittance whose phase components give conductance and capacitance. Two measurements are made; one with positive dc bias to turn on all the TFTs of one gate line, and a second with low or negative bias to hold these TFTs off. Thus we have four measured values for each pixel: Con, Gon, Coff and Goff.



BASIC TEST METHOD
FIGURE 1

All these are useful in separating faults as to type. The differences, ΔC = Con - Coff and ΔG = Gon - Goff, are the most useful for detecting faults because they vary only slightly over the area of a panel and, therefore, a slightly abnormal measured value indicates a circuit abnormality. For this type of pixel ΔC = Cs + Cgs if there are no other capacitances than those shown. The test connections are modified for other pixel circuits, and the value of ΔC may be different.

B. The Effect of Substrate Guard-Ring Parameters

Most bare substrates have a common guard ring that is connected to all the gate and drain lines through low-valued resistances. This guard-ring protects the TFTs on the substrate from high electrostatic voltages during manufacture and is then removed. The electrical parameters of this ring structure are critical to the speed and effectiveness of this method. Indeed, these parameters are critical to any non-instrusive method that isolates the effects of each pixel, including the method referenced. Particularly critical, for several reasons, are the values of the resistances between the line pads and the guard ring (Rprg and Rprd in figure 1). If these resistances are too low, they are hard to drive, they may burn out if a high dc bias voltage is used, and they cause increased measurement noise. This method also requires good probe contact resistance both to the connection pads on the gate and drain lines and to the guard ring itself. Low resistance along the guard-ring itself also improves the measurements.

Results and Discussion

A. Fault Detection Capability

A list of faults for substrates with a separate Cs bus is shown in table 1. This gives a simple measure of the ability to detect, locate and identify each fault and a note about their symptoms. Generally, only ΔC or ΔG is needed for detection. If the TFT is open (faults C or D) or is shorted drain to source (fault 3), there will be no ΔC change. A short from gate to source (fault 2) or across Cs (fault 13) will give a high ΔG, as shown in figure 2a. Other shorts (such as faults 1 and 4) give a high Gon and Goff. Note that most faults can be easily detected. Obviously, most faults that are detected can easily be located because the coordinates of the abnormal measurement are known. An open gate or drain line (fault A or B) affects many measurements, but is easily located as being just before the first pixel away from the source or detector that shows a low ΔC as shown in figure 2b.

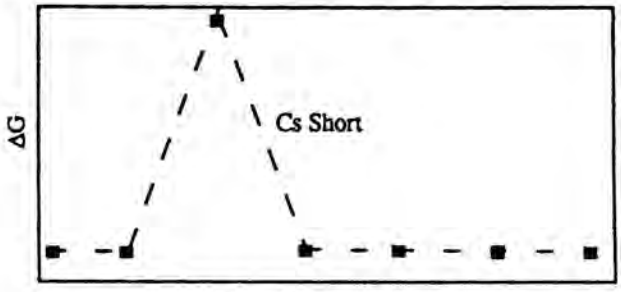


FIGURE 2A

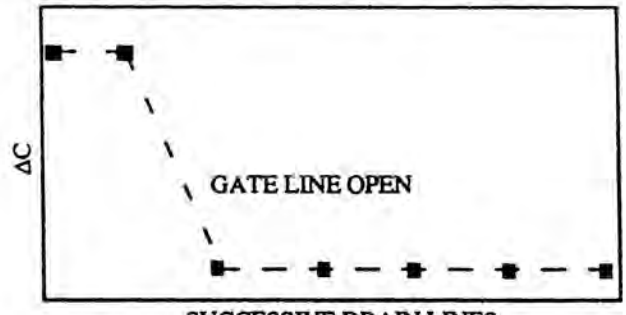


FIGURE 2B

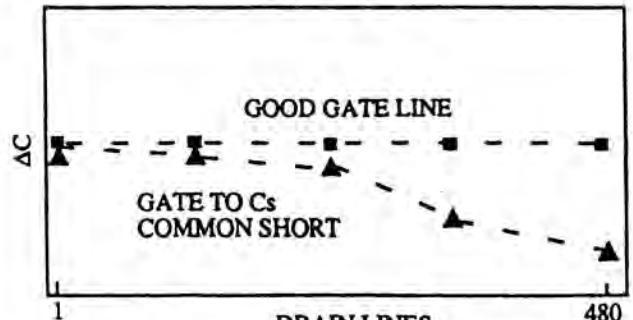


FIGURE 2C

Location of line-to-line shorts is more difficult because many measurements are affected. For example the Cs bus-to-gate line short (fault 15) measurements of figure 2c show a gradual decrease in ΔC which make it difficult to determine the exact location of the fault.

Fault identification is more complicated and often requires using Coff and Goff (or Con and Gon), as well as the differences. Some faults affect measurements on neighboring pixels and this data can help identification. For example, a short from the pixel electrode to the adjacent drain line (fault 8) will cause a high Coff when measuring the next pixel. Additional measurements are also useful. As an example, a Cgs short (fault 2) and a Cs short (fault 13) both give a high ΔG, but one can
distinguish between them by removing the ac signal from either the gate line or Cs bus input and making another measurement.

There are a few faults that this method cannot detect, but most of these could not be detected by any electrical means that does not make connections in the active substrate area. For example, a second open on a given gate line cannot be detected by any non-intrusive method. Analogously, only one of two parallel shorts would have an effect unless they were high resistance shorts. The list of faults has several pairs of shorts that cannot be separated because they are in parallel.

Theoretically, shorts between adjacent drain lines (fault 11) and between pixels across drain lines (fault 9) are not detectable with this method because it puts the shorted points at the same potential so that no current should flow between them. However, we have detected some of these faults because they caused detectable changes in pixel capacitances. Indeed, these faults must affect the pixel geometry and thus they must have some effect on the pixel capacitances.

All types of faults can be partial or "soft" faults. Opens can be almost open and shorts can be high resistance shorts. The two most common are TFTs that have high "on" resistance (fault 16) and leakage across the Cs capacitance (fault 17). The ability to detect these depends on how "soft" they are and on the measurement precision.

B. Pixel Characteristics

The measured capacitances of a pixel are useful as design and diagnostic tools because these capacitances are critical parameters. Moreover, changing the signal level allows one to make plots of ΔC and ΔG versus dc bias voltage which could be used to determine the TFT threshold and saturation voltages. A plot of the measured equivalent series conductance vs dc voltage of a good pixel is an approximate plot of the TFT conductance, but a more accurate plot of the TFT characteristic can be made if there is a Cs short. If the frequency is changed, the changes in the measured values for good pixels give a measure of line attenuation and phase shift and might be used to predict dynamic characteristics.

C. Precision and Speed

These measurements must be fast and yet they must be precise to see small changes in the very small pixel capacitances. The precision depends on speed. Difference measurements (ΔC and ΔG) made in 8ms gave standard deviations of about .002 pF and 100pS. This precision also depends on the resistance from line pad to test ring, which was about 500 ohms for these measurements. This precision is adequate for all actual shorts or opens but limits the precision to detect leakage resistances to a few gigaohms unless the measurement time is increased to give added precision.

System Configuration

A complete test system would combine a

signal sources, scanners and detectors, and a computer with appropriate software and peripherals. The prober might, for example, contact all of the 480 gate lines of a 10-inch diagonal panel simultaneously and 240 of the 1920 drain lines. It would step to make all the other drain line connections. Such a system should be able to test a good 10-inch panel in three or four minutes depending on the number of detectors used. If there are many faults, identifying and recording all of them would take extra time.

Conclusions

A test method for TFT-LCD substrates has been described that has shown that it can detect, locate and identify most of the many possible faults in a substrate, at high throughput speed and without intrusive connections that could damage the substrates themselves. This capability should make it possible to divide substrates into (1) those with no faults, (2) those with repairable faults and (3) those that are not repairable. This would avoid adding value to faulty substrates and also avoid wasting time trying to repair those that are difficult or impossible to repair.

Substrate design requirements for good testability were also discussed, particularly the design of guard rings and contacts. The recommendations given are important for all electrical test methods and should be seriously considered for all new designs.

Reference: "In-Process Testing of Thin-Film Transistor Arrays"
R. L. Wisnieff, L. Jenkins, R. J. Polastre and R. R. Troutman
1990 SID Symposium Digest paper 11.2, page 190.

Estimated Fault Detection Capability of
the Transfer Admittance Method
for Substrates with Cs Capacitances tied to a Common Bus

Codes for ability to:

Detect	Locate (if detect)	Identify (if detect)
Y Yes	Y Yes, to Pixel	Y Yes, to Type
P Probably	L To Line	P Probably
M Maybe	Q to Quarter of Line	T To One of Two Types
N No, Can't Detect	N No, Can't Locate	S To One of Several

Type	Where	Detect/Locate/Identify	Comment
OPENS			
A	Gate Line	Y/Y/Y	ΔC = 0 beyond open (from source)
B	Drain Line	Y/Y/Y	ΔC = 0 beyond open (from detector)
C	TFT-to-Drain-Line	Y/Y/T	ΔC = 0 one pixel only, see #7
D	TFT-to-Pixel (ITO)	Y/Y/P	ΔC small, Cgs, one pixel only
E	Cs line	Y/Y/Y	ΔC small, Cgs, beyond open line
SHORTS			
1	Gate line to Drn line	Y/Y/T	Very High Goff and Gon, see #4
2	TFT Gate to Source	Y/Y/T	High Gon, normal Goff, see #5
3	TFT Source to Drain	Y/Y/T	High Coff (by Cs + Cgs), ΔC=0, see #6
4	TFT Gate to Drain	Y/Y/T	Same effect as 1 (parallel effect)
5	Gate line to Pixel	Y/Y/T	Same effect as 3 (parallel effect)
6	Drain line to Pixel	Y/Y/T	Same effect as 3 (parallel effect)
7	Pix to Next Gate Line	Y/Y/T	Low ΔC, normal Coff, see C
8	Pix to Next Drn Line	Y/Y/P	Low Con, High Coff next DL
9	Pix to Pix, Across DL	M/Y/S	Detection depends on secondary effects
10	Pix to Pix, Across GL	Y/Y/P	High ΔC, Cgs + 2*Cs
11	Drain line to next DL	M/Y/S	Detection depends on secondary effects
12	Gate line to next GL	P/Q/T	Low ΔC, depends on DL. Nonlinear curve
13	Cs short	Y/Y/Y	High Gon, like 2 & 5. Put ac on Cs only
14	Cs line to Drain line	Y/L/Y	High Goff & Gon for all gate lines
15	Cs line to Gate line	P/Q/T	Low ΔC, depends on DL. Nonlinear curve
"SOFT" FAULTS			
16	Weak TFT (low G)	M/Y/Y	Low ΔC. Use Low dc to get bigger effect
17	Cs leakage resistance	M/Y/Y	Increased Gon, Detection depends on G

GL = Gate Line, DL = Drain Line, Pix = Pixel = Pixel electrode (ITO) area.
ΔC = Con - Coff ΔG = Gon - Goff