High performance current feedback amplifiers at your service

Dolly Wu, Ph.D. - September 06, 2016

Introduction

Current feedback amplifiers are one of the oldest amplifier topologies around. I remember the days when Comlinear ruled the market in the 80s with their high speed offerings. Analog Devices, Burr-Brown and Linear Technology later entered the fray as they grew their offerings. The following is another good treatment of these very useful, but kind of finicky, amplifiers especially for high speed application with "pathological slew rates." The author is Dolly Wu, a PhD, CalTech alumnus and former engineer at Analog Devices and Texas Instruments. Wu suggests that people typically design amplifiers with symmetrical nodes at the inputs of the amplifier. By taking various steps such as implementing current feedback amplifiers and making the input nodes asymmetrical, and properly reducing the capacitive loading on the feedback node really help to improve the bandwidth and to reduce distortion of the amplifier.

—EDN editor **Steve Taranovich**

The design topology

Figure 1 depicts a current feedback amplifier (CFA) having a pseudo-differential topology having two identical single-ended current feedback amplifiers (SCFA) connected in a non-inverting configuration. The CFA has high impedance inputs, allowing driving the amplifier without a transformer, which reduces costs, board space, and performance degradation due to the non-linearity of additional components in the signal path. The CFA is fabricated in a commercial, single 5V supply SiGE complementary bipolar process with a transistor transit frequency F_t of ~20 GHz. The wideband (optimized for ~150–200 MHz), high gain (20dB), low distortion CFA can be used in high speed buffers, filters, PGAs and VGAs. The CFA worked on first-silicon with test results, below. It appears to be easier to use and yield comparable or better results than a high performance voltage feedback amplifier made in the same process at that time (TI's THS4509).

The design and circuit layout are kept simple in order to reduce signal-dependent capacitance and parasitic effects that degrade bandwidth and linearity. Using two SCFAs with good matching achieves good CMRR, and is less likely to introduce undesirable distortion due to common mode problems. Since current feedback amplifiers tend to have higher slew rates than voltage feedback

amplifiers, this can lower distortion. Slew rate limitation can cause non-linear distortion to a signal when its frequency and amplitude are high and large enough.

The CFA has input signals Vp1 and Vp2 and differential outputs Out1 and Out2. Inputs Vp1 and Vp2 are fed to the high impedance non-inverting nodes of the two individual SCFAs; so, the outputs are non-inverting relative to the inputs. The CFA gain is set by the ratio of the resistors RF and RG, AG=1+RF/RG. To preserve stability, the gain is set =2 and can readily be set as high as 20–26dB and still yield overall high bandwidth and low distortion. According to the gain equation, only the ratio RF / RG matters, however the choice for the absolute values of the individual resistors is not arbitrary. As RF is reduced, the bandwidth increases but the margin for stability is sacrificed unless more frequency compensation is added. For CFAs, the maximum, theoretical, ideal bandwidth is BW=1/(2.×RF×CC) where CC is the frequency compensation capacitance internal to each SCFA. To ease use, the gain may be configured so a single gain resistor RG is set off chip, while RF is kept on-chip. An off-chip RG introduces package parasitic capacitances and inductances and degrades the performance of the amplifier, and generally reduces the stability of the amplifier. Some applications have fixed gain needs in which case both RF and RG may be on-chip.

The process technology is a bipolar transistor technology to provide a smaller chip and also reduce capacitances, compared with using a FET transistor process. Bipolar transistors generally have higher gain and better matching than FET transistors for the same physical layout size.

A single positive supply and ground are used to power the CFA. A quiet ground with dual, positive and negative supplies may yield better performance, but this is costly. Instead, for customer convenience, an on-chip mid-rail amplifier supplied by the single positive power is added in order to generate a quiet mid-supply voltage as a chip output reference voltage for the input signals, if the signals are AC coupled to the chip inputs. The mid-rail amplifier is also a current feedback amplifier, so that its variation with operating conditions would track that of the main CFA of **Figure 1**.

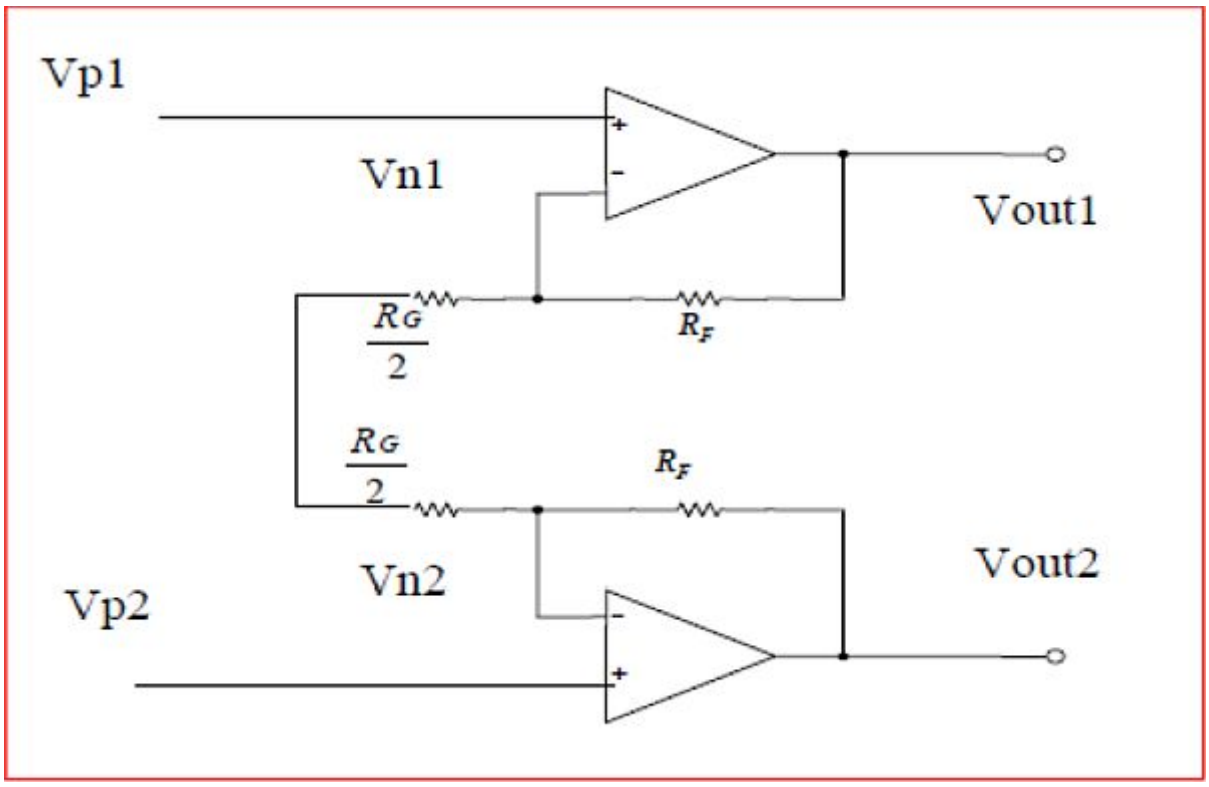

Figure 1 The pseudo-differential amplifier CFA with two identical single-ended current feedback amplifiers (SCFA).

Integrated circuit chip design

Integrated circuit chip design

The transistor level design of one of the SCFAs of **Figure 1** is shown in **Figure 2**. The SCFA has an input buffer stage, a transimpedance stage and an output buffer stage. Additional stages inserted before the final output stage proved to be beneficial in reducing distortion. Current transfer elements are used in the design to preserve speed; voltage transfer is avoided except in the use of emitter followers at the output, which inherently have very high bandwidth.

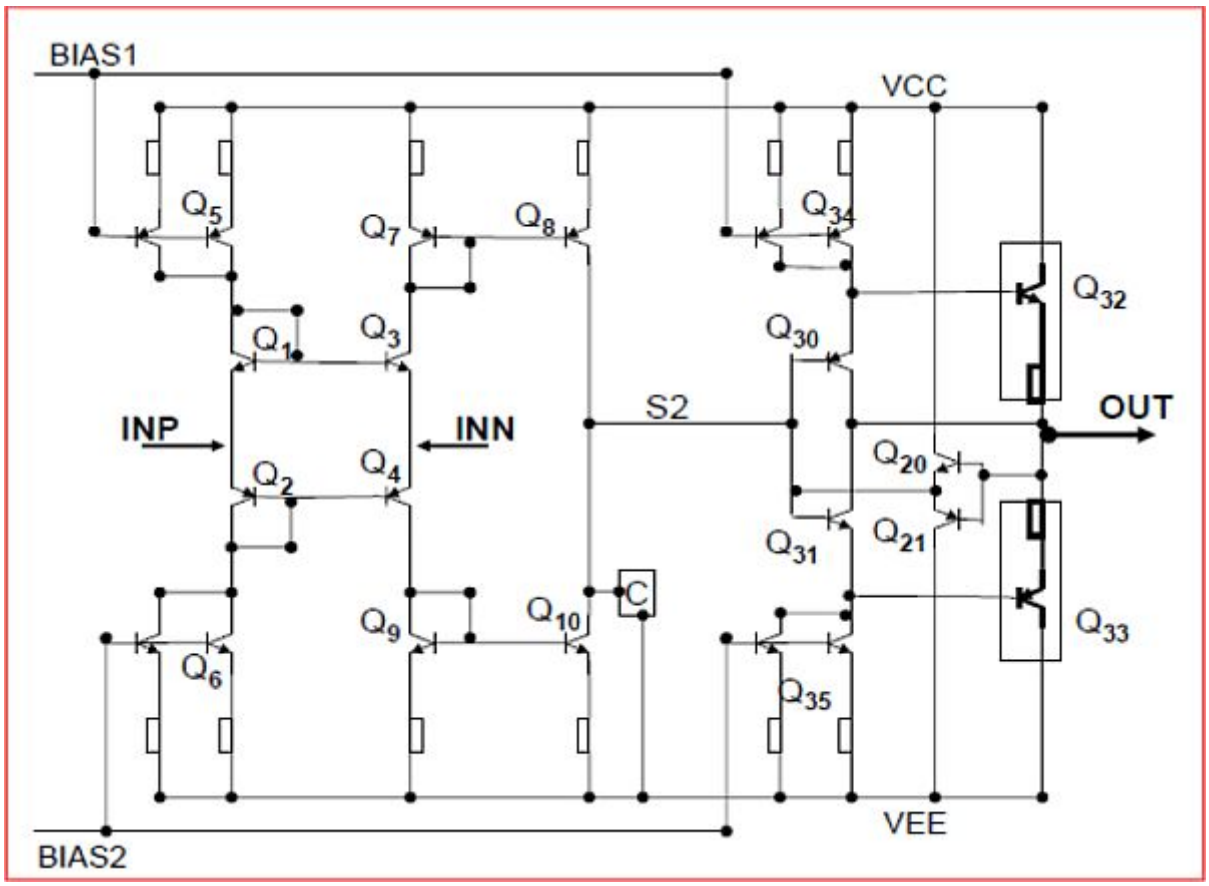

Figure 2 IC design of one of the SCFAs of Figure 1

Transistors Q1–Q4 form a current-mirror type input buffer receiving input signals VP and VN on the non-inverting and inverting nodes. A "current mirror" input buffer stage is used to reduce offsets because the transistor matching is better in this configuration than in a more often-used push-pull class A/B input buffer stage consisting of emitter followers. No further circuitry is added to correct the current mismatches, to avoid adding distortion.

One novelty of the design is to optimally size the input transistors relative to the feedback resistors. The SCFAs have separate feedback resistors RF but their gain resistors RG are coupled together. Although previous current-mirror input buffers have been symmetrical, here, the sizes of the transistors (Q3,Q4) connected to the feedback node VN, are made smaller by a factor of 2 to 3 than the corresponding ones (Q1,Q2) at the signal input node VP; so, there is a current reduction on the VN leg of the mirror. However, the sizes of (Q3,Q4) are still well above minimum feature sizes to avoid mismatch and electromigration. The size reduction of the feedback node VN transistors reduces distortion because PN junctions have capacitances that have a voltage dependent term that causes nonlinearity. Reducing the distortion is critical on the feedback node; the bandwidth is also increased with the reduction in parasitics. This reduces the overall capacitances seen at VN due to other elements, e.g. the number of feedback resistor interconnects.

The size of PNP transistors (Q2,Q4) are reduced relative to the NPN transistors (Q1,Q3) because the transistor gain for the two types of transistors is different. Also, the peak Ft and speed of the NPN

occurs at a lower current density than for PNP transistors. A different size is selected for each PNP than its corresponding NPN in all stages of the SCFA. The ratio of size difference should be 2x based on the difference in the Ft, but post-layout simulation is actually used to optimize the ratio of sizes.

The current output of the input buffer stage is mirrored by two complementary pairs of current mirrors, made up of transistors Q7-Q9 and Q9-Q10. The elements of the transimpedance stage in **Figure 2**, were set fairly small, with unity gain to preserve the bandwidth of the CFA. The outputs of the current mirrors are recombined at a common high impedance transimpedance node S2 where the inverting input node VN signal current is converted to a voltage. Amplification is provided by a transimpedance stage that senses a current IN, delivered at the inverting node VN to the external feedback network, and the amplifier produces an output voltage VOUT= z(jf)×IN where z(jf) is the transimpedance gain of the amplifier. A small frequency compensation capacitor C of ~200fF is placed at node S2.

This creates a single, dominant pole at node S2 for the CFA. The current through the total capacitance to ground at S2 is IN. With the feedback loop, any imbalance at the amplifier inputs will cause the input buffer to source (or sink) an imbalanced current IN, to the external network. This imbalance is passed by the mirrors to C, causing Vout to swing in the opposite direction until the original imbalance current is neutralized by the feedback loop. The voltage developed by the capacitance in response to IN is buffered to the output by the subsequent output buffer stage.

The output stage formed by transistors Q30-Q33 is a class AB push-pull output stage with local feedback. The transistor sizes are optimized “backwards,” from the output towards the input. Output transistors Q32-Q33 are selected to deliver a specified average current load to avoid electromigration; then the transistor size is increased beyond that minimum to avoid thermal distortion, but without creating so much parasitics to reduce the bandwidth. The stage prior to Q30-Q31 must be able to deliver sufficient average current to Q32-Q33. Continuing backwards, the currents in the current mirror legs are set up to provide a certain amount of impedance at S2.

Alternative designs of **Figures 3 and 4** include extra stages in the SCFA signal chain to gradually increase the signal gain and reduce the capacitance driven by a previous stage. The additional isolation between the output stage from the transimpedance stage may also reduce damage to the signal early on. These designs displayed lower distortion (e.g. reduced HD3 by ~6dB) based on simulations calibrated against test results of the SCFA of **Figure 2**. A set of small emitter followers (Q20,Q21) are inserted in **Figure 3**. The current mirror feeding node S2 now drives fewer emitter followers. To avoid supply head room issues, another set of emitter followers (Q22,Q23) are inserted to level shift the signal down.

Phase margin is reduced if the Q20-Q23 emitter followers are inserted; adding compensation is sometimes necessary such as at node S3, in addition to the usual compensation at the highest impedance node S2. Further improvement may be possible by “cascading” two input (current mirror) stages. The output of the second stage would be the high impedance collector output nodes

like in **Figure 2**. The voltage at the collector nodes may then be buffered up slowly by emitter followers.

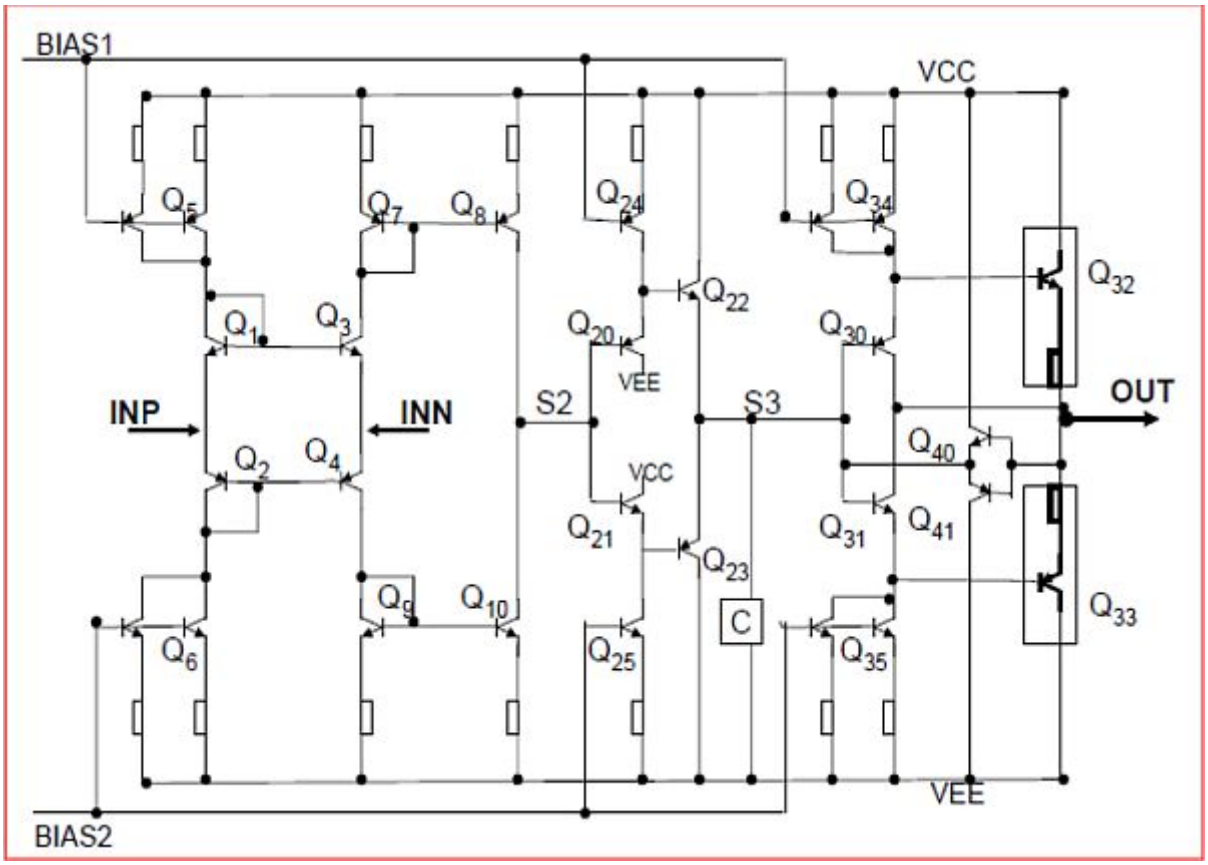

Figure 3 A version of the Figure 2 amplifier with an extra stages.

To reduce crossover distortion, the output stage elements (Q32, Q33) of **Figure 2** are sized large to reduce self-heating and to handle more current than an application would require so there is some class-A current always running through them. A small amount of resistor degeneration at the output also helps to reduce distortion. To reduce current consumption, the input of the class A/B driver (Q30,Q31) have their collectors tied together to VOUT rather than to the supply rails. An additional benefit of this local feedback is improved speed, by pre-setting the voltages at the input (Q30,Q31) and output (Q32,Q33) of this driver stage to be similar. An alternative local feedback and compensation, shown in **Figure 4**, was found to also work well compared to **Figure 3**.

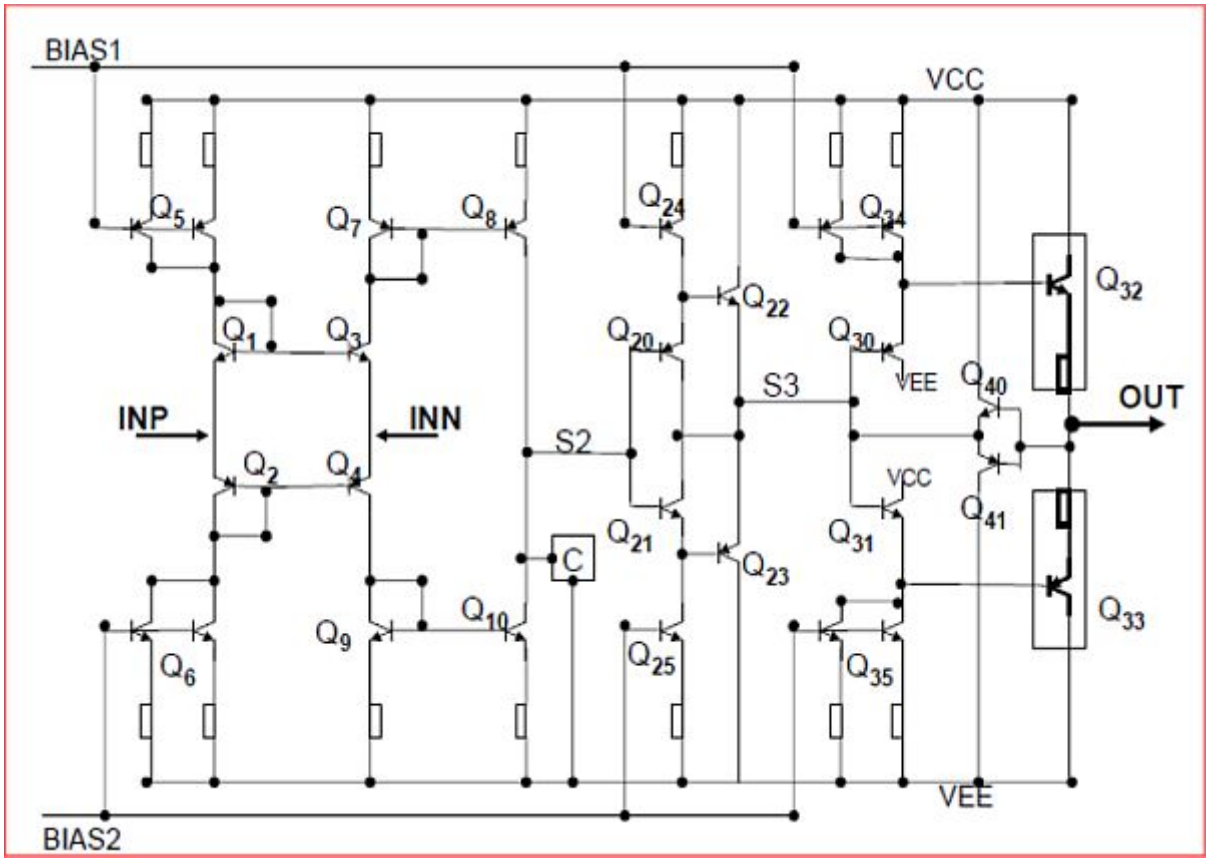

Figure 4 Another version of the Figure 3 amplifier.

Instead of tying the collectors of Q32-Q33 to the supplies, a current mirror may be inserted between Q32 and Vcc and also between Q33 and ground(VEE) and each mirror output is connected to VOUT. However, the current mirrors reduce the headroom at the output, preventing the circuit from working well on low supply voltages. If this current mirror local feedback is used at the output, it is better not to implement other local feedback loops simultaneously to avoid undesirable interference or instability.

SCFAs share the same current bias generator for better performance matching. Distortion in such peripheral circuits may introduce even order harmonic distortion in the CFA if the two SCFAs do not match. Odd order harmonics due to different sources may, by chance, cancel one another but this is hard to predict over frequency range.

Layout and packaging

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The chip layout (**Figure 5**) and packaging are critical to performance. A commercial compact QFN package with low electrical parasitics(short package legs) is used with a heat sink pad to maintain uniform temperature. The layout and choice of package pinout are as symmetrical as possible to reduce even order harmonic distortion. One SCFA layout is flipped or mirrored to create the CFA.

Multiple ground and power pins shield the signal path and used to reduce any ripple on the supply. A large amount of by-pass capacitors are placed on-chip, with sharp corners beveled, to dampen the effects of supply ripple and sources EMF distortion.

The on-chip capacitors are laid out offset from each other to avoid creating stresses on the die. These capacitors surround the SCFAs to buffer them from the die edges where stresses are largest. Current mirror circuit elements in the SCFA not carrying the signal are interleaved, ping-ponged from one SCFA to the other. The criss-crossing of the mirrors and metal busses reduces stresses created by long trenches on the die. The output stage is isolated from the rest of the SCFAs by large ground and power busses.

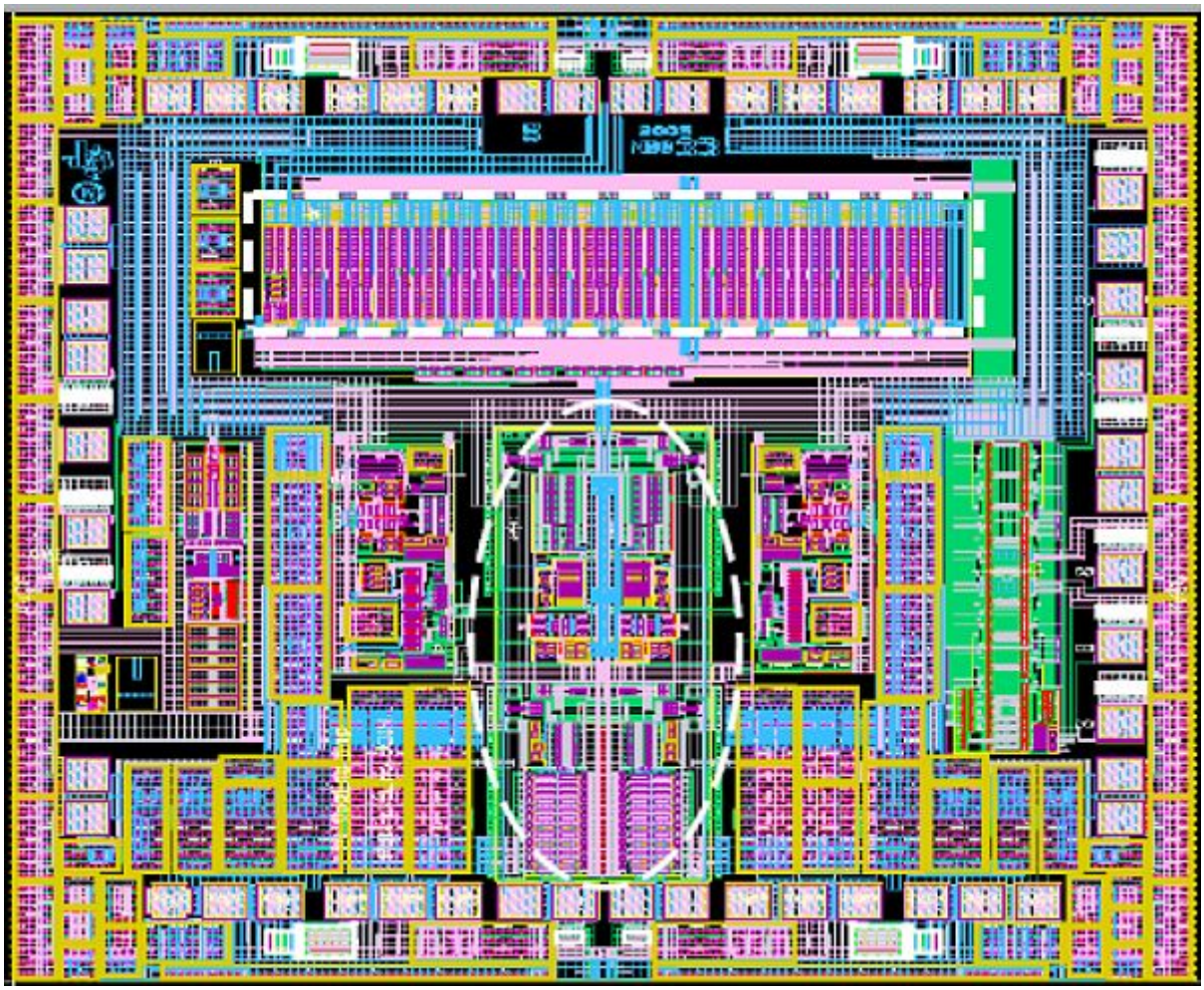

Figure 5 A layout of a PGA containing the CFA, circled. The rest of the layout includes a R-2R switch array for the PGA, digital control and biasing circuits.

The gain and feedback resistor segments of the CFA are matched by sizing them as wide as reasonable, placing many vias at the heads and dummy resistors on the ends of the array. A shield plane is underneath the entire set of resistors to reduce distortion. A current bias circuit is placed on one side of the CFA, with the mid-rail voltage reference buffer on the other side, which balances the heat from the current bias generator circuit. Sharing a single current bias generator allows both SCFAs to track each other better. Balanced layout symmetry reduces even-order harmonic

distortion. Simulation tools provided guidance to reduce odd-order harmonic distortion at particular frequencies, by adjusting the on-chip by-pass capacitors and the elements of the test board.

Test measurements

Tests were conducted using the circuits of **Figures 1 and 2** and test board of **Figure 6** with the output transformers in a parallel balun configuration. The input transformer is in isolation mode, turning a single ended input signal to differential. The two layer test boards have large areas devoted to ground and supply planes. The amplitude of the input differential signal was tuned to provide a 2Vpp signal at the output of the CFA with a 200O differential load (RLOAD) and 2pF capacitance, 5.2V power supply and 41mA current. The CFA voltage gain measured 20.9dB; small signal bandwidth of 690MHz with untrimmed cap; input referred noise of 1.9nV/RtHz. The slew rate measured ~4000V/us using 1V input steps.

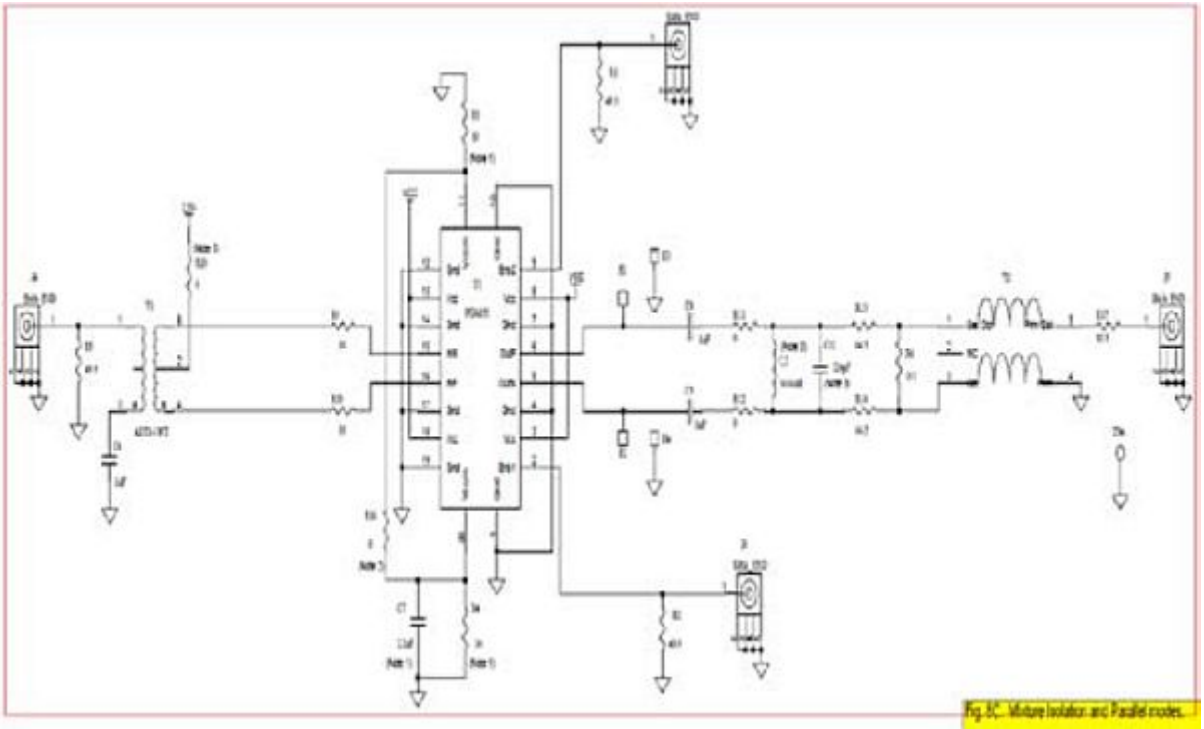

Figure 6 Test board circuit configuration used to test the CFA chips.

Different flavors of the chip layout were fabricated with different guard rings and on-chip symmetry. For a particular combination of the chip and PCB layout, the HD2 is better than -90dB even up to 200MHz and fairly flat across the frequency range. Although the HD2 for this combination is very good, the HD3 is worse than for other PCB configurations. The most desired combination of chip and board depends on application. The third order harmonic distortion(HD3) test results are -80 to -85dB for frequencies around 170 MHz suitable for mobile applications. The HD3 results improved as the supply voltage was increased from 5–6V. A higher supply voltage enabled more current to bias the amplifier which reduced the HD3 distortion to about -8dB. The third order intermodulation measured -85 to -83dB for an average two-tone frequency between 90–170MHz, and was measured

better than that of a voltage feedback amplifier (e.g.THS4509) for all frequencies between 10–250MHz for the same output RLOAD=500O on the amplifiers.

About the author

Dolly Wu received her BA from Columbia University and PhD from Caltech, both in physics. She worked as a circuit designer on data converters and amplifiers at Analog Devices and Texas Instruments. She is presently a patent lawyer (e.g. IP counsel at John Deere and Devlin Law Firm).

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