Identification of Faults on TFT–LCD Substrates Using Transfer Admittance Measurements

Henry Hall

300 Baker Ave, Concord, MA 01742–2174

Abstract

Identifying faults as to type on TFT–LCD substrates is necessary in order to determine if they can be repaired and to provide information to improve product quality. Fast fault detection and determining fault type requires different test strategies. Transfer admittance measuring techniques can be used effectively for both purposes.

No pass/fail test is made, instead the new data for each pixel are subjected to a series of tests that categorize those hard faults whose characteristics are easily detected. This is very fast because these tests are just numerical comparisons. Their order is important (see categories 1 to 5 in Table 1). The first tests are for gross shorts (large Goff and Δ G) because these can overload the detector giving meaningless Δ C values which would cause erroneous diagnostic decisions. These are followed by several tests of Δ C with the most easily detected faults first to reduce the possibility of erroneous classification.

Table 1
Simplified Identification Program (Preliminary)
when have Cs Bus and Redundant TFTs

```
1.  IF Goff Very High MEASURE Goff with Ecs = 0
      IF Goff high: GLDS or TGDS (in parallel)
      IF NOT: CBDLS
2.  IF Δ G Very High MEASURE Δ G with Ecs = 0
      IF Δ G high: TGSS or PGLS (in parallel)
      IF NOT: PCBS (Cs shorted)
3.  IF Δ C ~ 0 MEASURE Δ C of pixel to right
      IF Δ C = 0: Possible GLO
            VERIFY by testing more pixels.
      IF NOT MEASURE Δ C of adjacent up or down
            IF Δ C = 0: Possible DLO
                  VERIFY by measuring more pixels.
            IF NOT MEASURE with ac on Next Gate Line
                  IF Δ G high: PNGL
                  IF NOT MEASURE Coff above and below
                        IF Coff high: TDSS or PDLS (parallel)
                        IF NOT MEASURE Coff right and left
                              IF Coff high: PNDLS
                              IF NOT TDO or TGO (both TFTs open)
4.  IF Δ C ~ Cgs MEASURE Δ C left & right.
      IF Δ C ~ Cgs for both: CBO
      IF NOT: TSO (both TFTs open)
5.  IF Δ C High MEASURE Δ C above & below
      IF Δ C either high: PPVS

    [[Measure Pixel N Times and Average]]

6.  IF Δ Slightly Low Test Δ C Gs (series value)
      IF Δ Cs Low MEASURE Δ C with Ecs = 0
            IF Δ C high: RTDO (R = redundant)
            IF Δ C Normal: RTSO or WkTFT (Wk = weak)
            IF Δ C Low: MEASURE Goff
                  IF Goff high: TDSLk (Lk = leakage)
                  IF NOT: RTGO
      IF Δ Gs NOT low MEASURE Δ C left & right
            IF Δ C low: CBGLS
                  VERIFY by Measuring Δ C along gate line
            IF NOT: possible PPHS, continue program
7.  IF Δ G High MEASURE Δ G with Ecs = 0
      IF Δ G low: PCBLk (cs has leakage)
      IF NOT: TGSLk or PGLLk (parallel leakage)
8.  IF Goff High MEASURE Goff with Ecs = 0
      IF Goff High: GLDLLk, TGDLk or TDSLk
      IF NOT: CBDLk
```

The pixels that pass these first tests are those with soft faults, or with hard faults that are difficult to detect, and good pixels that failed the initial pass/fail test because of measurement imprecision. More precision is needed to separate out the good pixels and to identify the faults of the bad. Therefore the next step is to repeat the measurements several times and average the results, with the number of averaged can be chosen to optimize the trade-off between accuracy and speed. This improved data is then used to test for the final categories of faults.

Once categorized to a group of faults with similar data, more electrical tests are made to determine the specific fault type (see Table 1). In some cases only one more measurement is necessary to determine the specific fault type but usually more than one is needed. Often, an additional test is made after identification to verify the decision. These measurements take added time. We expect that it will usually take less than 100 ms to identify a fault in the first five categories and somewhat longer for the last categories depending on the number of measurements averaged (about 10 ms per measurement). If there are thousands of faults, this would add appreciably to the test time, but it would not be practical to repair such a poor substrate. The test program allows a maximum number of faults to be set and testing is aborted if this number is exceeded.

The type and location of all faults is stored and can be printed out or sent to a remote computer. This is necessary for the repair operation. The number of occurrences of each fault type is also listed for quality control purposes.

Some of the special tests made are listed below and in the test program of Table 1.

- Testing with one ac source removed.

Several categories use a test with ac only on the gate line because it distinguishes between shorts or leakage resistances to the gate line and those to the Cs bus. Thus this test is used when Goff or Δ G is high. Testing with ac only on the Cs bus would also distinguish between these faults and this test could be used for verification.

Testing with ac only on the gate line gives a better measurement of Cgs because Δ C = Cgs in this case, not Cgs + Cs. Thus, we want to use this test when we want to measure Cgs accurately to locate an open in a redundant TFT.

- Testing for Δ C = 0 in Adjacent Pixels

Testing the adjacent pixels, above, below, left and right, can distinguish line opens from