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P-Channel Dual JFETs Make High-Performance Complementary Input Stages Possible

Linear Systems

Lower Current Noise
Lower Bias Current Required

LSJ689

Application Note

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P-Channel Dual JFETs Make High-Performance Complementary Input Stages Possible

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Introduction

The dual monolithic P-channel LSJ689 is the complement to the N-channel LSK489. Both devices feature low offset, low noise and low capacitance. They enable the efficient implementation of fully complementary input stages without many of the device matching requirements when pairs of discrete devices are employed.

Used alone, the LSJ689 also enables the implementation of more traditional differential input stages in applications where P-channel devices are preferred.

Features of the LJ689 include:
- o Low noise on the order of 2 nV/√Hz
- o Low gate-drain capacitance, typically 3pF
- o Low gate leakage current typically 3pA (V_{ds} = 15V, I_d = 1mA)
- o Breakdown voltage of 50V
- o IDSS range of 5-20 mA
- o Typical transconductance of 3mS at I_d = 1mA

This note covers the full-complementary input stage application for the LSJ689 in combination with the LSK489.

Full-Complementary Topologies

Figure 1 shows a typical full complementary input stage connected to a second stage that acts in push-pull to sum the outputs of the top and bottom input pairs. This is an example of a popular topology made practical by the availability of the LSJ689. Net gain without feedback is set to 20dB. In most applications this arrangement would be used with negative feedback. Each long-tailed pair (LTP) is powered by a 2mA current source connected to the appropriate power rail. With their inputs connected in parallel, each pair produces signal output referred to its rail. This arrangement provides a simple way to drive a push-pull second stage.

The bias current in the second stage depends on the values of the tail current sources and load resistors R1 and R2. It is important that the currents in each pair be balanced for lowest distortion. Half the tail current should be flowing in R1 and R2 when the drop across these load resistors results in the desired second-stage bias current. This can be a bit of a juggling act. In Figure 1, the tail current is set to 2mA and the second stage bias current is set to 1mA. Variations in tail current and second stage V_{be} can upset the balance of the LTPs and/or the bias current of the second stage.
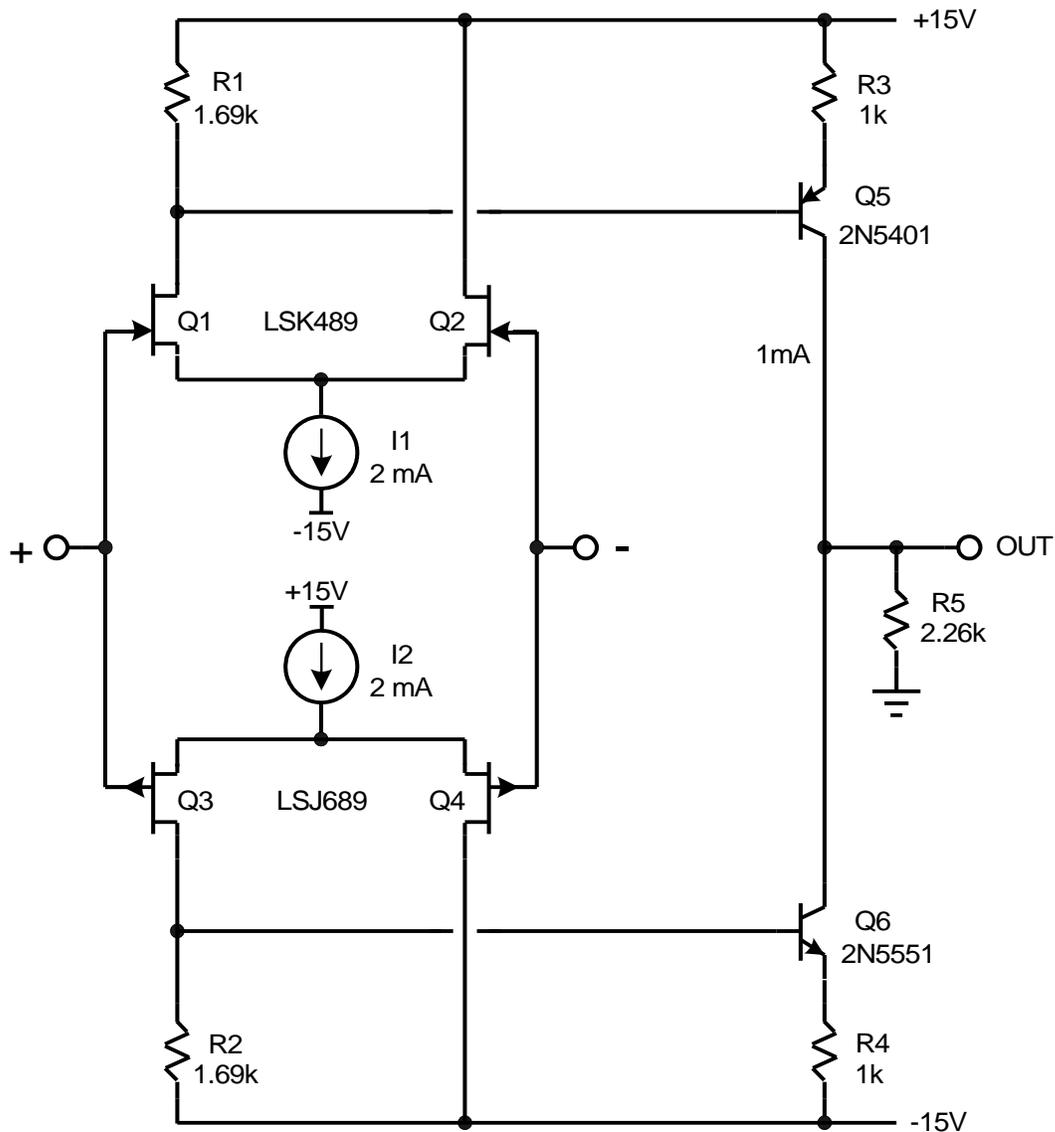
Figure 1: Full Complementary Input Stage with Push-Pull Second Stage

At the expense of 2 transistors, the second stage can be made differential and the biasing challenge can be mitigated. This is shown in Figure 2, where the gain is set to 40dB. The LTPs now more naturally operate with balanced drain currents and changes in the tail currents have a much smaller effect on second stage bias current. The second stage now produces a balanced output if both sets of collector nodes are used. Only one collector 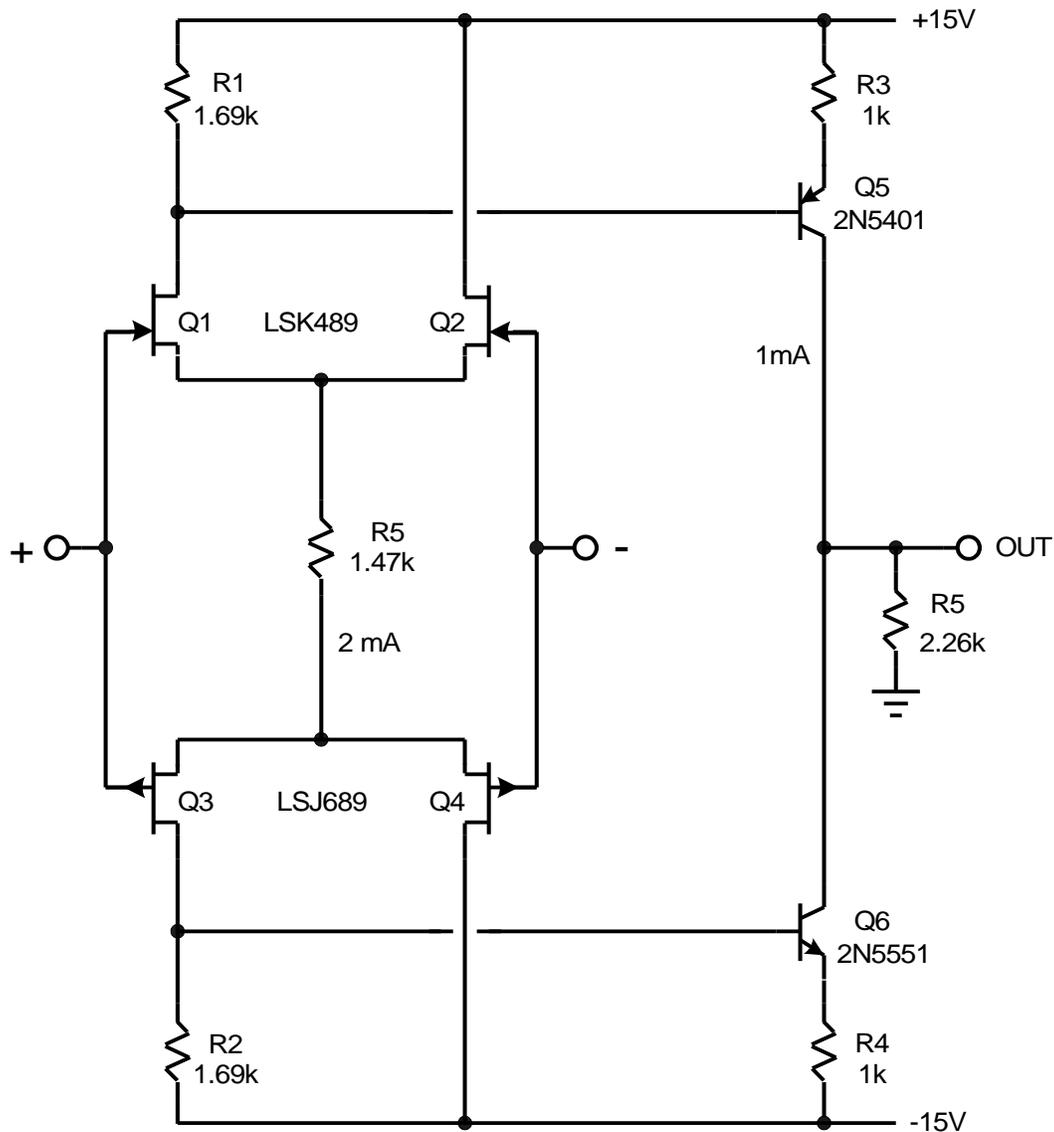node needs be used for a single-ended output. If a load resistor is tied between the collector nodes, a floating balanced output results. Note that the common-mode level is poorly defined absent a common-mode resistance to ground or some other means for establishing the common mode voltage. The differential output of this arrangement could be useful in a condenser microphone preamp, for example.
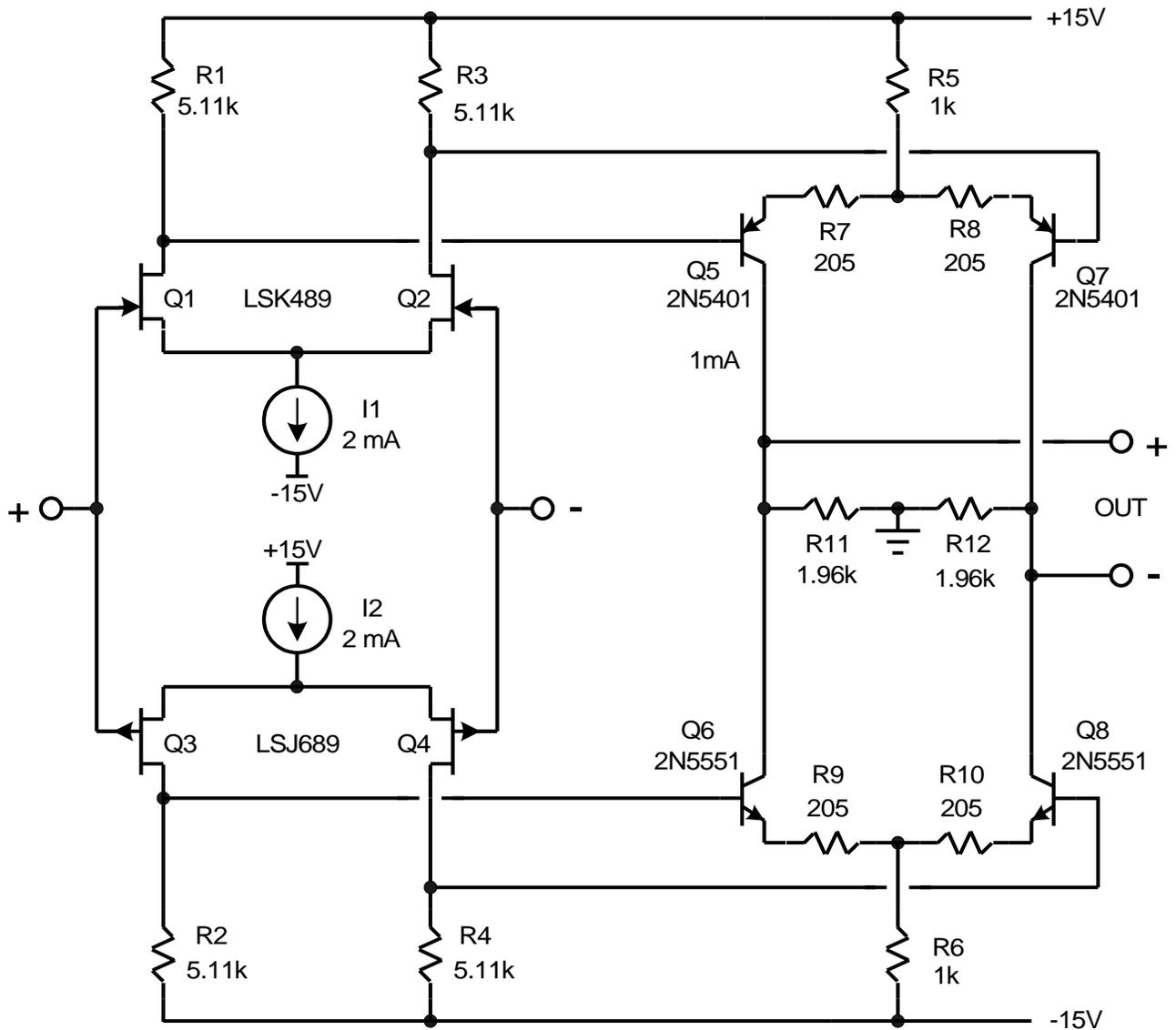
Figure 2: Complementary Input Stage Driving a Differential Second Stage

An elegant complementary JFET input stage popularized by John Curl floats the complementary differential pairs, as shown in Figure 3. This design takes advantage of the depletion mode biasing of the JFETs to create what is effectively a floating current source for the two pairs. The sum of the V_{gs} operating voltages of the top and bottom pairs appears across bias resistor R5, thus establishing the tail current. This design makes double-use of a single tail current, halving the operating current of the design of Figure 1.

R1
1.69k

R3
1k

Q5
2N5401

+15V

Q1 LSK489 Q2

1mA

R5
1.47k

+ ○

2 mA

- ○

OUT

R5
2.26k

Q3 LSJ689 Q4

Q6
2N5551

R2
1.69k

R4
1k

-15V

Figure 3: Floating Complementary Input Stage

The tail current in this design depends directly on the threshold voltages of the JFET pairs, so some selection or adjustment of R5 may be necessary to arrive at the desired tail current. Selection of N- and P-channel JFET pairs can be accomplished to first order by selecting devices by IDSS, since operating V_{gs} is dependent on IDSS. The potentially imprecise setting of the tail current in this design can exacerbate the challenge of keeping the LTP dc currents balanced and the second stage bias at the desired operating point. The differential second stage arrangement of Figure 2 can be especially helpful with the floating input stage.

DC Matching

In unipolar input stages (e.g., N-channel only), dc offset between the devices in the differential input pair can be tolerable, especially if a dc servo is used to manage output offset of the amplifier. However, differing dc offset in the N- and P-channel pairs of a full complementary input stage can cause the top and bottom stages to fight.

For this reason, the use of dual monolithic pairs is very desirable if selection for device matching is to be avoided. Simple binning by direction of offset in the monolithic pairs can further mitigate the effects of differing offset. For some monolithic pairs, there may be a systematic offset direction due to slight differences in mask layout.

Noise

The top and bottom input pairs each contribute signal to the output. When their outputs are summed, the output increases by 6dB. Because the noise from the top and bottom pairs is uncorrelated, the output noise goes up by only 3dB. A 3-dB SNR advantage thus results. This makes up for the 3-dB noise penalty incurred by using a differential input stage as opposed to a single-ended stage.

Unfortunately, the noise in an amplifier is not solely dependent on the noise of the input JFETs, but also includes noise from the load resistors and the second stage transistors. These other noise sources can be significant when the effective voltage gain of the first stage is not large. Input-referred noise in Figure 1 simulates at 3.3 nV/√Hz, but it would be only 2.5 nV/√Hz if noiseless resistors were used. Base shot noise in the second stage also contributes some noise. Making the second-stage transistors Darlingtons and increasing the value of the first stage load resistors accordingly decreases the input-referred noise to 2.8 nV/√Hz. Real-world noise levels will generally be a bit higher than in simulation due to JFET device imperfections.

The design of Figure 2 permits a larger voltage drop of 5V across the load resistors at the expense of output stage headroom. This increases the size of the load resistors and the effective voltage gain of the input stage, reducing noise. Input noise for Figure 2 is 2.3 nV/√Hz. If smaller resistors are used to allow only a 1.25V drop, headroom increases and noise rises to a still-respectable 2.6 nV/√Hz. Note that taking both sides

of an LTP output, as in Figure 2, does not necessarily reduce noise because the noise in these differential outputs is correlated.

Transconductance Differences

A key parameter for JFETs is transconductance at a given drain current. This number varies little over IDSS and threshold voltage in a given process, but it is generally different for P-channel and N-channel devices. Transconductance of a JFET increases as the square root of drain current. While the *gm* of the LSJ689 is about 3000μS at 1mA, that of the LSK489 is about 2500μS at 1mA.
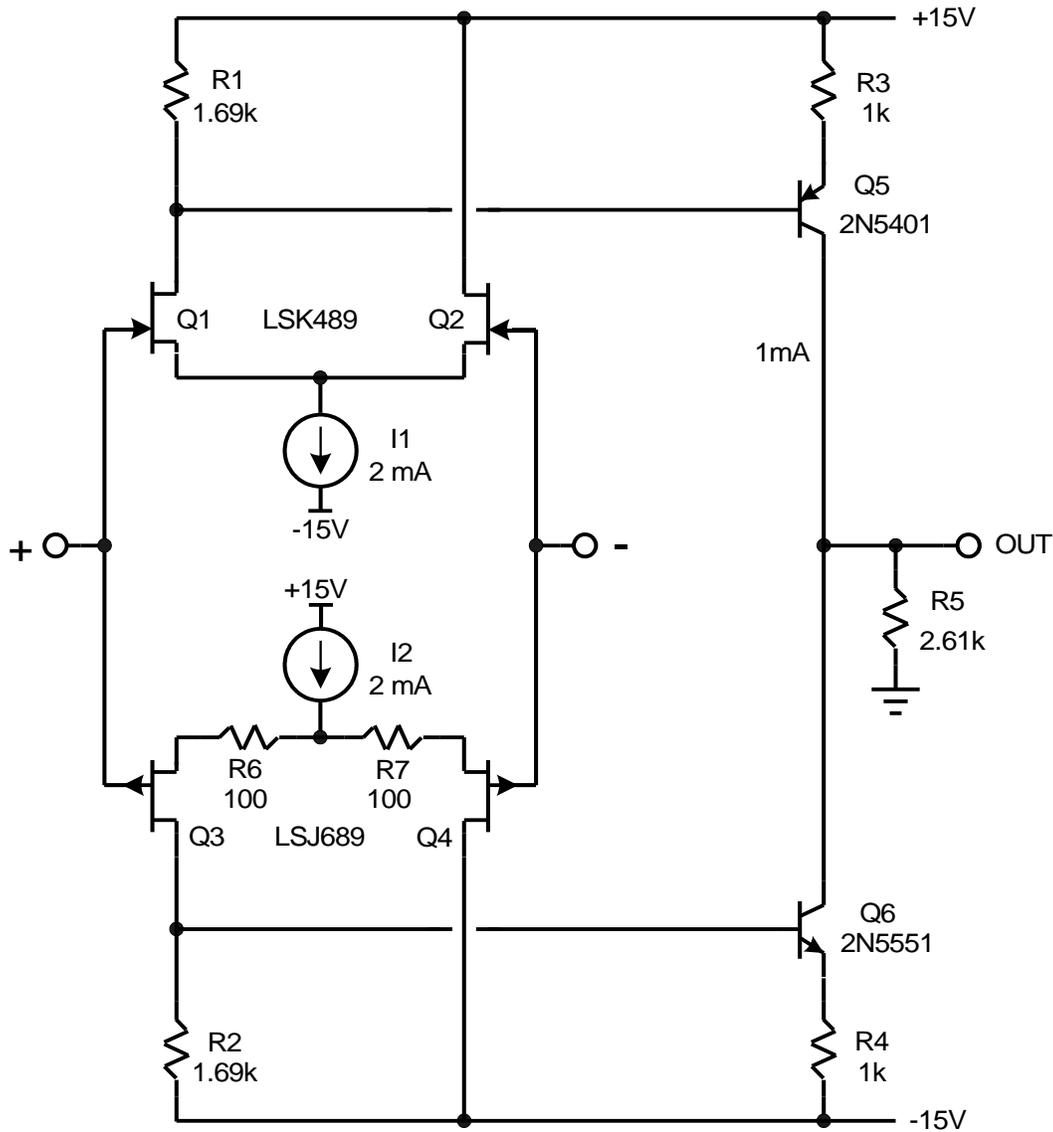
Figure 4: Use of Source Degeneration to Equalize Transconductances

Unequal transconductance of the top and bottom pairs in this input stage can compromise operation in some applications, such as where top and bottom Miller compensation is used in a feedback amplifier (shunt feedback amplifiers connected in parallel tend to fight). If desired, source degeneration resistances can be added to the P-channel pair to equalize *gm* of the top and bottom pairs. This is illustrated in Figure 4. This incurs a noise penalty of about 1dB. An alternative in the Miller compensation arrangement is to use a slightly smaller capacitor on the top side.

Gate Leakage Current

The fact that the leakage currents of the top and bottom pairs sums in opposition at the input is helpful, but the difference between the N- and P-channel JFET leakage currents may make the reduction in net leakage current fairly small.

If one could servo the net leakage current to zero, the very high-value gate return resistor in condenser microphone and similar applications (GΩ) might be avoided. It may be possible to accomplish this by manipulating the leakage current of the gate-substrate diodes that are integral to the dual monolithic devices. A bias voltage bootstrapped with the common mode signal could be applied to the substrate in devices where this connection is brought out (normally the common substrate is left floating). In critical applications where power dissipation and cost are less important, another approach would be to servo the leakage current of one device to a higher, optimum value, by using a dc servo to heat that device with a BJT attached to it.

Distortion and Input Capacitance

Although the symmetry of the full complementary input stage suggests lower distortion, this is not strictly the case. However, its ability to conveniently drive a push-pull second stage can contribute to lower distortion by reducing second harmonic distortion in the second stage. For high-impedance inputs, second harmonic distortion caused by the common-mode nonlinearity of the JFET junction capacitance will be reduced. As the common mode voltage goes positive, the N-channel drain-gate capacitance increases, while the P-channel drain-gate capacitance decreases. Both the LSJ689 and the LSK489 feature low input capacitance, making them especially suitable for applications where source impedance is high, such as in condenser microphones.

Conclusion

The availability of the P-channel LSJ689 opens up additional options for designers in applications where the matching provided by dual monolithic devices is important. The combination of low noise and low capacitance makes the LSJ689 especially attractive.