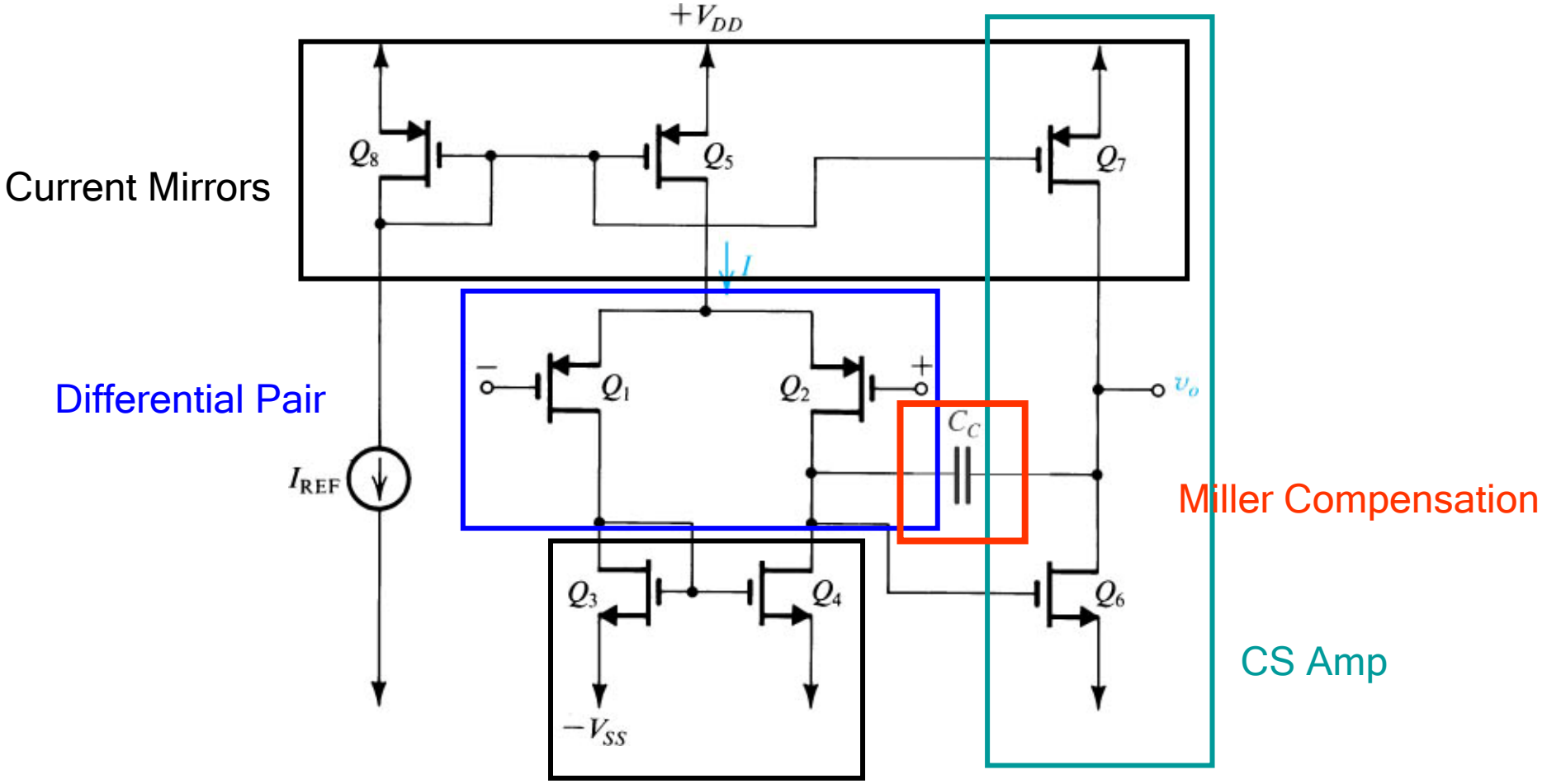
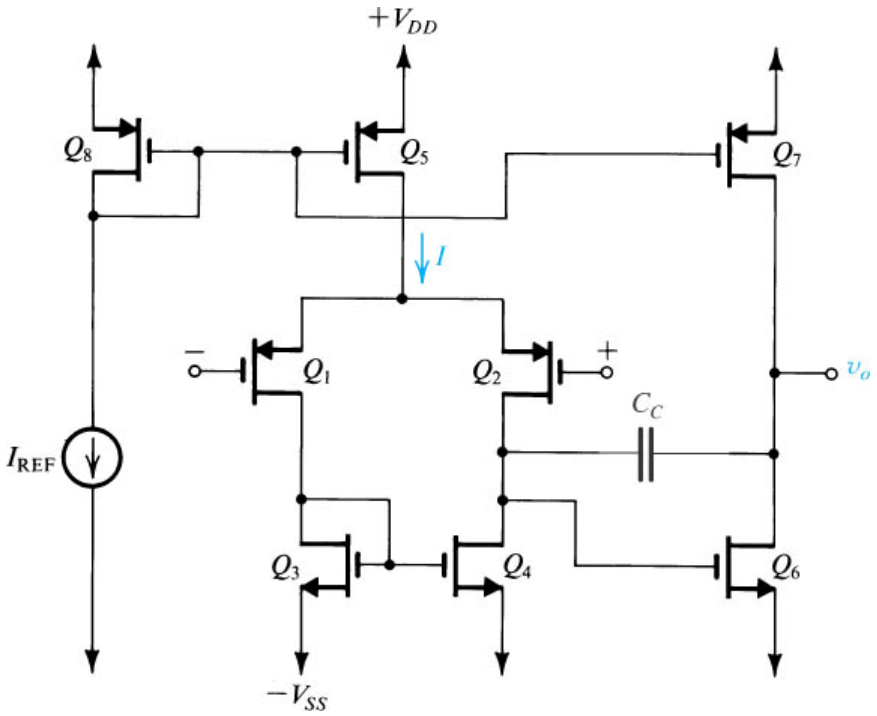
Lect. 12: Two-Stage OTA (S&S 9.1)



OTA: Operational Transconductance Amplifier ➔ High Output Impedance

Lect. 12: Two-Stage OTA



Input Offset

Make it as symmetric as possible!

$I_3 = I_4 = I/2$

$$V_{GS3} \sim V_{GS4} \sim V_{GS6}$$

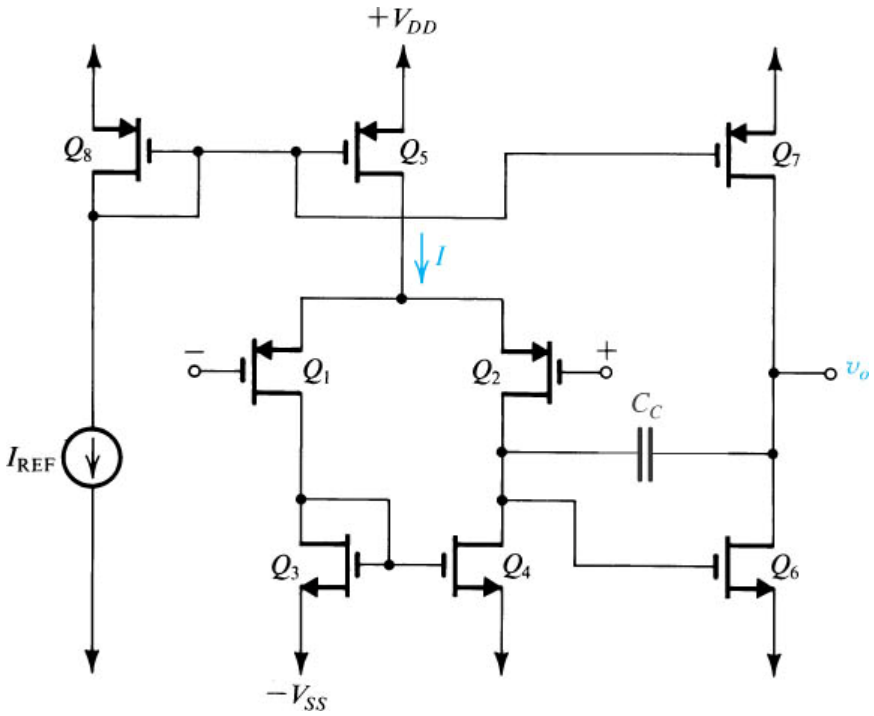
$$\frac{I/2}{(W/L)_4} \simeq \frac{I_6}{(W/L)_6}$$

$$\text{Since } I_6 = I_7 = \frac{(W/L)_7}{(W/L)_5} I,$$

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

Additional asymmetric factors due to fabrication

Lect. 12: Two-Stage OTA



Large I ➔ Large V_{SG5}, V_{SG1}, V_{GS3}

➔ Small input CM range

Input Common-Mode Range

Q_1, Q_2 should be in saturation

$$V_{SD1} > V_{SG1} - |V_{tp}|$$

$$V_{S1} - V_{D1} > V_{S1} - V_{ICM} - |V_{tp}|$$

$$V_{ICM} > V_{D1} - |V_{tp}|$$

$$V_{ICM,min} = -V_{ss} + V_{GS3} - |V_{tp}|$$

Q_5 should be in saturation

$$V_{SD5} > V_{SG5} - |V_{tp}|$$

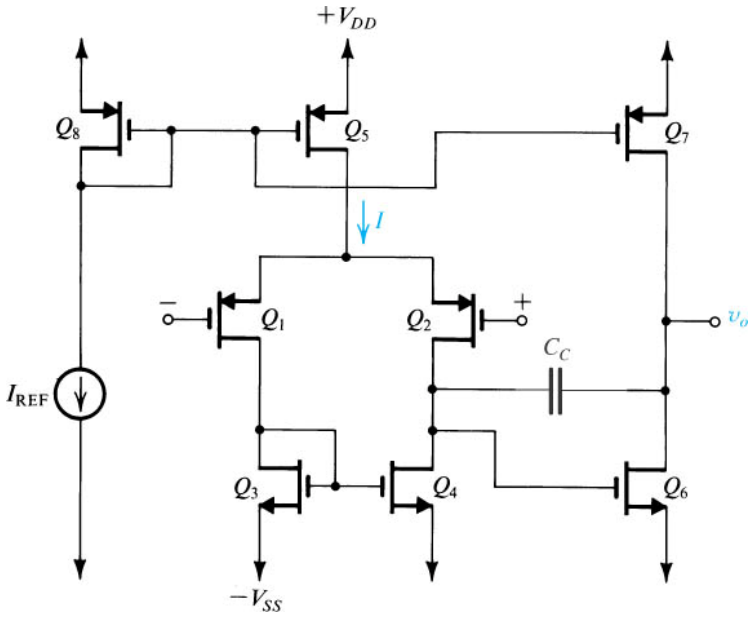
$$V_{S5} - V_{D5} > V_{S5} - V_{G5} - |V_{tp}|$$

$$V_{D5} < V_{G5} + |V_{tp}| = V_{DD} - V_{SG5} + |V_{tp}|$$

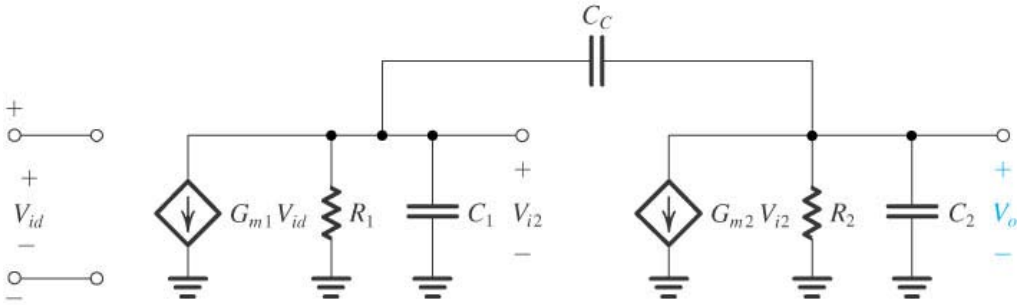
$$V_{ICM} + V_{SG1} < V_{DD} - V_{SG5} + |V_{tp}|$$

$$V_{ICM,max} = V_{DD} - V_{SG5} - V_{SG1} + |V_{tp}|$$

Lect. 12: Two-Stage OTA



Small Signal Model



Voltage Gain (DC)

Two CS amps in cascade

$G_{m1} = g_{m1} = g_{m2}$ (Ignoring Body Effect)

$R_1 = r_{o2} // r_{04}$

$A_{v1} = -g_{m2} (r_{02} // r_{o4})$

$G_{m2} = g_{m6}$

$R_2 = r_{o6} // r_{o7}$

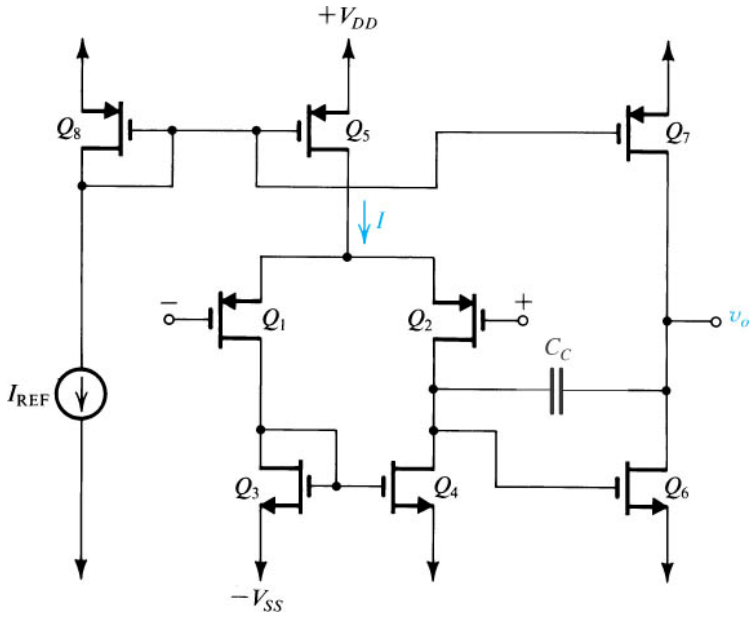
$A_{v2} = - g_{m6} (r_{o6} // r_{o7})$

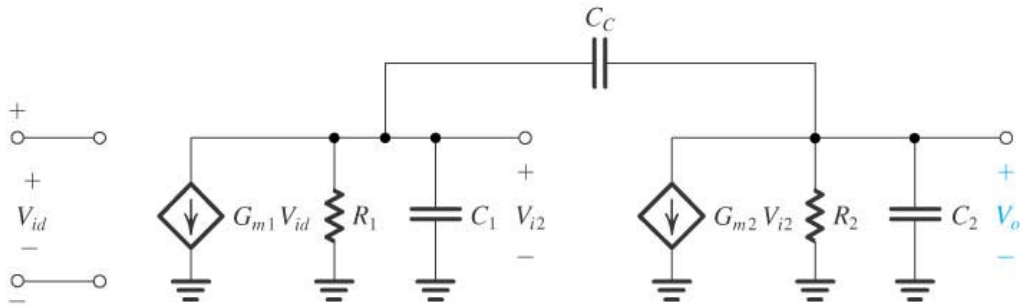
$A_v = g_{m2}\, g_{m6}\, (r_{o2} // r_{o4})\, (r_{o5} // r_{o7})$

R_{in}: infinity

R_{out}: $r_{o6} // r_{o7}$

Lect. 12: Two-Stage OTA





Frequency Response

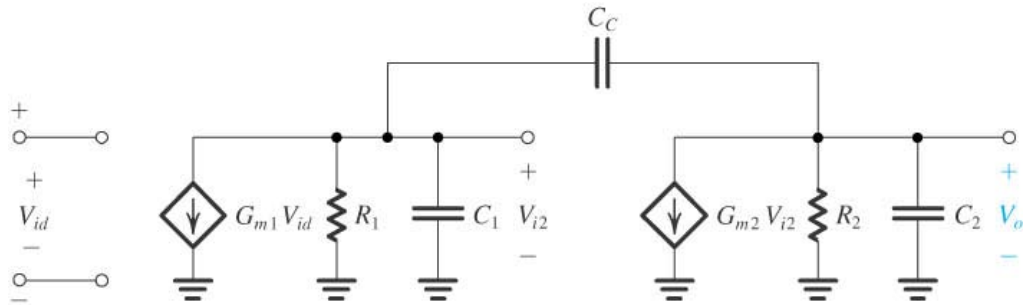
$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

(C_{gd6} is included in C_c)

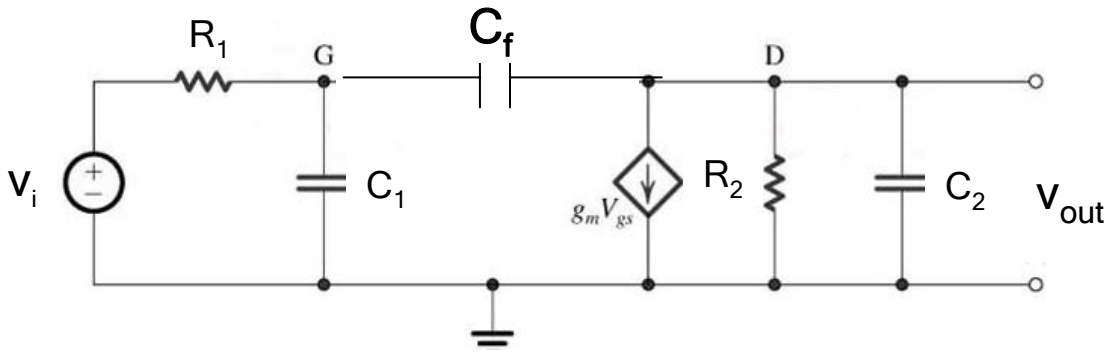
C_2 >> C_1 since C_L is usually larger

Lect. 12: Two-Stage OTA



$$\frac{V_o(s)}{V_{id}(s)} = ?$$

In Lect. 9,

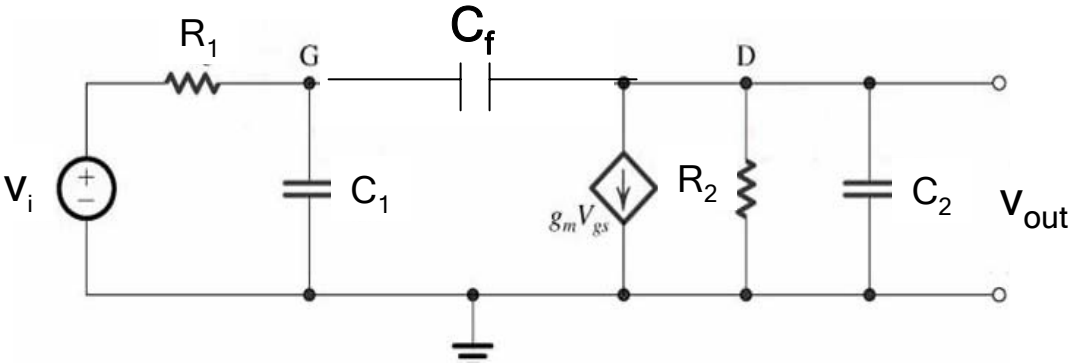


$$\frac{V_o}{V_i} = \frac{\left(g_m - sC_f\right)R_2}{1+s\left[C_1R_1 + C_2R_2 + C_f\left(g_mR_1R_2 + R_1 + R_2\right)\right] + s^2\left[C_1C_2 + C_f\left(C_1 + C_2\right)\right]R_1R_2}$$

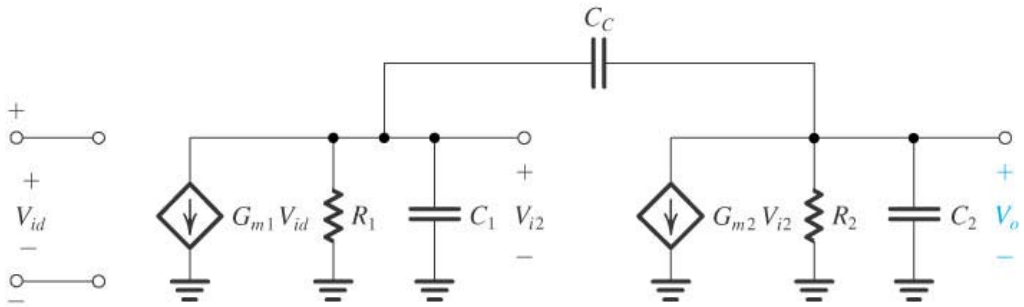
Since $V_i = G_{m1}V_{id}R_1$, $\dfrac{V_o(s)}{V_{id}(s)} = G_{m1}R_1\dfrac{V_o}{V_i}$ Same Pole-Zero characteristics!

Lect. 12: Two-Stage OTA

In Lect. 9,



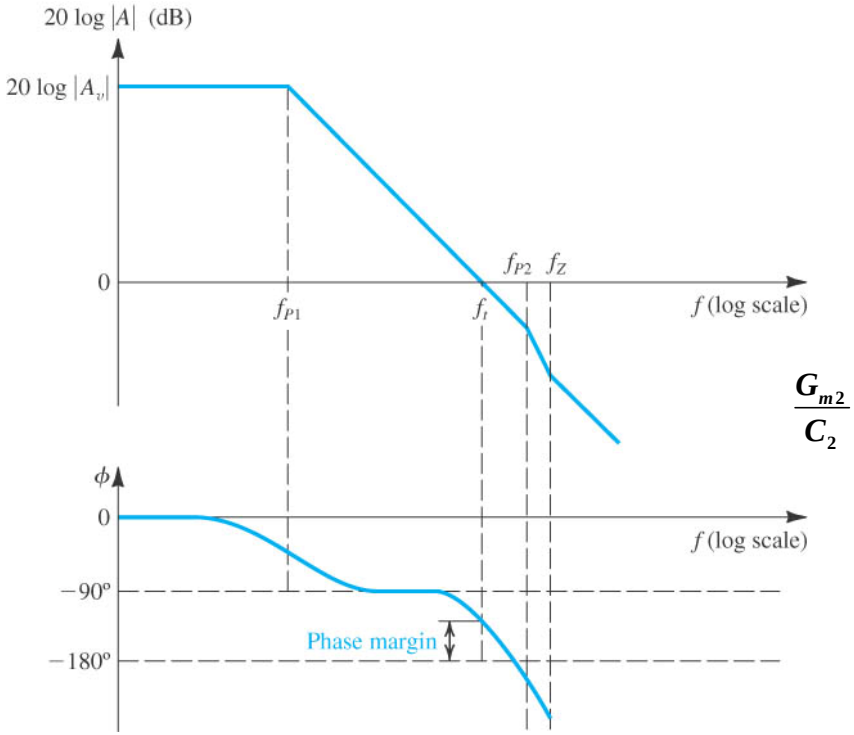
$$\omega_{P1} \simeq \frac{1}{C_f g_m R_1 R_2} \qquad \omega_{P2} \simeq \frac{g_m C_f}{C_1 C_2 + C_f (C_1 + C_2)} \qquad \omega_Z = \frac{g_m}{C_f}$$



$$\omega_{P1} \simeq \frac{1}{C_C G_{m2} R_1 R_2} \qquad \omega_{P2} \simeq \frac{G_{m2} C_C}{C_1 C_2 + C_C (C_1 + C_2)} \simeq \frac{G_{m2}}{C_2} \qquad \omega_Z = \frac{G_{m2}}{C_C}$$

Lect. 12: Two-Stage OTA

Assume we want the following Bode plot so that any amount of feedback is allowed.



$$\omega_{P1} \simeq \frac{1}{C_C G_{m2} R_1 R_2}$$

$$\omega_{P2} \simeq \frac{G_{m2}}{C_2}$$

$$\omega_Z = \frac{G_{m2}}{C_C}$$

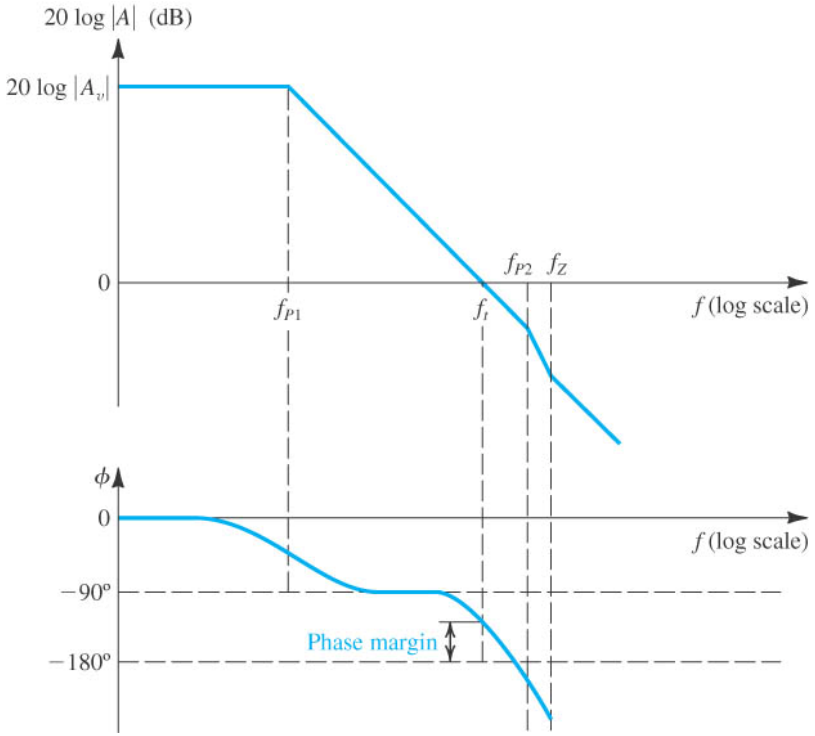
$$\omega_{P1} < \omega_t < \omega_{P2}, \omega_Z$$

$$\omega_t = |A_v| \omega_{P1} \simeq G_{m1} G_{m2} R_1 R_2 \frac{1}{C_C G_{m2} R_1 R_2} = \frac{G_{m1}}{C_C}$$

$$\omega_t < \omega_{P2} \Longrightarrow \frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2}$$

$$\omega_t < \omega_Z \Longrightarrow \frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_C} \Longrightarrow G_{m1} < G_{m2}$$

Lect. 12: Two-Stage OTA



$$\omega_{P1} \simeq \frac{1}{C_C G_{m2} R_1 R_2}$$

$$\omega_{P2} \simeq \frac{G_{m2}}{C_2}$$

$$\omega_Z = \frac{G_{m2}}{C_C}$$

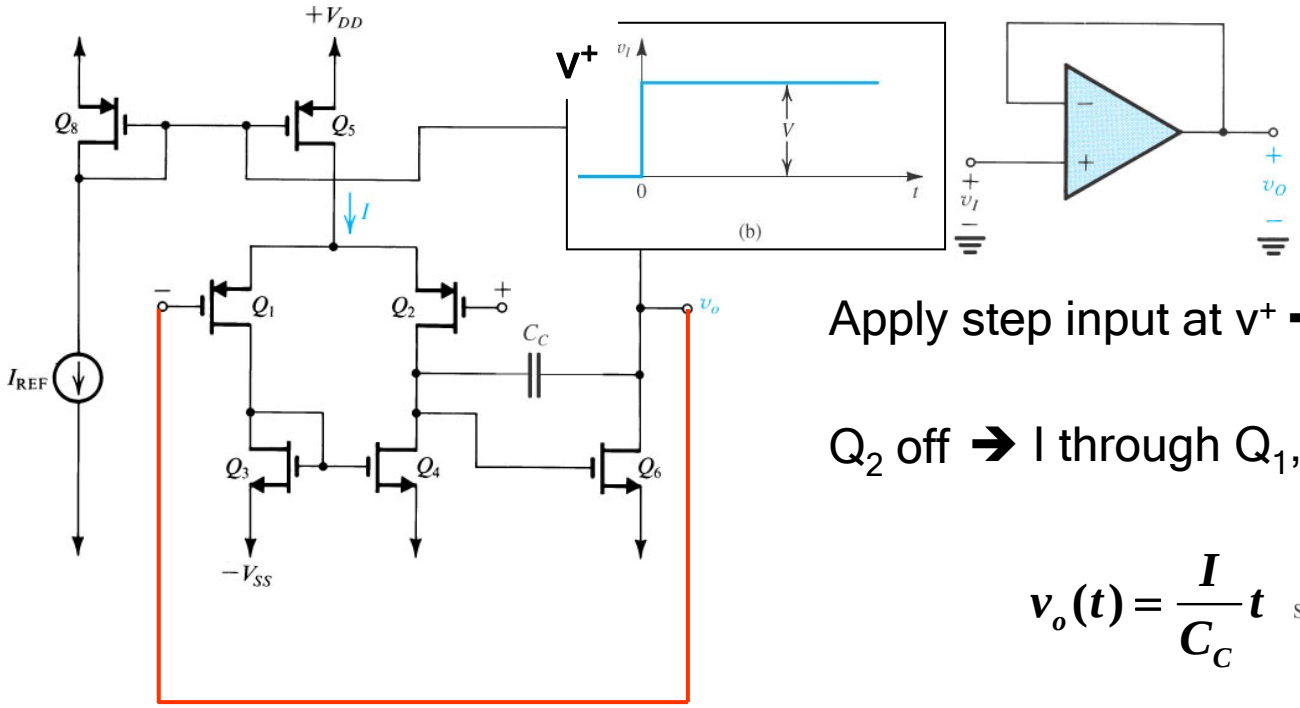
More phase margin is possible with a resistor in series with C_C

➔ Different Pole-Zero characteristics (Project #2)!

Lect. 12: Two-Stage OTA

Slew Rate

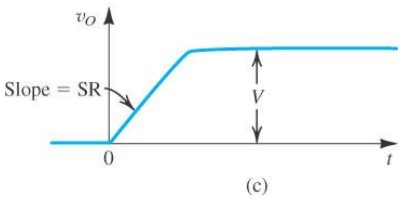
What does the circuit do?



Apply step input at v^+ ➔ $v_o(t)$=?

Q_2 off ➔ I through Q_1, Q_3 ➔ I through C_C

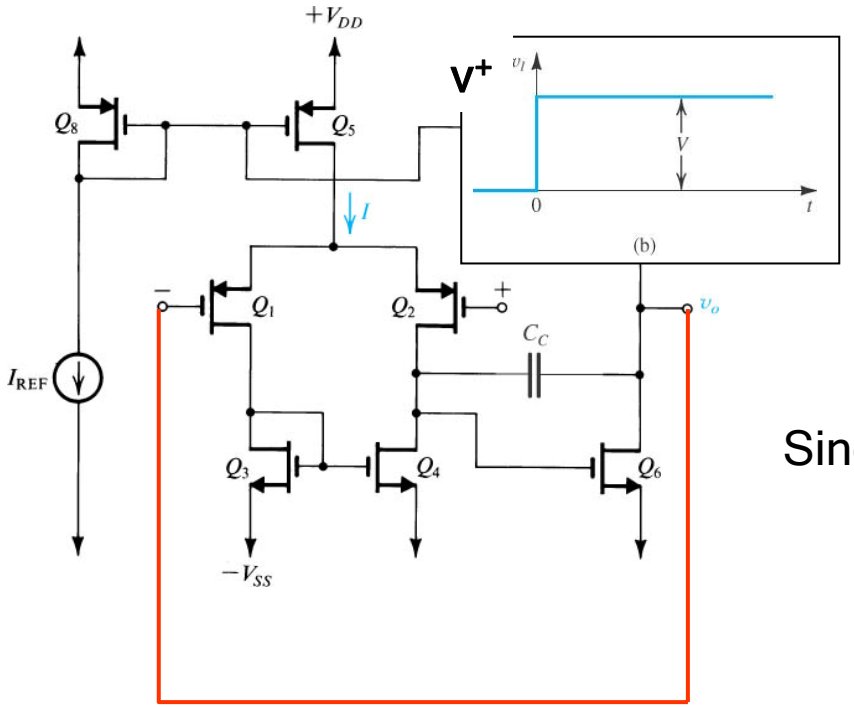
$$v_o(t) = \frac{I}{C_C} t$$



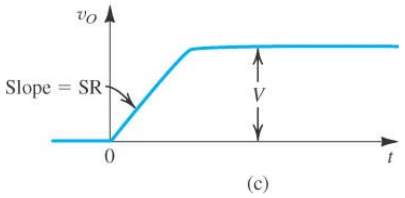
Slew Rate: Maximum rate of v_o change $\quad SR = \left.\frac{dv_o}{dt}\right|_{max} = \frac{I}{C_C}$

Lect. 12: Two-Stage OTA

Slew Rate



$$v_o(t) = \frac{I}{C_C}t$$



$$SR = \frac{I}{C_C}$$

Since $\omega_t \simeq \frac{G_{m1}}{C_C}$ and $G_{m1}=g_{m1}=\frac{2I_{D1}}{V_{GS1}-V_T}=\frac{I}{V_{GS1}-V_T}$

For same I and W/L,
PMOS has larger (V_{GS1}-V_T)

➔ Larger SR

➔ Smaller G_{m1}

$$\therefore SR = \frac{I}{C_C} = \frac{G_{m1}(V_{GS1}-V_T)}{C_C} = \omega_t(V_{GS1}-V_T)$$

Many design trade-offs!