Video amplifier provides digital gain control

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Programmable-gain amplifiers, many of them monolithic, are continuously improving, with lower noise and higher gain-bandwidth products. But for high-end applications, multichip circuits are still necessary. For example, the amplifier in **Figure 1** originally served as the photomultiplier preamplifier in a Doppler system intended for eventual operation in the Martian atmosphere. The design is based on a switchable array of six Maxim MAX4258 dual-channel video multiplexer-amplifiers, IC_1 through IC_6.

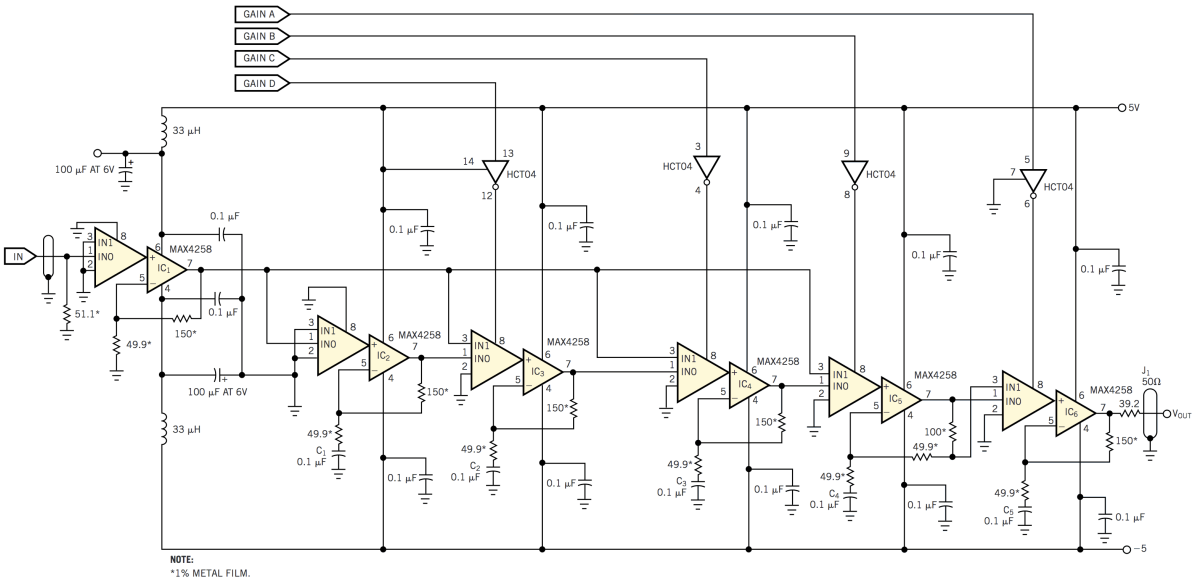

Figure 1 You can obtain eight distinct gain settings with this low-noise, high-bandwidth video amplifier.

Under control of a 4-bit input word, you can set the number of stages in the gain cascade to three, four, five, or six. Because each multiplexer-amp has a fixed gain of four, each unit change in the stage count changes the overall gain by 12 dB. In addition, you can interpose a 6dB attenuator between the last and the next-to-last gain stages. The attenuator adds a factor-of-two resolution to the programmed gain and eight distinct gain settings (**Table 1**).

TABLE 1—DIGITAL GAIN SETTINGS

Code	D	C	B	A	Gain (into 50Ω, in decibels)
1	0	0	0	0	×16=24.1
2	0	0	0	1	×32=30.1
3	0	0	1	0	×64=36.1
4	0	0	1	1	×128=42.1
5	0	1	1	0	×256=48.2
6	0	1	1	1	×512=54.2
7	1	1	1	0	×1024=60.2
8	1	1	1	1	×2048=66.2

Gain-change settling time is lower than 30 ns. The >100 MHz bandwidth of each stage results in an overall passband for all gain settings of greater than 60 MHz. The five lowpass-bandpass capacitors, C_1 through C_5, determine the lower end of the passband. In the original application, the frequencies of interest don't extend much below 100 kHz. So, using 0.1µF capacitors results in a roll-off of approximately 50 kHz. Larger values for these capacitors would reduce this figure. Omitting the capacitors for a dc response is not recommended, however, because the resulting amplification of IC_1's input offset would produce an output offset in the order of volts at high gain settings. You can generate the gain-programming word using any TTL-compatible, 8-bit parallel-I/O port, such as a PC's parallel printer port or an EIA-1284-compatible port. The HCT04 CMOS inverter chip in the gain-control pathway blocks any possible noise entry in the gain-control lines.

The overall input-referred voltage noise is approximately 2nV/√Hz, equivalent to the Johnson noise of a 250Ω resistor. Maximum output level is 15 dBm (3.6V p-p) into 50Ω and twice that into high-impedance loads. The combination of extreme gain and high-frequency response (gain-bandwidth products approaching 200 GHz) of this circuit mandates careful attention to issues of ground-plane and power-supply-bypass integrity. In addition, you must make every effort to minimize stray capacitance around the feedback-pin (Pin 5) components of all gain stages. (DI #2559)