CMOS Active-Cascode Gain Stage

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***ABSTRACT*—**An *s*-domain analysis of the full dynamics of the pole-zero pair (frequency doublet) associated with the broadly used CMOS active-cascode gain-enhancement technique is presented. Quantitative results show that three scenarios can arise for the settling behavior of a closed-loop active-cascode operational amplifier depending on the relative locations of the unity-gain frequencies of the auxiliary and the main amplifiers. The analysis also reveals that, although theoretically possible, it is practically difficult to achieve an exact pole-zero cancellation. The analytical results presented here provide theoretical guidelines to the design of CMOS operational amplifiers using this technique.

Keywords—CMOS operational amplifier, gain enhancement, active cascode, regulated cascode, gain boosting, pole-zero pair, doublet, slow settling

I. INTRODUCTION

Invented in 1979 [1] and subsequently refined in 1990 [2]–[4], the CMOS active-cascode gain-enhancement technique[1] finds wide applications in analog integrated circuits, such as Nyquist-rate and oversampling data converters, sample-and-hold amplifiers, switched-capacitor filters, band-gap reference circuits, and voltage regulators. By boosting the low-frequency transconductance of the cascode device, the technique increases the output resistance of a CMOS cascode operational amplifier (op amp), and hence the voltage gain without degrading its high-frequency performance. As a result, it is ideally suitable for on-chip applications, where a large gain-bandwidth product is desirable while driving capacitive loads. In addition, as the technique derives extra gain laterally using an auxiliary amplifier (booster) without stacking multiple cascode transistors, it retains the high-swing feature of a simple cascode stage, and thus, becomes widely popular in scaled CMOS technologies with low supply voltages.

In sampled-data applications, the circuit accuracy and speed are usually determined by the settling behavior of op amps when employed. In an attempt to achieve a high unity-gain frequency and a high dc gain simultaneously, the active cascode introduces a pole-zero pair (doublet) near the unity-gain frequency of the auxiliary amplifier, which potentially leads to slow-settling behavior of such op amps [2]. A guideline to avoid the deleterious effects of the doublet was also discussed in [2]. However, an accurate, closed-form solution of the doublet does not exist. Lacking theoretical guidance, designers often resort to circuit simulators to verify and to fine-tune their op amps, rendering the design process time consuming and heuristic.

[1] Alternative names are gain boosting, regulated cascode, and active-feedback cascode.

This note examines the doublet behavior of CMOS active cascodes. Quantitative analysis reveals that three scenarios can arise for the closed-loop settling behavior dependent on the ratio of the unity-gain bandwidth of the booster to that of the main amplifier. Sections II and III review the principles of the cascode gain stage and the CMOS active-cascode technique, respectively. Section IV presents a small-signal analysis of the active cascode and a closed-form solution of the doublet followed by the corresponding result on settling behavior. In Section V, computer simulation results are shown to validate the developed theory; and lastly, a brief summary concludes the note in Section VI.

II. CMOS Active-Cascode Gain Technique

Cascode provides a gain-enhancement function in amplifier circuits, allowing the product of the intrinsic gains of two stages–a common-source stage (CS) and a common-gate stage (CG)–to be developed in one. This has an advantage in the attainable bandwidth of the amplifier when driving a capacitive load, which itself acts as the compensation capacitor [5], [6]. As a result, a single-stage cascode amplifier typically exhibits a better power efficiency relative to a Miller-compensated two-stage design, and is widely used in analog circuits.

A. Small-Signal DC Gain

A typical CMOS cascode gain stage is shown in Fig. 1a along with its output impedance as a function of frequency in Fig. 1b. In a voltage-gain amplifier, a two-port formulation readily shows that the small-signal gain is simply the product of the effective input transconductance (G_m) and the output resistance (R_o) of the stage [7]. In Fig. 1a, assuming both transistors are biased in saturation, the drain current of M_1 is only weakly influenced by M_2 (through channel-length modulation) and the following expression of G_m holds:

$$G_m = g_{m1} \cdot \frac{(g_{m2} r_{o2} + 1) r_{o1}}{(g_{m2} r_{o2} + 1) r_{o1} + r_{o2}} \approx g_{m1}. \tag{1}$$

Thus, the extra gain developed by the cascode can only be explained by the increase in R_o:

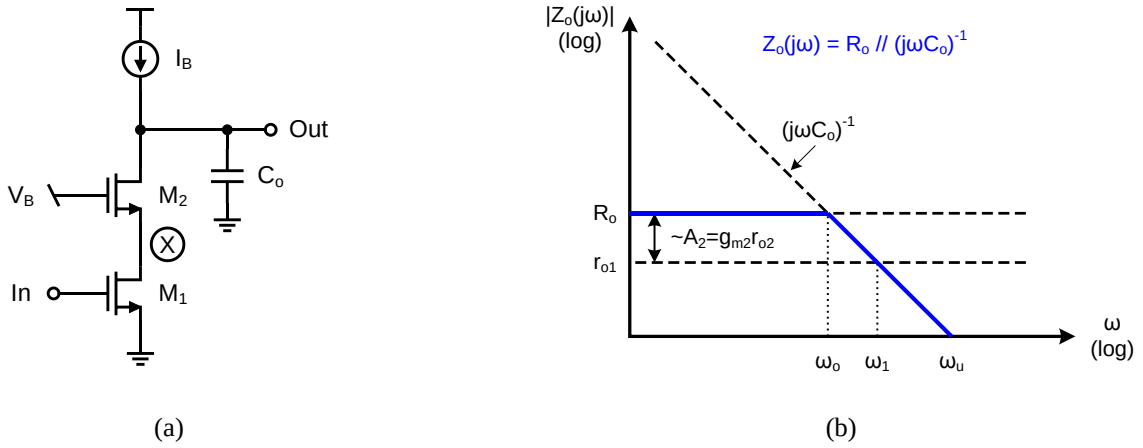
$$R_o = (g_{m2} r_{o1} + 1) r_{o2} + r_{o1}. \tag{2}$$

Eq. (2) is obvious when we consider the stage as a degenerated current source from the output-resistance standpoint, i.e., transistor M_2 is degenerated by r_{o1} when the gates of M_1 and M_2 are both ac-grounded. The factor $g_{m2} r_{o1}$ is just the loop-gain of the local series feedback formed by M_2 and r_{o1}. Thus, the dc gain of the stage is

$$A_{dc} = -G_m \cdot R_o = -g_{m1} r_{o1} \cdot (g_{m2} r_{o2} + 1). \tag{3}$$

B. Frequency Response

Next we consider the frequency response of the stage by adding a load capacitor C_o to the output. We will neglect all other capacitance in the circuit for simplicity. Since the addition of C_o has no effect on the G_m part of



(a) (b)

Fig. 1. CMOS cascode gain stage: (a) simplified circuit diagram and (b) Bode plot of the output impedance. The frequency dependence of the output impedance derives from C_o.

(1), the frequency dependence derives solely from the output impedance $Z_o(s)$, which can be expressed as

$$Z_o(s) = R_o \| (sC_o)^{-1} = \frac{R_o}{1+sR_oC_o}, \tag{4}$$

and depicted in Fig. 1b by the solid lines. Since in this case the G_m part exhibits no frequency dependence, the overall frequency response of the small-signal gain is simply

$$A(s) = -G_m \cdot Z_o(s) = -\frac{G_mR_o}{1+sR_oC_o}, \tag{5}$$

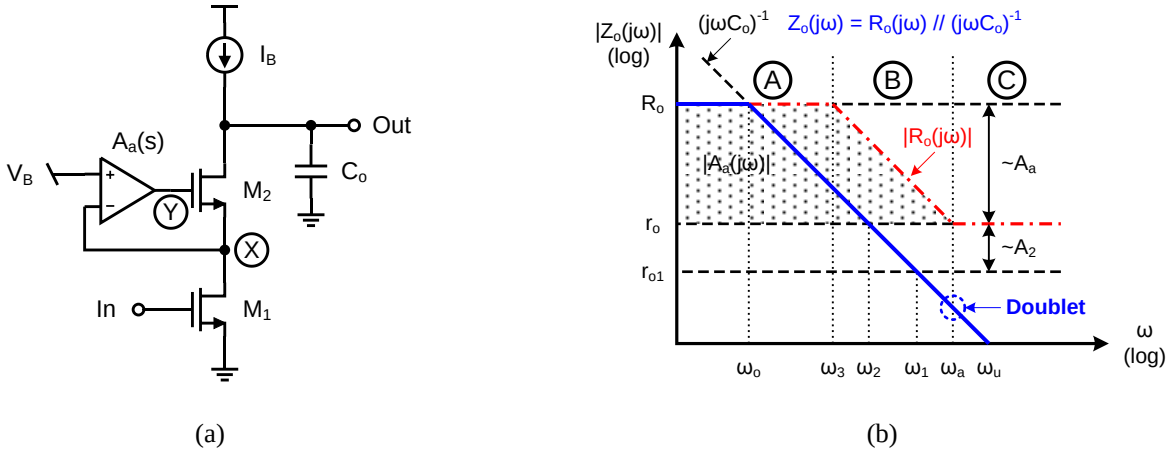
which has a dominant pole at ω_o ($\approx 1/R_oC_o$) and a unity-gain frequency of ω_u ($\approx g_{m1}/C_o$).

III. CMOS Active-Cascode Gain Technique

CMOS active cascode further improves the achievable dc gain by employing a lateral auxiliary amplifier—$A_a(s)$ in Fig. 2a—to enhance the cascode effect. The operation principles of the technique can be explained as follows.

A. Output Resistance and Gain

At this point, we understand that the extra voltage gain of the normal cascode stage in Fig. 1a derives from the improved output resistance due to the local series feedback formed by M_2 and r_{o1}. Therefore, additional gain can be potentially obtained by further increasing either g_{m2} or r_{o1}. The active-cascode technique exploits the g_{m2} option as shown in Fig. 2a. Let's consider the effective transconductance of M_2 due to the presence of the auxiliary amplifier. The gate-source voltage of M_2 is $0-v_x = -v_x$ and $v_y-v_x = -(A_a+1)v_x$ before and after the booster insertion, respectively. Therefore, the net effect of the booster is essentially to make the effective transconductance of M_2



(a) (b)

Fig. 2. CMOS active-cascode gain stage: (a) simplified circuit diagram and (b) Bode plot of the output impedance. The frequency dependence of the output impedance derives from C_o and the auxiliary amplifier $A_a(s)$.

(A_a+1) times larger, with everything else being equal between Figs. 1a and 2a. Thus, the dc solution to the active-cascode amplifier of Fig. 2a can be readily obtained by substituting (A_a+1)g_{m2} for g_{m2} in (1)–(3):

$$G_m = g_{m1} \cdot \frac{\left[\left(A_a+1\right) g_{m2} r_{o2} + 1\right] r_{o1}}{\left[\left(A_a+1\right) g_{m2} r_{o2} + 1\right] r_{o1} + r_{o2}} \approx g_{m1}, \tag{6}$$

$$R_o = \left[\left(A_a+1\right) g_{m2} r_{o1} + 1\right] r_{o2} + r_{o1}, \tag{7}$$

$$A_{dc} = -g_{m1} r_{o1} \cdot \left[\left(A_a+1\right) g_{m2} r_{o2} + 1\right].^{2} \tag{8}$$

We see that the key function of the booster is to enhance g_{m2}, hence to further increase the output resistance (and gain) of the amplifier.[3] This is done by introducing a push-pull operation between the source and gate voltages of M_2, i.e., between nodes X and Y, through the insertion of a booster amplifier. This inevitably introduces another negative feedback loop that is local to the cascode M_2. As the bandwidth of the booster amplifier is finite, the frequency response of the active cascode exhibits an interesting artifact—a pole-zero pair or frequency doublet, which will be explained next.

B. Frequency Doublet

For simplicity, we will assume a single-pole roll-off for the auxiliary amplifier:

$$A_a(s) = \frac{A_a}{1 + sA_a/\omega_a}. \tag{9}$$

[2] The body effect of M_2 can be readily included in (6)–(8). For example, the dc gain is $A_{dc} = -g_{m1} r_{o1} \cdot \left\{\left[\left(A_a+1\right) g_{m2} + g_{mb2}\right] r_{o2} + 1\right\}$ with body effect.

[3] A similar argument also suggests that the technique works only for MOSFET, not BJT amplifiers, in that the base resistance of BJT will ultimately limit the achievable amplifier output resistance to approximately $\beta_0 r_o$, where β_0 is the small-signal current gain of the BJT, regardless of the value of A_a.

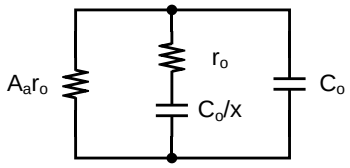


Fig. 3. Model of the output impedance of the active cascode in Fig. 2.

Therefore, the frequency dependence of the gain stage can be readily obtained by replacing A_a with $A_a(s)$ in (6)−(8).

The effect of $A_a(s)$ on the output resistance was qualitatively analyzed in [2], which is sketched in Fig. 2b. Let's examine R_o first. The roll-off of $A_a(s)$ at high frequency introduces frequency dependence of R_o as illustrated by the dash-dotted lines in Fig. 2b, mathematically,

$$R_o(s) = \left[A_a(s) + 1\right] g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2}. \tag{10}$$

In Fig. 2b, $r_o = g_{m2} r_{o1} r_{o2} + r_{o1} + r_{o2}$, which can also be obtained from (10) by setting $A_a(s)$ to 0. Thus, $R_o(s)$ exhibits a pole at ω_3 and a zero at ω_a in Fig. 2b. The overall output impedance of the stage $Z_o(s)$ is then the parallel combination of $R_o(s)$ and $(sC_o)^{-1}$,

$$Z_o(s) = R_o(s) \| (sC_o)^{-1}, \tag{11}$$

which is represented by the solid lines in Fig. 2b.

An equivalent RC model of $Z_o(s)$ was proposed in [8], which is sketched in Fig. 3. If we divide the frequency axis into three bands by ω_3 and ω_a in Fig. 2b, the left resistor $A_a r_o$ in Fig. 3 captures the low-frequency output resistance in region A ($\omega \le \omega_3$), the middle series R-C network captures the roll-off part of $R_o(s)$ in region B ($\omega_3 \le \omega \le \omega_a$) and the flat part in region C ($\omega \ge \omega_a$), and lastly the right C_o represents the shunt load capacitor. In regions A and B, an approximate expression of the output impedance is

$$Z_o(s) \approx A_a r_o \| \frac{1}{sC_o} \| \frac{x}{sC_o}, \tag{12}$$

where, $x = \omega_3/\omega_o = \omega_a/\omega_2$. Obviously, this only results in one pole at ω_o. In regions B and C, an approximate expression of the output impedance is given by

$$Z_o(s) \approx \left(r_o + \frac{x}{sC_o} \right) \| \frac{1}{sC_o} = \frac{1 + s\frac{r_o C_o}{x}}{sC_o \left(1 + \frac{1}{x} + s\frac{r_o C_o}{x} \right)}. \tag{13}$$

Apparently, this results in two poles and one zero, with a pole at $s_p = -(1+x)/r_o C_o$ and a zero at $s_z = -x/r_o C_o$—

both are very close to the unity-gain frequency of the booster ω_a when $x >> 1$ holds. This is the pole-zero pair or doublet.

C. Slow Settling

In [9]−[11], a closed-loop amplifier containing a closely spaced pole-zero pair in its frequency response was examined. It was found that, although the doublet effect on the open-loop Bode plot is often negligible, its deleterious impact on the time-domain settling behavior may be significant. Specifically, it introduces a so-called slow-settling component to the step response of the amplifier. The magnitude of the slow component is proportional to the doublet spacing and the time constant corresponds to the doublet frequency.

The same line of development will be followed here to establish a framework for the next two sections. Let the open-loop transfer function have a closely spaced pole-zero pair at (ω_z, ω_p). The dominant pole and unity-gain frequencies, ω_o and ω_u, respectively, are given for the open-loop response. When the loop is closed, the feedback will reduce the pole-zero spacing by an amount equal to the loop-gain at the doublet frequency; and the closed-loop pole frequency will move to ω_p' [10], [11]. With the assumption $\omega_o << (\omega_z, \omega_p) << \beta\omega_u$, the step response of the closed-loop amplifier is given as

$$V_o(t) \approx V\left(1 - k_1 e^{-\beta\omega_u t} + k_2 e^{-\omega_p' t}\right), \tag{14}$$

where, β is the feedback factor, and

$$\omega_p' \approx \omega_z\left(1 + \frac{\omega_z - \omega_p}{\beta\omega_u - \omega_z}\right) \approx \omega_z, \quad k_2 \approx \frac{\omega_z - \omega_p}{\beta\omega_u}. \tag{15}$$

The k_2 term in (14) is the slow-settling component when $\omega_p' < \beta\omega_u$ holds.

IV. Solving Doublet

For the CMOS active cascode, although the approximate equivalent circuit model of $Z_o(s)$ in Section III-B reveals the existence of a pole-zero pair near the unity-gain frequency of the auxiliary amplifier ω_a, the results are only qualitative as the frequency dependence of $G_m(s)$ is not considered in the model. In this section, we will attempt to obtain an exact small-signal solution for the doublet. In the treatment, the frequency dependence of the circuit is assumed to derive from the load capacitor C_o and the booster $A_a(s)$; and all other capacitance will be neglected first to keep the math tractable. After the first-order pole- zero behavior is derived, the effects of other capacitance in the circuit will be examined in Section V using computer simulation.

A. Open-Loop Transfer Function

To solve for the open-loop transfer function, we first obtain the expressions for $G_m(s)$ and $Z_o(s)$:

$$G_m(s) = g_{m1} \cdot \frac{\left[\left(A_a(s)+1\right) g_{m2} r_{o2} + 1\right] r_{o1}}{\left[\left(A_a(s)+1\right) g_{m2} r_{o2} + 1\right] r_{o1} + r_{o2}}, \tag{16}$$

$$Z_o(s) = R_o(s) \| \frac{1}{sC_o} = \frac{R_o(s)}{1 + sC_o R_o(s)}. \tag{17}$$

The product of (16) and (17) gives the small-signal voltage gain,

$$\begin{aligned} A(s) = G_m(s) \cdot Z_o(s) &= \frac{\left[\left(A_a(s)+1\right) A_2 + 1\right] A_1}{1 + sC_o R_o(s)} \\ &= \frac{\left[\left(A_a+1\right) A_2 + 1\right] A_1 + \left[\dfrac{A_a A_1 \left(A_2+1\right)}{\omega_a}\right] s}{1 + \left\{\left[\left(\left(A_a+1\right) A_2 + 1\right) r_{o1} + r_{o2}\right] C_o + \dfrac{A_a}{\omega_a}\right\} s + \left\{\left[\left(A_2+1\right) r_{o1} + r_{o2}\right] C_o \dfrac{A_a}{\omega_a}\right\} s^2}. \end{aligned} \tag{18}$$

where $A_1 = g_{m1} r_{o1}$, $A_2 = g_{m2} r_{o2}$, and the expression of $A_a(s)$ in (9) is assumed.

B. Frequency Doublet

The numerator of (18) readily solves to one LHP zero:

$$s_z = -\left(\frac{A_2}{A_2+1} + \frac{1}{A_a}\right)\omega_a \approx -\omega_a. \tag{19}$$

To solve for the poles, we define $\gamma = r_{o2}/r_{o1}$, $\omega_u = g_{m1}/C_o$, and $r_{o1} = A_1/C_o\omega_u$; the denominator of (18) reduces to the following:

$$s^2 + \left[\frac{\left(A_a+1\right) A_2 + 1 + \gamma}{A_a\left(A_2+1+\gamma\right)}\omega_a + \frac{\omega_u}{A_1\left(A_2+1+\gamma\right)}\right] s + \frac{\omega_u \omega_a}{A_a A_1 \left(A_2+1+\gamma\right)} = 0. \tag{20}$$

Due to the presence of the doublet, we may assume that one pole is at $s_{p1} = -\alpha\omega_a$ with $\alpha \approx 1$; and (20) can be factorized into

$$\left(s + \alpha\omega_a\right) \cdot \left(s + \frac{\omega_u}{\alpha A_a A_1 \left(A_2+1+\gamma\right)}\right) = 0. \tag{21}$$

Compare (21) with (20), we obtain

$$\alpha \approx \frac{A_2}{A_2+1+\gamma} + \frac{1}{A_a} + \frac{A_a - 1}{A_a A_1 \left(A_2+1+\gamma\right)} \frac{\omega_u}{\omega_a}, \tag{22}$$

where, $\dfrac{\omega_u}{A_a A_1\left(A_2+1+\gamma\right)} \approx \omega_o << \omega_a$ is assumed since $x >> 1$. At this point, we arrive at the solution for the two LHP poles of the open-loop transfer function:

$$-s_{p1} \approx \frac{\omega_u}{A_1\left[\left(A_a+1\right)A_2+1+\gamma\right]+\left(A_a-1\right)\dfrac{\omega_u}{\omega_a}} \approx \omega_o, \tag{23}$$

$$-s_{p2} \approx \left(\frac{A_2}{A_2+1+\gamma}+\frac{1}{A_a}\right)\omega_a + \frac{A_a-1}{A_aA_1\left(A_2+1+\gamma\right)}\omega_u \approx \omega_a, \tag{24}$$

where, the fact $x = \omega_3/\omega_o >> 1$ is again assumed.

C. Closed-Loop Settling Behavior

We recognize that s_{p1} of (23) is the dominant pole of the open-loop amplifier and (s_z, s_{p2}) of (19) and (24) form a doublet. Substituting (19) and (24) in (15) results in an expression for the slow-settling component:

$$\omega_p' \approx \omega_a, \tag{25}$$

$$k_2 \approx \frac{1}{\beta}\left[\frac{A_2\gamma}{\left(A_2+1\right)\left(A_2+1+\gamma\right)}\frac{\omega_a}{\omega_u} - \frac{A_a-1}{A_aA_1\left(A_2+1+\gamma\right)}\right]. \tag{26}$$

Eq. (26) reveals that three scenarios can arise for the closed-loop settling behavior dependent on ω_a/ω_u, the ratio of the unity-gain bandwidth of the auxiliary amplifier to that of the open-loop main amplifier:

1) $k_2 = 0$, critically damped, when $\omega_u/\omega_a \approx \gamma A_1 = g_{m1}\,r_{o2}$. The pole cancels the zero exactly and the slow-settling term vanishes;
2) $k_2 > 0$, overshoot, when $\omega_u/\omega_a < g_{m1}\,r_{o2}$. This results in a falling doublet;
3) $k_2 < 0$, slow settling, when $\omega_u/\omega_a > g_{m1}\,r_{o2}$. This results in a rising doublet, the one often cited in literature [2].

In addition, as $\omega_u = g_{m1}/C_o$, the criterion $\omega_u/\omega_a = g_{m1}\,r_{o2}$ leads to $\omega_a = 1/r_{o2}C_o$. In other words, even when a constant C_o is assumed, the significant dependence of r_{o2} on the amplifier output voltage makes it practically difficult to achieve an exact pole-zero cancellation.

There are two strategies to avoid the deleterious effect of the doublet. One suggests to make $\omega_a > \beta\omega_u$ to avoid slow settling [2]. The other suggests to make k_2 small enough, i.e., to have a "slow-but-accurate" doublet. Let's examine the feasibility of the latter. Assuming a very slow doublet, i.e., $\omega_a << \beta\omega_u$ holds, then following (26),

$$k_2 \approx -\frac{1}{\beta A_1A_2} \approx -\frac{1}{\beta A_o}. \tag{27}$$

This implies that k_2 cannot be made arbitrarily small—the smallest value of k_2 is proportional to the accuracy level of the original amplifier without gain enhancement. A "slow-but-accurate" doublet does not exist.

Table I. Small-signal parameters used in simulation

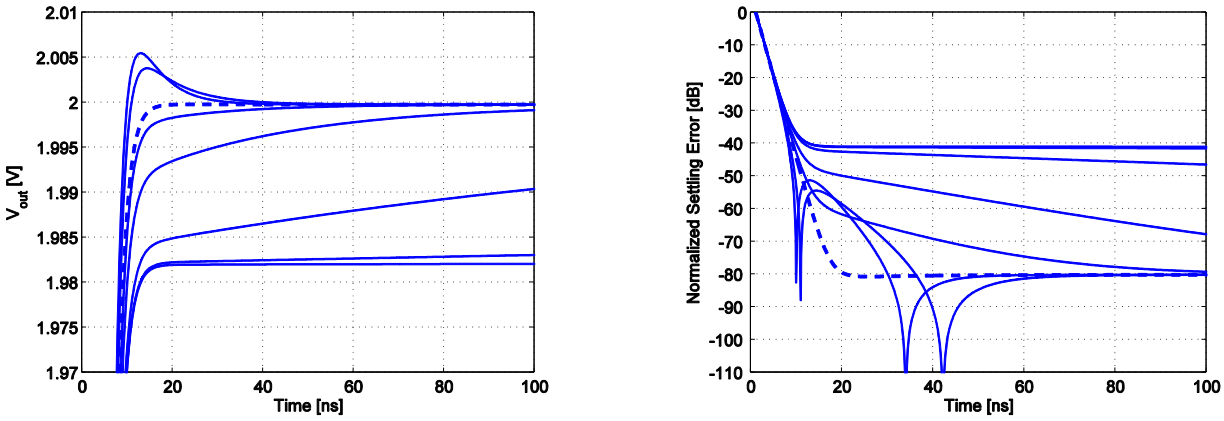
β	0.5	r_{o2}	10 k
f_u	200 MHz	C_m	$C_o/3$
A_a	40 dB	C_{gs1}	$C_o/6$
g_{m1}	2 mA/V	C_{gs2}	$C_o/6$
g_{m2}	1 mA/V	C_{gd1}	$C_o/12$
r_{o1}	10 k	C_{gd2}	$C_o/12$

V. Computer Simulation

Computer simulations are performed to validate the analysis developed in Section IV. For easy access to and programmability of all device parameters, i.e., g_m, r_o, etc., a small-signal linear model of the active cascode shown in Fig. 4 was used instead of a real transistor circuit. An ideal VCVS models the auxiliary amplifier with a transfer function $A_a(s)$. In Fig. 5, the external feedback is assumed ideal with a feedback factor β = ½ (i.e., the closed-loop gain is 2); and a 1-V step is applied at the input. A capacitor C_m on node X (resulting in the second pole) and the C_{gs}' and C_{gd}'s of M_1 and M_2 are also included for completeness. All device parameters used in the simulation are listed in Table I.

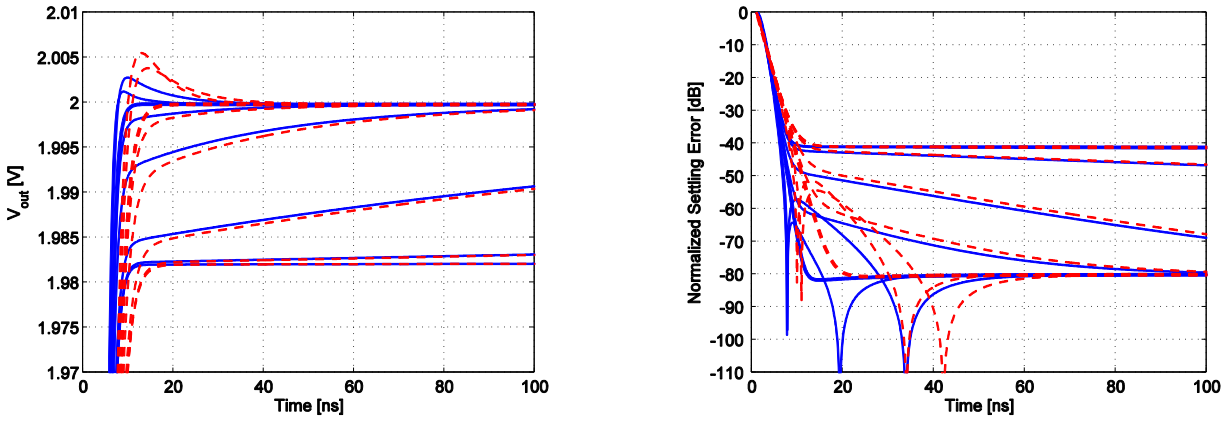
A. *Intrinsic Doublet Behavior*

To evaluate the intrinsic behavior of the doublet, all capacitors are removed except C_o in Fig. 4; the unity-gain frequency of $A_a(s)$ is swept to observe the settling behavior of the closed-loop amplifier. Figs. 6a and 6b show the output voltage and the normalized settling error of the circuit, respectively. The settling error is defined as



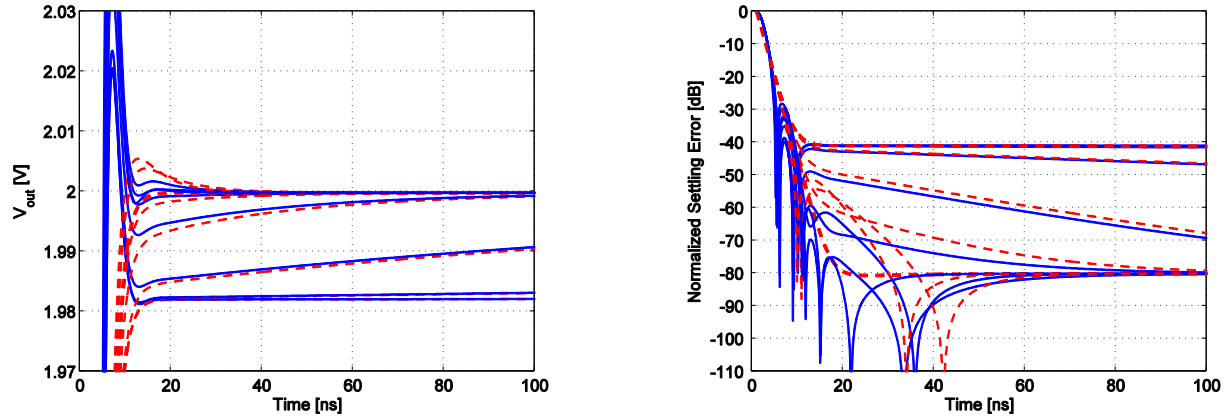
(a) (b)

Fig. 4. Closed-loop settling behavior for f_a = 10 kHz, 100 kHz, 1 MHz, 5 MHz, 9 MHz, 10.95 MHz, 20 MHz, and 30 MHz: (a) the amplifier output voltage (increasing in f_a from bottom up), and (b) the normalized settling error (increasing in f_a from top down). Open-loop parameters: f_a = 10 kHz, f_u = 100 MHz, and A_{to} = 80 dB. The dashed curves (f_a = 10.95 MHz) correspond to the case of k_2 = 0, i.e., exact pole-zero cancellation.



(a) (b)

Fig. 5. The same results as those of Fig. 4 with the inclusion of C_m. The phase margin of the loop-gain is 71°. The dashed curves are for $C_m = 0$. The basic settling behavior remains the same in the presence of a second pole.



(a) (b)

Fig. 6. The same results as those of Fig. 4 with the inclusion of C_m and the C_{gs}'s and C_{gd}'s of M_1 and M_2. The slow tails of the transients closely resemble those of the original case (the dashed curves) in spite of the initial significant overshoots.

$$\delta(t) = \frac{V_o(t) - V_i(t)/\beta}{V_i(t)/\beta}, \tag{28}$$

It is apparent that indeed three scenarios for the settling behavior exist as predicted in Section IV-C. Specifically, a critically damped output transient was observed confirming the possibility of an exact pole-zero cancellation. In the example used here, (26) predicts that $k_2 = 0$ when $f_a = (2\pi r_{o2} C_o)^{-1} \approx 10$ MHz; while computer

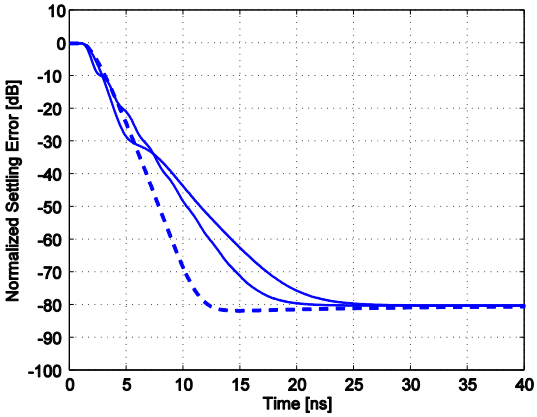


Fig. 7. The normalized settling error for f_a = 10.95 MHz (dashed curve), 100 MHz, and 1 GHz with $f_{p2} \approx$ 300 MHz.

simulation reveals that this actually occurs for $f_a \approx$ 10.95 MHz. In addition, Fig. 6b further indicates that, when the slow-settling component is really "slow" ($\omega_a << \beta\omega_u$), the knee accuracy where the slow term starts to dominate is always nearly −40 dB, corresponding to $k_2 = 1/\beta A_0 = -0.01$ as predicted by (27).

B. Effect of the Second Pole

A capacitor C_m at node X in Fig. 4 is added to introduce a non-dominant pole with a frequency three times larger than $\beta\omega_u$, the close-loop bandwidth (i.e., the phase margin of the loop-gain is around 71 °). The simulation results are shown in Figs. 7a and 7b. The basic settling behavior is unaltered with the inclusion of the second pole; and the slow tails after the initial overshoots die out closely resemble those of the case with $C_m = 0$, especially when $\omega_a << \beta\omega_u$ holds.

C. Effect of Other Parasitics

The C_{gs}' and C_{gd}'s of the transistors M_1 and M_2 are further included to make the small-signal model complete. Reasonably large values for these capacitors are assumed (Table I), and the simulation results are shown in Figs. 8a and 8b. Again, the behavior of the slow-settling component is seemingly independent of the various second-order effects introduced by the parasitics. An exact pole-zero cancellation always occurs for $f_a \approx$ 10.95 MHz.

In [2], the criterion $\beta\omega_u < \omega_a < \omega_{p2}$ was proposed to ensure proper operation of the active cascodes. This is verified in simulation by keeping C_m constant while stepping ω_a up to and beyond ω_{p2}. Fig. 9 illustrates that sluggish settling occurs when ω_a is in the vicinity of ω_{p2}, where the local feedback loop formed by the booster and the cascode becomes marginally stable. The instability is lifted when ω_a is further pushed out (not shown in the figure).

VI. CONCLUSION

An accurate, closed-form *s*-domain analysis and computer simulation results of the pole-zero pair (doublet) associated with the widely used CMOS active-cascode gain stage are presented. The conventional picture of "slow settling" is clarified and augmented with a set of equations that completely describe the doublet dynamics. These results provide easy-to-follow guidelines to the design of such amplifiers in practice.

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