A 200nV/√Hz Noise PSD Signal-Conditioning Circuit with Sensor-Offset Cancellation

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Abstract: - This paper describes a low-noise low-offset signal conditioning circuit with a feature of canceling an offset voltage caused by sensor elements. A Wheatstone bridge with sensor elements such as piezoresistors usually has an offset voltage due to the mismatch of resistors. In order to reduce or cancel this offset voltage, a DC voltage corresponding to the sensor-offset voltage is given and chopper-modulated, then subtracted from the chopper-modulated input signal. The circuit was fabricated in a 1.6 micrometer CMOS process and a 200nV/√Hz input noise power spectral density (PSD) was achieved using a 30-kHz chopper frequency. It consumed 700 micro amperes with +/– 0.9V supply voltages.

Key-Words: - chopper amplifier, analog signal processing.

1 Introduction

A piezoresistor is widely used as a sensing device such as a pressure sensor, a magnetic field sensor, and an accelerometer [1][2]. Generally a Wheatstone bridge with four piezoresistors shown in Fig.1 is utilized to convert a physical amount of interest into voltage.

The output of the bridge is typically an order of millivolts and hence it needs to be amplified with a gain of several hundreds for the subsequent signal processing such as analog-to-digital conversion. The amplification has to be done while keeping the noise caused by the amplifier as low as possible and the chopper amplifier is a good candidate for this purpose since it has very low noise and DC offset voltage [3].

On the other hand, the output voltage of the sensor bridge contains a DC offset due to the mismatch of piezoresistors in the bridge. For example a 0.5% mismatch of resistors in the bridge with a 3-V supply voltage results in a 15-mV offset voltage. Since this offset voltage is amplified by a gain of a few hundred as well as the generated output voltage proportional to the physical amount of interest, the DC offset caused by the sensor elements has to be cancelled in the signal-conditioning circuit.

Fig.2 shows an example of sensor-offset cancellation configuration. A DC offset generator consists of a buffer op-amp and a variable voltage source. After the sensor output is pre-amplified by an amplifier AMP1, a DC offset voltage is subtracted, and then the residue is amplified by a subsequent amplifier AMP2. Since the op-amp used in the DC offset generator has a noise, this noise is also amplified by AMP2. Hence, the noise increases and it becomes a serious problem in a high-precision sensor system.

In earlier work on the low-noise low-offset amplifier, quite a few circuits, such as a chopper amplifier, an autozeroing circuit, and a composite of both techniques, have been reported [3]-[6]. Although these circuits significantly reduce the offset voltage and noise caused by the op-amp, a method for cancelling the offset voltage caused by sensor elements has not been reported.

In this paper, we propose a signal conditioning circuit with a feature of canceling the sensor offset voltage while keeping the noise level as low as possible.

2 Proposed Circuit for Sensor Signal Conditioning

Fig. 3 shows a proposed sensor signal conditioning circuit using a chopper amplifier with a feature of canceling the sensor offset voltage. Each op-amp in Fig. 3 has a noise at the input denoted as v_{ni}. These noises of op-amps will be chopper-modulated to a clock frequency and removed by a low-pass filter. (The low-pass filter is not shown in Fig. 3.)

A variable DC voltage source in Fig. 3 produces a DC voltage to cancel the DC offset due to the sensor (piezoresistor) mismatch. The variable voltage source can be realized by a reference voltage, a resistor ladder, switches, and electrically erasable programmable read-only memories (EEPROMs) as shown in Fig. 4 for example. After measuring a sensor-offset voltage, data corresponding to the sensor-offset is stored in EEPROMs which enable a switch in the resistor ladder to provide a DC voltage.

The variable DC voltage is chopper-modulated as well as the input signal (the output of the sensor bridge) and added together followed by a consequent amplification. If the DC voltage is equal to the sensor offset and the polarity is opposite from each other, the sensor offset will be cancelled.

To generate a variable DC voltage with the opposite polarity for a positive sensor-offset voltage, clock $\phi 1$ and $\phi 2$ shown in paretheses in Fig. 3 will be used.

3 Experimental results

The signal-conditioning circuit with a feature of canceling a sensor-offset voltage was fabricated in a 1.6μm CMOS process. The chip microphotograph is shown in Fig. 5. And the circuit implemented in the chip is shown in Fig. 6. There are three input terminals: in1 and in2 for a sensor bridge (that is, a main path) and in3 for cancellation of sensor-offset voltage. Note that a voltage applied between the terminals in1 and in2 is amplified with a gain of 100 while a voltage applied to the terminal in3 is amplified with a gain of 10.

In this test chip, a variable DC voltage source using EEPROMs are not implemented. Instead, it is provided from an input terminal in3 (in Fig.6) using an external voltage source AFG3021 (Tektronix) for evaluation of the circuit principle.

Differential output voltages of the circuit were converted to a single-ended voltage by a differential amplifier ADA400 (Tektronix) and then the noise power spectral density (PSD) was measured by an FFT analyzer CF-5220 (Ono Sokki). +/– 0.9V supply voltages were used (instead of a 1.8V supply voltage) for ease of measurements.

Dependence of the noise spectral density on chopper frequency is shown in Fig.7(a). The higher the clock frequency is, the lower the noise PSD becomes. In this noise measurement, all the input terminals (in1, in2, and in3) in Fig. 6 were connected to 0V.

Dependence of the gain of the circuit on chopper clock frequency is shown in Fig.7(b). A 15-Hz sinusoidal input with an amplitude of 10mVpp was used for the measurement. At a clock frequency of 30kHz, the gain decreased by 1.8% compared to the one at lower clock frequencies. In the following experimental results, a clock frequency (a chopper frequency) of 30kHz was chosen for measurements assuming a tolerance of 2% for the gain error.

Next, four different experimental conditions and their results are shown below.

1) in1=in2=in3=0V (GND).
In order to measure the offset voltage of this circuit, all the input terminals (in1, in2, and in3) in Fig. 6 were connected to 0V. Measured offset voltage at the output was 1mV. Since the total gain of the circuit is 100, the input-referred offset voltage of this circuit is 10μV.

Fig. 8 shows the noise power spectral density at the output of the circuit. The measured PSD using a 30-kHz chopper frequency was 19.3μV/√Hz in average from DC to 20Hz. And the input-referred noise PSD was 193nV/√Hz.

2) in1: a sinusoidal signal plus a DC offset of 1mV; in2=in3=0V.
Next a 15-Hz sinusoidal signal with an amplitude of 10mVpp was given to the terminal in1. (The differential output was 1Vpp.) Both input terminals in2 and in3 were connected to 0V. When a DC offset voltage of 1mV was added to the sinusoidal input, the output shifted 100mV. The output waveform (200mV/div, 10ms/div) is shown in Fig.9(a).

3) in1: a sinusoidal signal plus a DC offset of 1mV; in2=0V; in3=10mV.
Then, a DC voltage of 10mV was added to the terminal in3 to cancel the DC component caused by the offset voltage given at in1. Also the clock signals $\phi 1$ and $\phi 2$ shown in parentheses in Fig.6 were used to

multiply 10mV by –1. The output waveform is shown in Fig.9(b). As can be seen from Fig.9(b), the output shifted –100mV by the 10-mV DC voltage applied to the terminal in3. We can see that this offset-cancellation system works well.

4) in1=1mV, in2= 0V, in3=10mV.
In order to investigate the noise PSD while sensor-offset canceling, a DC voltage of 1mV was applied between in1 and in2, and a DC voltage of 10mV to in3. In this case, the input-referred noise PSD was 201nV/√Hz, which is slightly larger than the one without the sensor-offset canceling feature (193 nV/√Hz), but the noise increase was only less than 5%.

Table 1 shows experimental results of this chip. The noise of this work is considered to be due to the thermal noise of the op-amp. By enlarging the transconductance of the input stage of the op-amp, lower noise PSD is expected for this circuit. The circuit consumed 700μA with +/– 0.9V supply voltages.

4 Conclusion

We have proposed a low-noise low-offset signal conditioning circuit with a feature of canceling an offset voltage caused by mismatch of piezoresistor sensor elements. In order to cancel this offset voltage, a DC voltage corresponding to the sensor-offset voltage is given and chopper-modulated, then subtracted from the main chopper amplifier. The circuit was fabricated in a 1.6 micrometer CMOS process and 200nV/√Hz input noise PSD was achieved using a 30-kHz chopper frequency. This noise PSD was nearly the same with or without sensor-offset cancellation. The circuit consumed 700 micro amperes with +/– 0.9V supply voltages.

References:

[1] T. Ishihara, K. Suzuki, S. Suwazono, M. Hirata, and H. Tanigawa, "CMOS Integrated Silicon Pressure Sensor," *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 151-156, Apr. 1987.

[2] W. Jung, *Op Amp Applications Handbook*, Newnes, 2004.

[3] C. C. Enz, E. A. Vittoz, F. Krummenacher, "A CMOS Chopper Amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 335-341, No.3, 1987.

[4] I. E. Opris and G. T. A. Kovacs, "A Rail-to-Rail Op-Amp," *IEEE Journal of Solid-State Circuits*, vol. 31, No. 9, pp. 1320-1324, Jun. 1996.

[5] A. T. K. Tang, "A 3μV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing," *IEEE ISSCC Digest of Technical Papers*, pp. 386-387, 2002.

[6] T. Yoshida, Y. Masui, T. Mashimo, M. Sasaki, and A. Iwata, "A 1V Supply 50nV/√Hz Noise PSD CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 118-121, 2005.

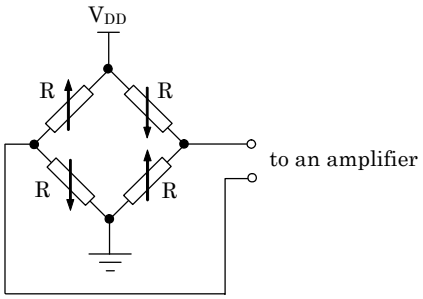


Fig. 1. A general structure of a piezoresistor sensor bridge.

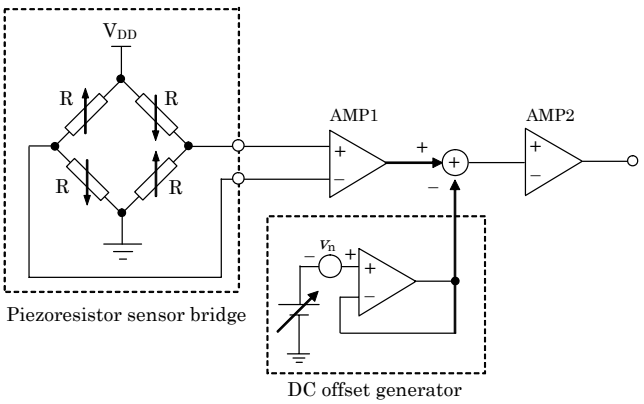


Fig. 2. Sensor-offset cancellation circuit.

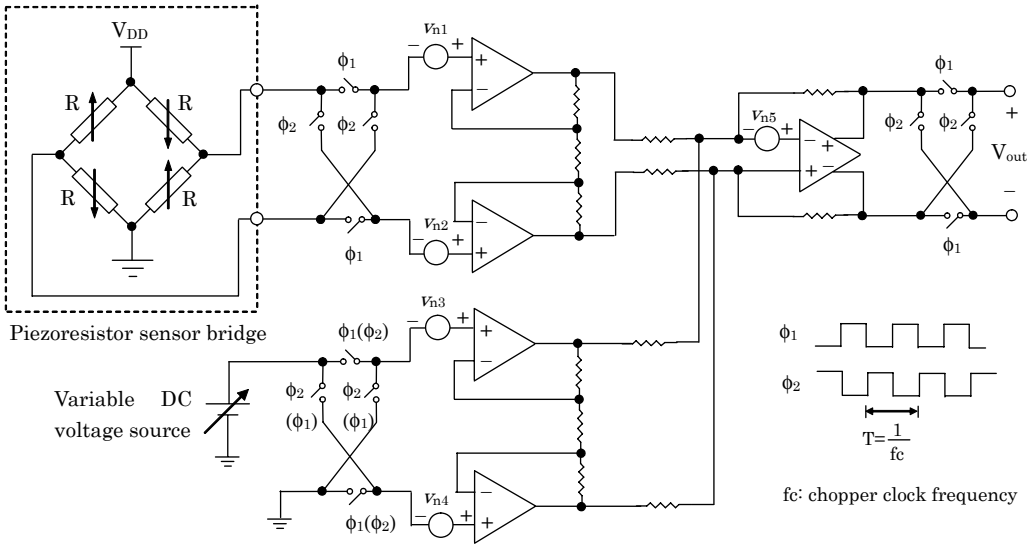


Fig. 3. Proposed circuit for sensor-offset cancellation.

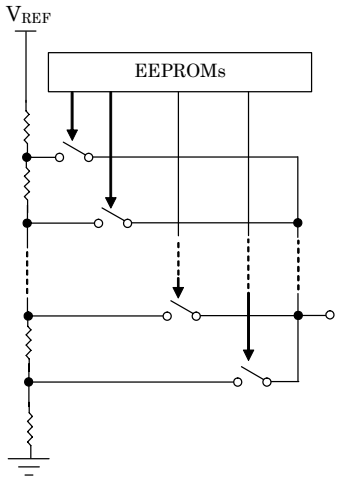


Fig. 4. A variable DC voltage source.

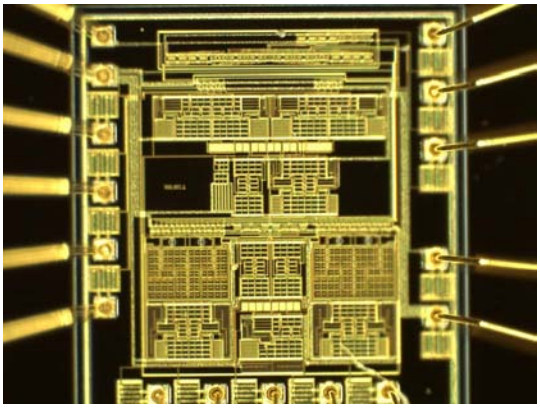


Fig. 5. Chip microphotograph.

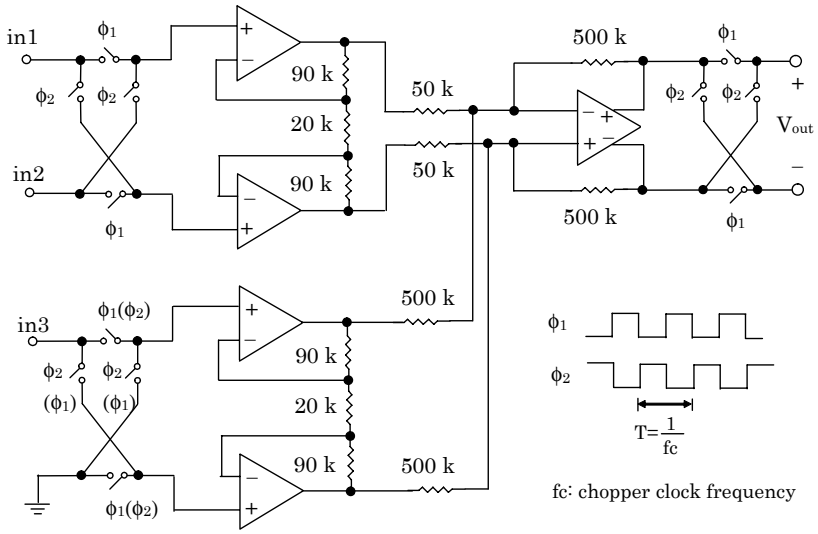
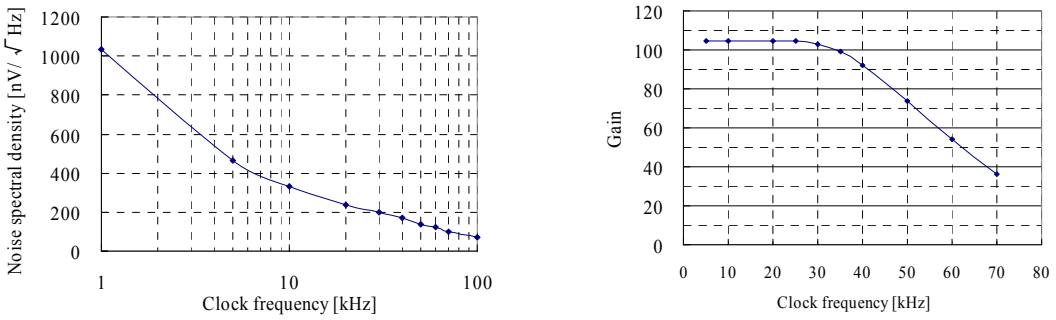


Fig. 6. Signal-conditioning circuit implemented in the chip.



(a) (b)

Fig. 7. Dependence on clock frequency: (a) noise spectral density; (b) gain of the circuit.

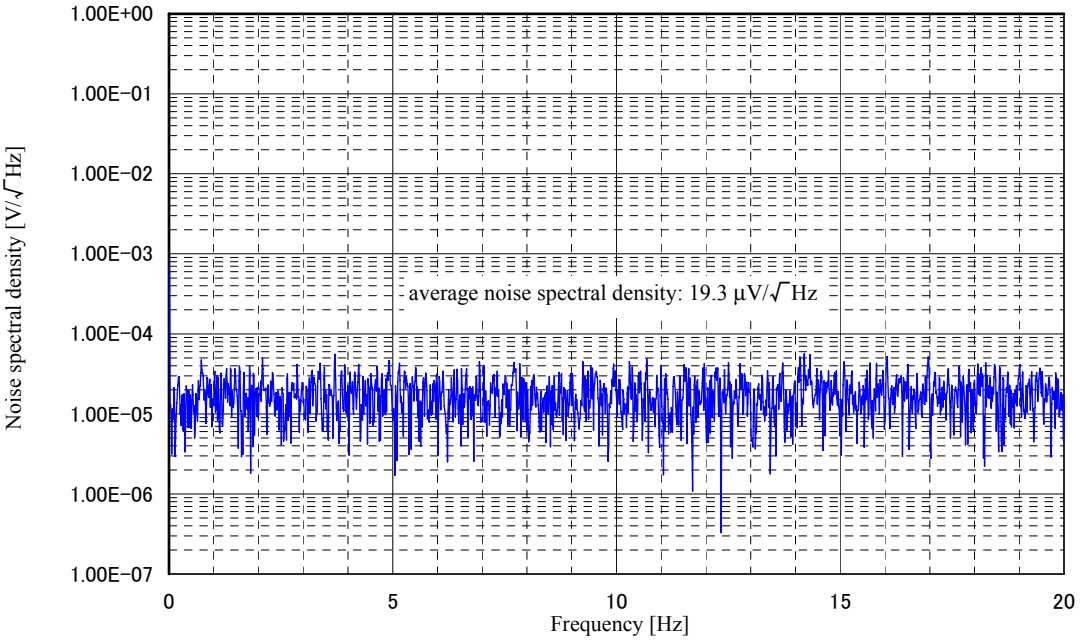
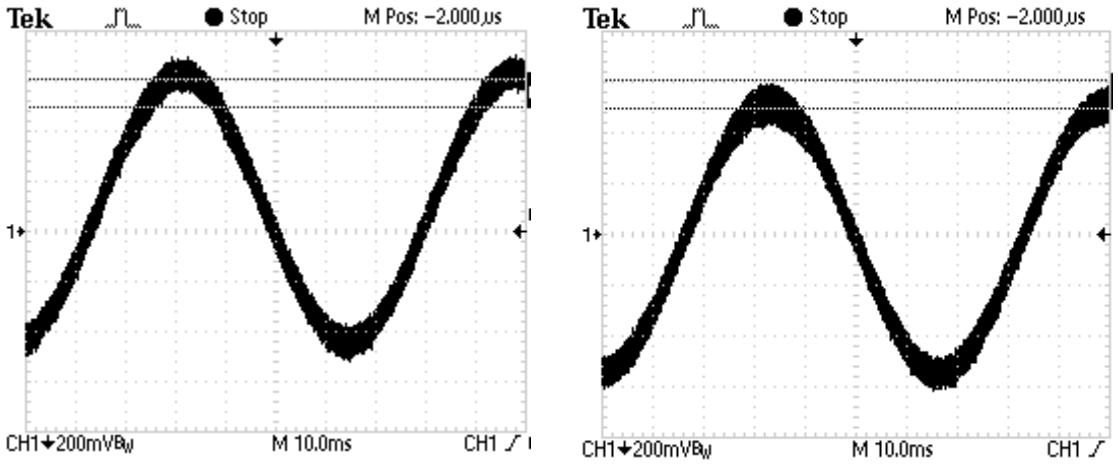


Fig. 8. Measured noise spectral density of the circuit (DC to 20Hz) with a 0-V input (x100 total gain).



(a) (b)

Fig. 9. Measured output waveform for a 15-Hz sinusoidal signal with an amplitude of 10mVpp and with a DC offset of 1mV: (a) in2=in3=0V; (b) in2=0V, in3=10mV.

TABLE 1 Measured performance of the signal-conditioning circuit

Input noise spectral density without offset cancellation (average value from DC to 20 Hz)	193 nV/√Hz
Input noise spectral density with offset cancellation (average value from DC to 20 Hz)	201 nV/√Hz
Chopping frequency	30 kHz
Power consumption	1.26 mW
Supply voltage	+/– 0.9V
Process	1.6 µm CMOS
Die area	1.44 mm^2