ECEN3250 Lab 7: Design of Common-Source MOS Amplifiers

Prelab Assignment

Introduction:

A typical discrete-circuit common-source MOS amplifier configuration is shown in Figure 1. The amplifier is based on the following general considerations:

1. Selection of the DC bias operating point:
    a. The device should be biased in saturation to obtain a large voltage gain
    b. Everything else the same, a larger dc bias current I_D results in lower resistance values R_3 and R_4. As a result, the output resistance is lower, which is desirable because the overall voltage gain is less dependent on the load at the output of the amplifier. Furthermore, larger I_D and lower resistance result in wider bandwidth of the amplifier. However, a larger I_D also results in higher power consumption.
    c. The choice of the dc bias voltage V_S is dictated by a trade-off between the stability of the dc bias operating point with respect to component tolerances and the loss in the available voltage swing at the output of the amplifier. If a larger V_S is selected, the dc operating point is less sensitive to variations in circuit parameters (V_t, K_n, temperature, resistance values). However, a larger V_S implies that the device reaches the triode/saturation boundary at higher v_D, which means that a lower signal voltage swing is available at the output of the amplifier.
    d. It is in general desirable to have a large input resistance, so that the amplifier does not load the signal source significantly. Therefore, it is usually desirable to choose large R_1 and R_2 values.
    e. Once a dc bias current I_D, a dc bias voltage V_S, and R_1 (or R_2, or $r_{in} = R_1 \,||\, R_2$) are selected, the required resistances R_1, R_2 and R_4 can be found.
2. Selection of the drain resistor R_3, the ac coupling capacitor C_1, and the V_S-decoupling capacitor C_2
    a. For a given dc bias current I_D, the choice of R_3 affects the voltage gain, the output resistance, and the available output voltage swing.
    b. To achieve the maximum possible gain, it is desirable to choose R_3 as large as possible. A larger R_3, however, results in larger output resistance, and smaller available voltage swing (the output signal voltage range in which the device stays in saturation)
    c. The achieve the maximum possible output voltage swing, it is desirable to choose R_3 so that the dc output voltage V_O is half-way between the maximum output $v_{O,max} = V_{DD}$ (at the saturation/cut-off boundary) and the minimum output $v_{O,max} = V_G - V_t$ (at the saturation/triode boundary).

d. The ac-coupling capacitor C_1 should be large enough so that the ac signal v_{in} from the signal source is coupled to the gate without attenuation
e. The decoupling capacitor C_2 should be large enough so that the device source is essentially shorted to ground for ac signals. Removing C_2 results in a significantly lower gain, which however, also becomes less dependent on device parameters.

The purpose of this prelab assignment is to design a common-source amplifier, which will then be tested experimentally in the lab.

Prelab assignment:

Given a ZVN2106 NMOS transistor and VDD = 15 V, design the amplifier of Figure 1 so that:

- I_D = 1 mA
- V_S = 2 V
- r_{in} = 100 KΩ
- maximum possible output voltage swing is available

Use $C_1 = C_2 = 1$ μF. Choose all resistance values, then compute the voltage gain, the output resistance, and the available output voltage swing.

Use PSpice .ac and .tran simulations to (a) verify the dc operating point, (b) find the amplifier's magnitude response, and (c) verify the result found for the available output voltage swing.

Have the complete prelab work ready *at the beginning* of the lab session.

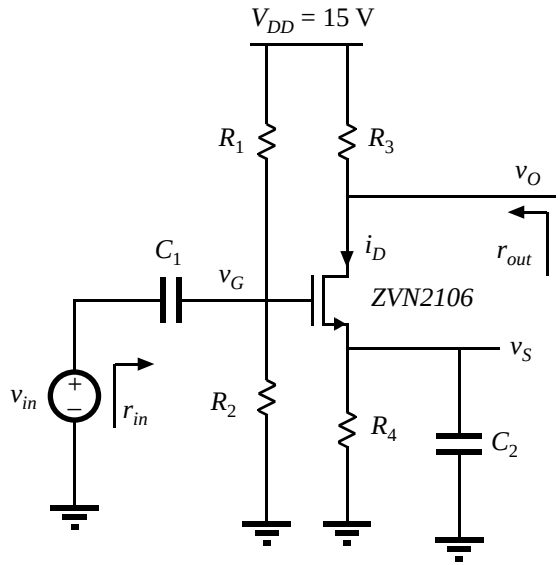
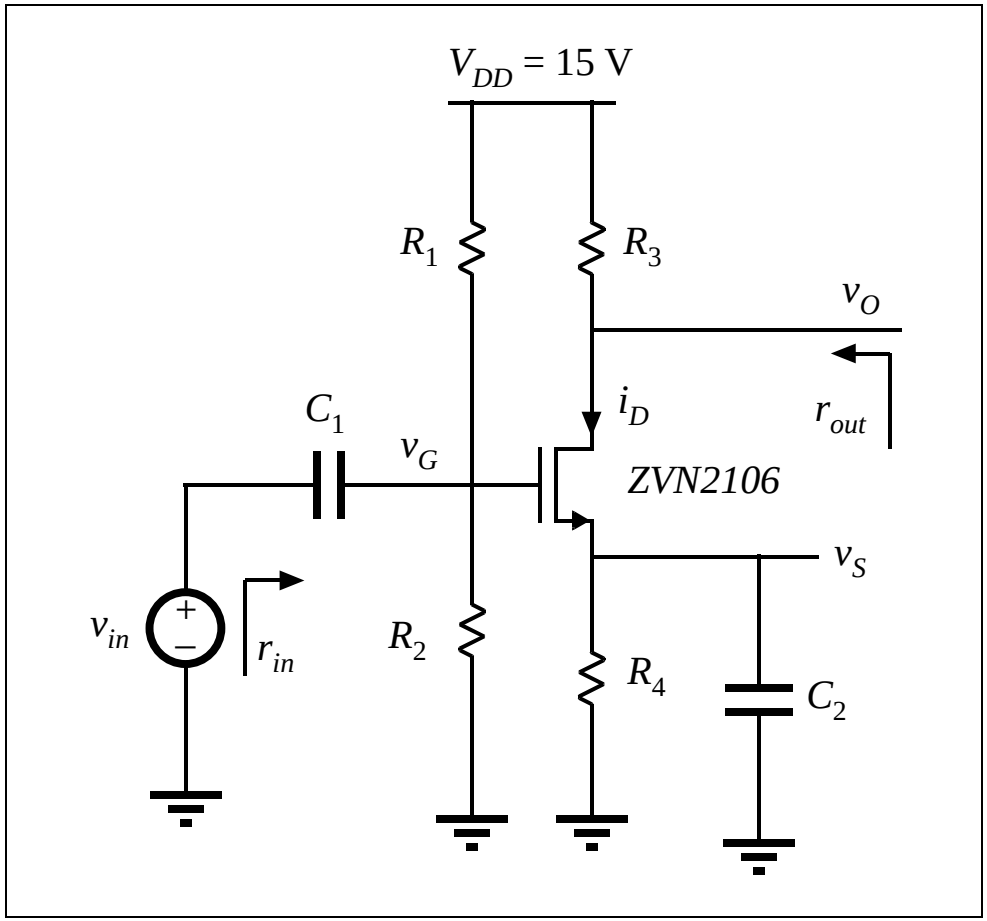


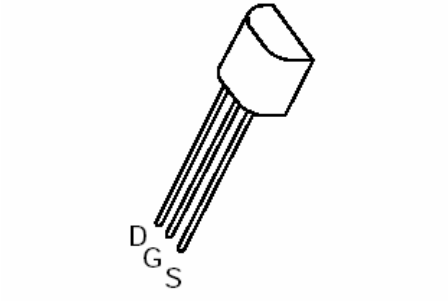
Figure 1: Discrete-circuit common-source amplifier.

ECEN3250 Lab 7
Design of Common-Source MOS Amplifiers

ECE Department
University of Colorado, Boulder

1. Discrete-circuit common-source amplifier





Design specs:

- I_D = 1 mA
- V_S = 2 V
- Maximize available output voltage swing
- $C_1 = C_2 = 1\ \mu F$

1. Experiments and post-lab report

a) Using your prelab results, construct the amplifier. In the report, include the analysis leading to the selection of the resistance values, and a complete labeled circuit diagram of the amplifier.

b) Check the DC bias operating point: measure and report V_S, V_G, I_D, V_O. The measured values for V_S and I_D should be within 10% of the specifications. Comment on the results.

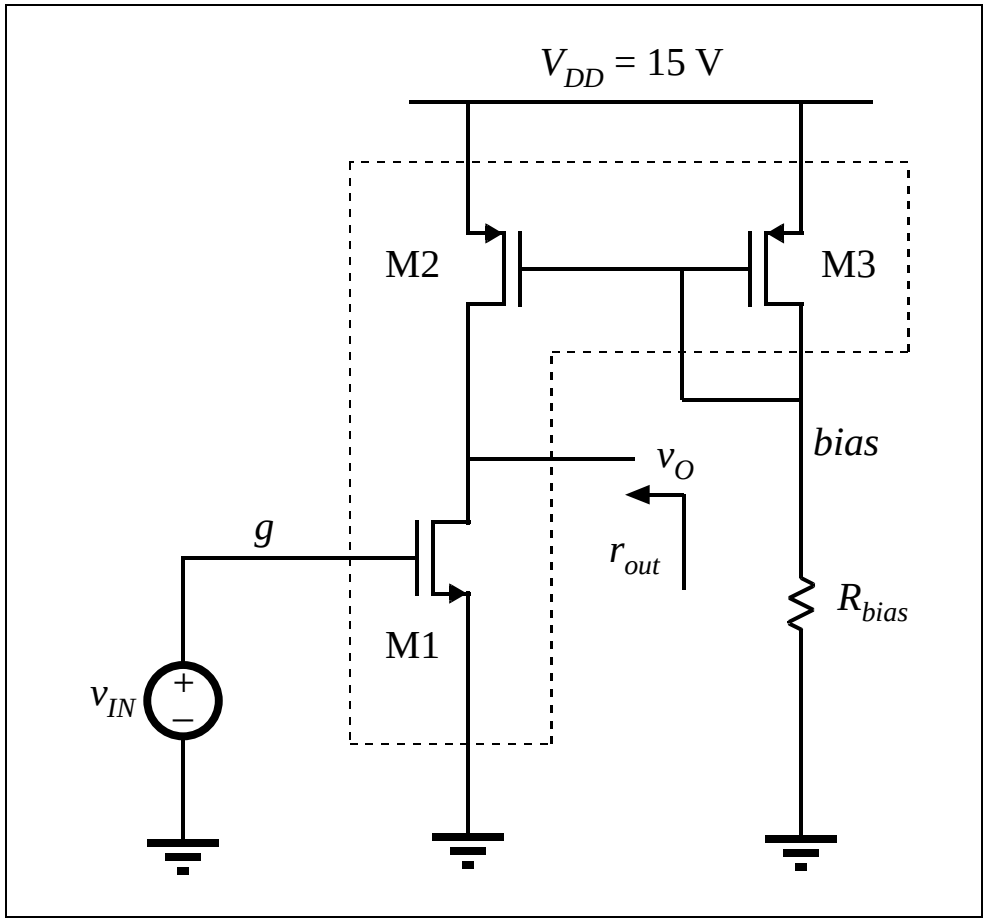
c) Use the lab signal generator to produce a sinusoidal waveform as the input signal v_i. Let v_{ipp} be the input peak-to-peak signal amplitude, and v_{opp} be the output peak-to-peak signal amplitude. Adjust the input signal frequency to 1 KHz and v_{ipp} so that v_{opp} = 1 V. Measure and report the gain $|A| = v_{opp}/v_{ipp}$ and compare to the values obtained by analysis and by simulation. Comment on the results.

d) By increasing v_{ipp}, find and report the maximum output voltage swing $v_{opp,max}$ before significant distortion is observed in the output signal. Compare to the maximum voltage swing obtained by analysis. Sketch and label the waveforms $v_i(t)$, $v_G(t)$ and $v_O(t)$ over one period of the waveforms for the input $v_{ipp,max}$ corresponding to $v_{opp,max}$ and for 2 $v_{ipp,max}$. Comment on the results.

e) Readjust v_{ipp} so that v_{opp} = 1 V at 1 KHz. Measure the magnitude response of the amplifier by sweeping the signal frequency and measuring $|A|$ as a function of frequency. Express $|A|$ in dB. Use a printout of the amplifier's magnitude response obtained by simulation to plot the measured magnitude response data. Compare the lower and upper bandwidth limits (frequencies where the magnitude response is 3dB less than the gain in dB at 1 KHz). Comment on the results.

f) Remove C_2 from the circuit. How do the results for the mid-frequency gain, and the output voltage swing change? Explain in the report.

2. Integrated-circuit common-source amplifier



Design specs:

- Use NMOS and PMOS devices from the CD4007 CMOS integrated circuit

- Small-signal voltage gain:

  $A = v_o/v_g$

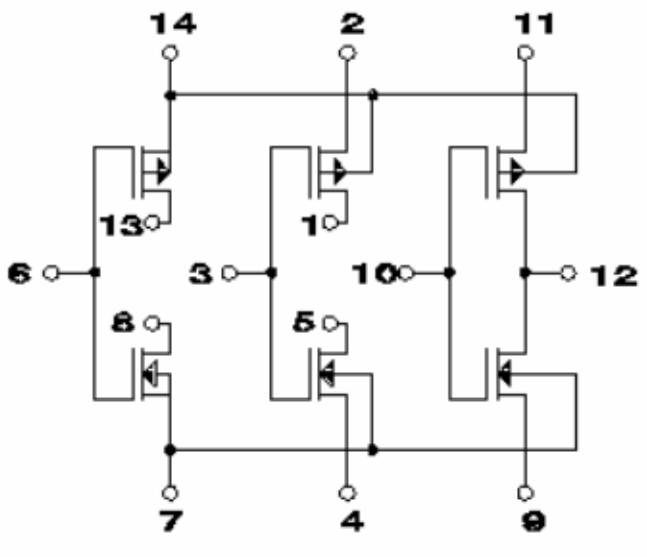
  is **–50** (+/- 20%) at the DC bias operating point where

  $V_O = V_{DD}/2 = 7.5\text{V}$

Integrated-circuit common-source amplifier with active load

CD4007 CMOS integrated circuit

- CD4007 includes two NMOS/PMOS transistor pairs and a CMOS inverter
- Power supply for the IC:
  - Pin 14 should be connected to VDD
  - Pin 7 should be connected to ground
  - Do not forget to include power supply decoupling capacitors



PSpice models (from 3250.lib library):

```
*-------------------------------------------------------------------------------
* N4007 (NMOS on CD4007 CMOS integrated circuit)
*
.model N4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6
+                          Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p N=1)
*-------------------------------------------------------------------------------
* P4007 (PMOS on CD4007 CMOS integrated circuit)
*
.model P4007  PMOS (Kp=500u Vto=-1.5 Lambda=0.04 Gamma=0.6
+                          Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=4.0p Cbs=4.0p Pb=.8 Cgso=0.2p Cgdo=0.2p Is=16.64p N=1)
*
*-------------------------------------------------------------------------------
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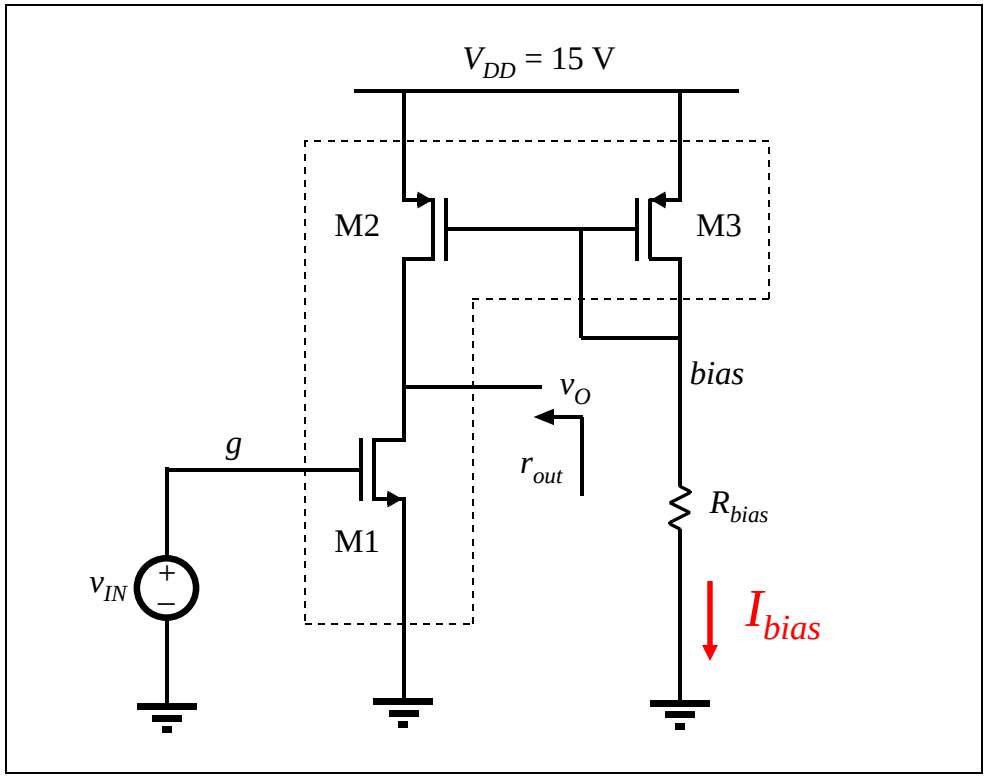
For PSpice simulations, do not forget to download the library file 3250.lib to your working folder

2.1 Analysis and design



At a DC operating point where both M1 and M2 are in saturation, the small-signal voltage gain is:

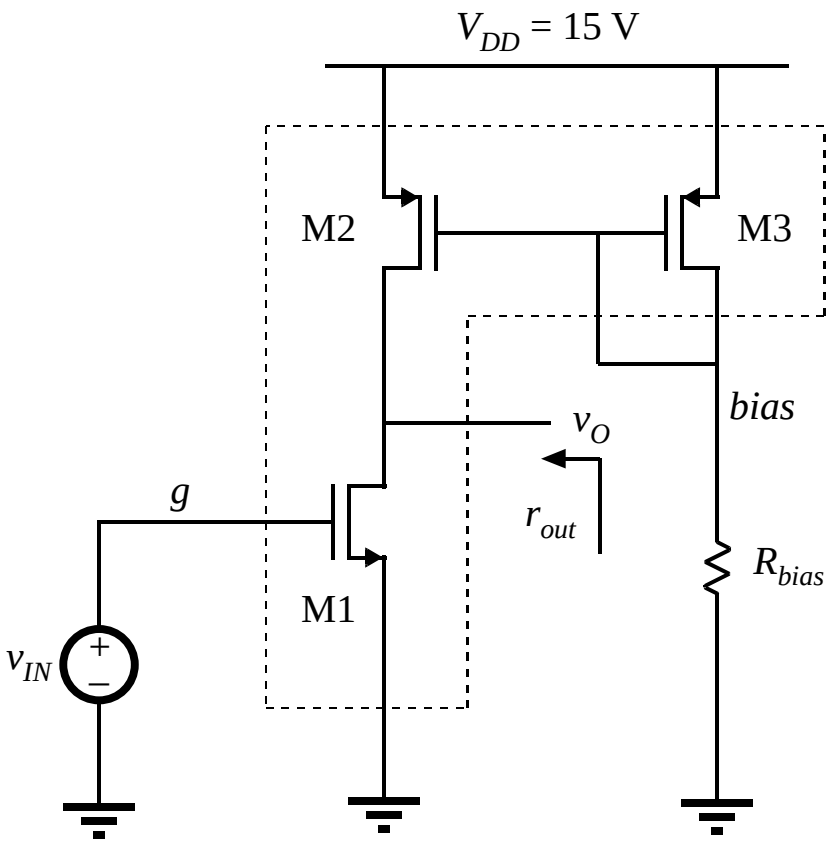
$$A = v_o/v_g = -g_{m1}(r_{o1} \parallel r_{o2})$$

The transconductance g_{m1} and the device output resistance r_{o1} and r_{o2} depend on the bias current I_{bias} and the device parameters. In the report, derive the following expression for A:

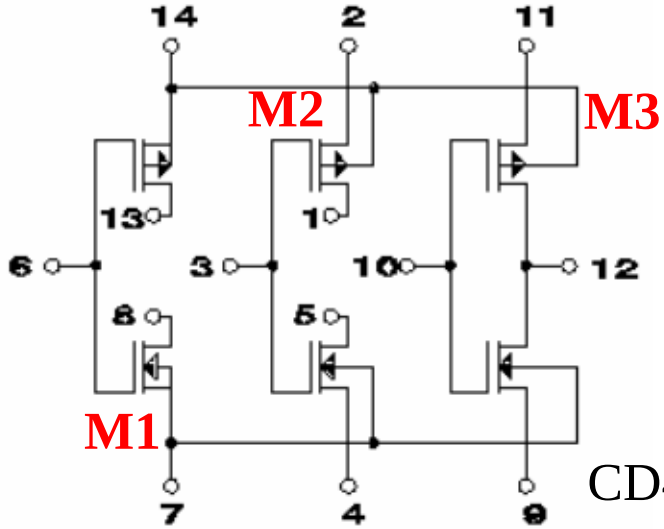
$$A = \frac{v_o}{v_g} = -\frac{2\sqrt{K_n}}{\lambda_n + \lambda_p}\frac{1}{\sqrt{I_{bias}}}$$

- Design: using the parameters from the PSpice NMOS and PMOS models, and the expression for A, choose I_{bias} and then choose R_{bias} so that the gain of –50 is obtained. Document the design in the report.
- Use PSpice to check your design: plot the dc transfer characteristic and find the slope of the characteristic around the point where V_O=7.5 V. Report the results.

2.2 Experimental CMOS amplifier



Integrated-circuit common-source amplifier with active load



CD4007

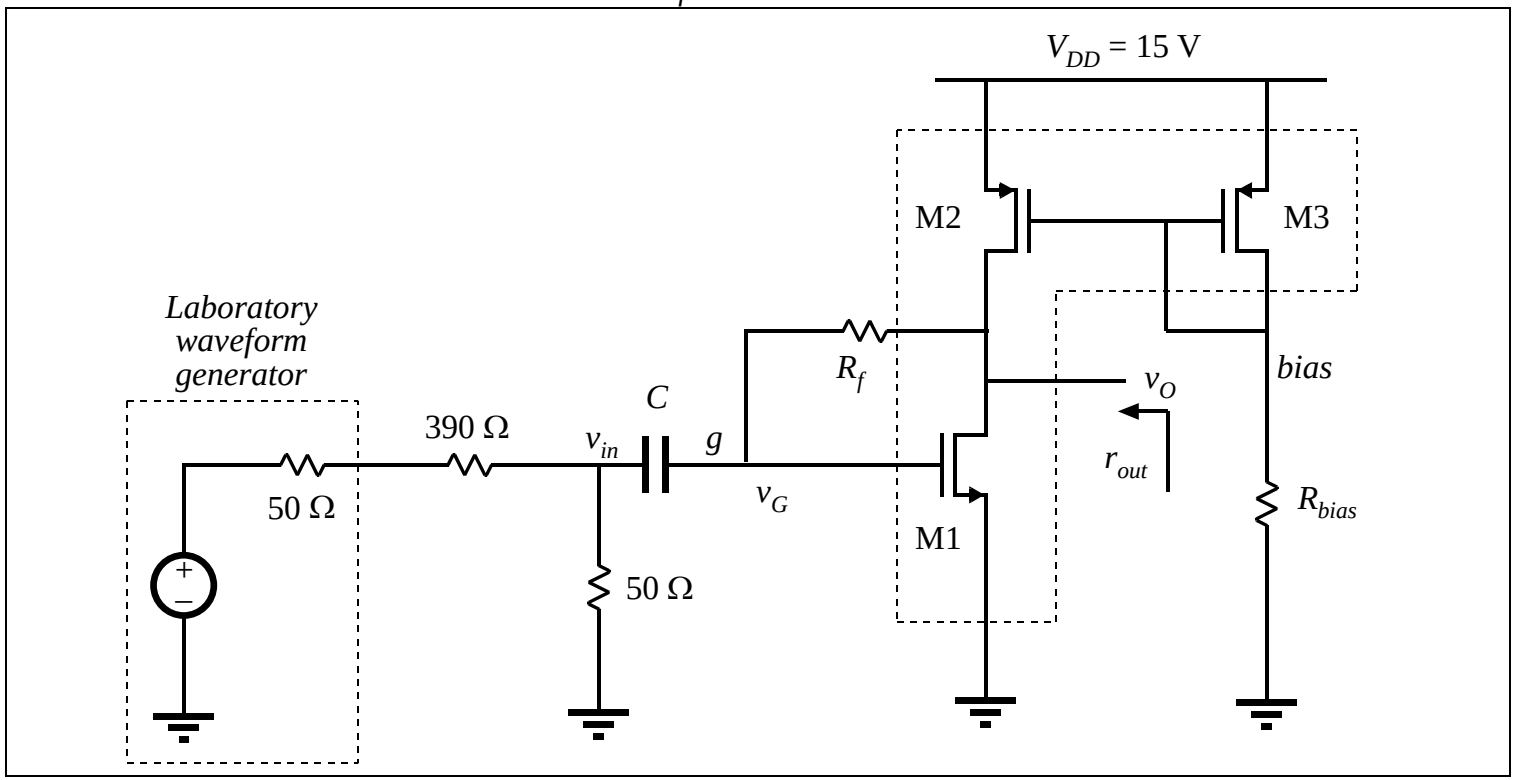
- Use the amplifier circuit diagram and the CD4007 chip pinout shown on this page to figure out how to connect the amplifier.
- Use the bench variable DC voltage source as v_{IN}
- Do not forget DC decoupling capacitors for V_{DD}
- Unused CD4007 transistors can be left open
- R_{bias} is an external discrete resistor; start with the value you found in the design (page 3)
- The report should include a circuit diagram that shows how you made all connections around CD4007

2.3 DC Transfer Function Experiment

1. Use the bench variable DC source to measure the DC transfer characteristic of the amplifier: V_O as a function of V_{IN}. Find the gain A from the slope of the DC transfer characteristic around the operating point where V_O = 7.5 V.
2. Modify the design (i.e. change R_{bias}) to get the required gain of –50 (+/- 20%)
3. Report the experiment, and comment on the results. Compare the experimental results to the analysis and simulation.
4. Is it necessary to update the PSpice model parameters? If so, change the model parameters in 3250.lib, and use the updated models in the remaining parts of the lab. It may be necessary to perform separate experiments (as in Lab 5) to measure V_t and K parameters of the NMOS and PMOS transistors on the CD4007 chip.
   - In the report, describe how you updated the PSpice models.

2.4 Amplifier test with AC signal input

- Since the actively-loaded CMOS common-source amplifier has large gain, setting up the DC operating point so that both M1 and M2 stay in saturation (and V_O = VDD/2 = 7.5V) is difficult. Compared to the discrete-circuit amplifier where R4 served the purpose of stabilizing the DC operating point, no such DC stabilizing mechanism exists in the active-loaded CMOS amplifier. As a result of even small variations in V_{IN} (or temperature or device parameters) the output voltage can easily drift toward VDD or toward 0.
- A common technique to stabilize the DC operating point in a high-gain amplifier is to use negative feedback as shown below. Use R_f = 1 MΩ and C = 1 μF.



2.4 Amplifier test with AC signal input

Your task is to perform the experiments, simulations and analyses necessary to complete the report:

1. In the report, answer the following questions: what is V_G and V_O in this circuit? Do all transistors operate in saturation? Is the DC operating point very sensitive to variations in temperature or parameter values? Why or why not? Do your observations in the lab match your conclusions?

2. Use the lab signal generator at the minimum output voltage amplitude (100 mVpp), and a voltage divider (390 Ω and 50 Ω) to attenuate the input signal as shown in the circuit diagram. This will reduce the input to about v_{ipp} = 10 mV.

3. Use the oscilloscope to check the signal gain $A = v_{opp}/v_{ipp}$ at the signal frequency 1KHz. Sketch the scope waveforms $v_{IN}(t)$, $v_G(t)$, and $v_O(t)$.

4. Measure the magnitude response of the amplifier and find the lower and the upper bandwidth limits. In the report, document the experiment and compare the measured magnitude-response results with .ac PSpice simulation results.

5. Modify the circuit so that the DC operating point of the amplifier with the feedback resistor R_f moves to the desired point $V_O = V_{DD}/2 = 7.5$ V. *Hint:* consider adding a resistor from gate of M1 to ground.

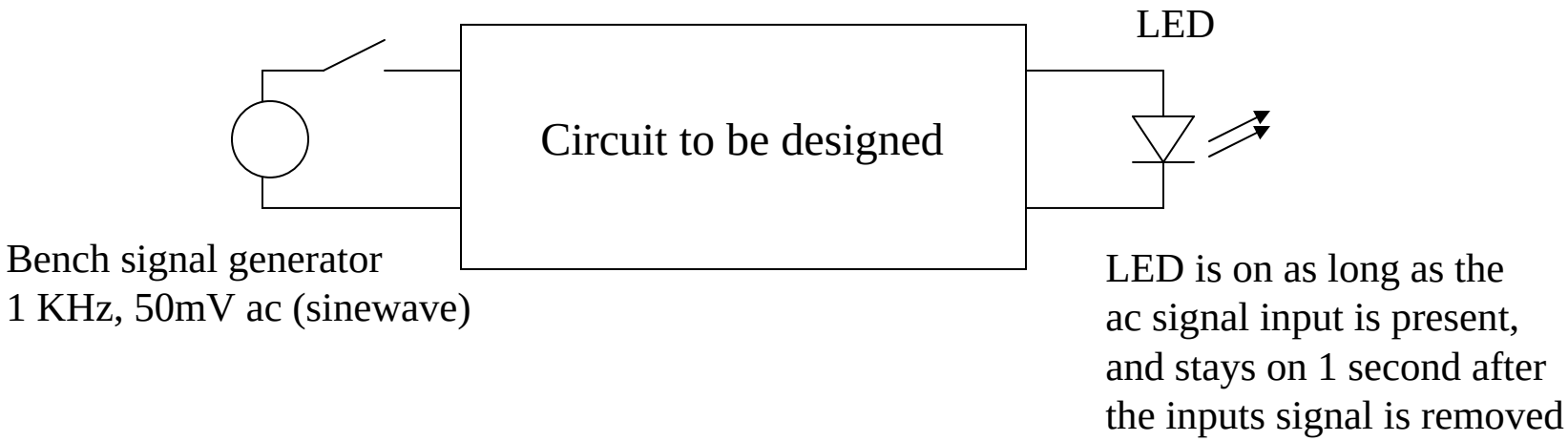
6. In the report, explain how the modified circuit works. Does the circuit modification affect the signal gain? What is the output voltage swing? Describe the experiment you performed and show the experimental results verifying the output voltage swing of the amplifier.

Lab 7 extra-credit: voice-activated switch

Introduction

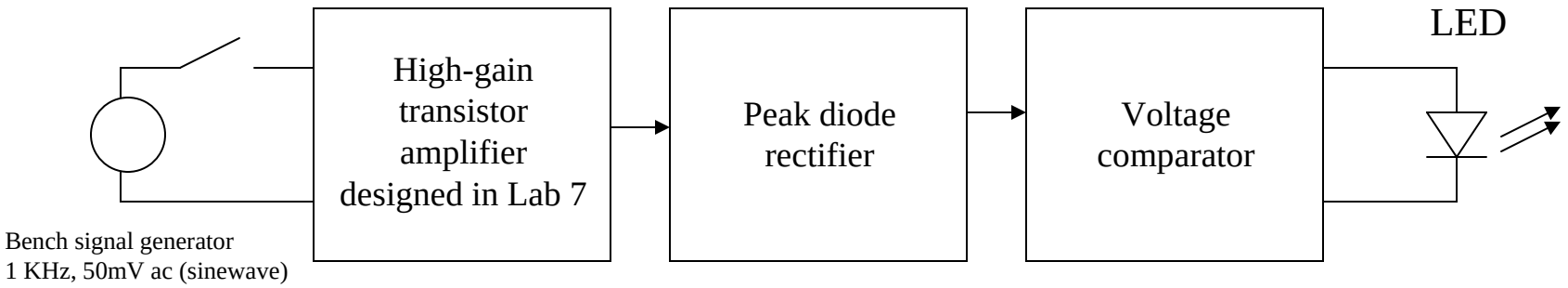
It is desired to design a circuit to turn on a switch when a signal coming from a microphone is detected. The switch should stay on as long as the signal coming from the microphone is present, and should turn off after 1 second of silence.

Your task is to design the voice-activated switch circuit and demonstrate its operation using the test setup shown below. Use the bench sinewave generator set to 50mV amplitude, 1 KHz frequency to model the signal coming from the microphone. Use a light-emitting diode (LED) to indicate the on/off state of the switch.



Design hints and extra credits

A conceptual block diagram of the voice-activated switch circuitry is shown here:



The high-gain MOS transistor amplifier you designed in Lab 7 can be used to increase the amplitude of the input ac signal. No credit will be given for other circuit implementations of the amplifier.

A peak diode rectifier can be used to generate a dc voltage (with small ac ripple) proportional to the amplified ac signal amplitude.

A voltage comparator (you can use the LM311 comparator to design this part) can be used to detect presence of the increased dc voltage at the output of the peak diode rectifier when the ac input is applied, and to turn on the LED at the output

Up to 5 extra-credit points will be awarded for a complete, documented circuit design and successful demonstration of the circuit operation.