A Low-Power Transponder IC for High-Performance Identification Systems

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Abstract—**A novel integrated circuit for a batteryless transponder system is presented. Batteryless transponders require contactless transmission of both the information and power between a mobile data carrier and a stationary or handheld reader unit. The operating principle of this system gives a superior performance in reading distance due to separation of the powering and data transmission phases—compared to systems with continuous powering and damping modulation [9], [12]. This paper describes the function of the transponder IC and the circuit design techniques used for the various building blocks.**

I. Introduction

THERE is a growing interest in electronic identification systems in many different fields of application since data can be collected and managed very easily by computer systems. Radio frequency identification (RFID) systems have additional advantages like contactless reading/writing over large distances, robustness and reliability under difficult environmental conditions (dust, humidity, heat, cold), and, last but not least, ease of use.

Examples of major application fields for the RFID systems are lifestock management, security systems and access control, and work tracking for factory automation [2].

The Texas Instruments Registration and Identification System (TIRIS) presented here uses a batteryless transponder working at 134.2 kHz (Fig. 1). Data transmission is done by means of the frequency-shift keying (FSK) technique.

The system works in half-duplex mode. First, energy is transmitted to and stored in the transponder. Second, the data telegram is sent back to the reader unit. This technique allows greater reading distances over simpler receivers that use full-duplex systems [1], [9].

The transponder consists of an LC tank, a supply capacitor, and the transponder chip. The LC tank L_R and C_R serves as an RF interface to receive energy from the reader unit and to send back data. The transmission of data bits by means of a certain format frame will be referred to as a "telegram" in this paper. The supply capacitor C_L stores the energy during the charge-up phase and delivers the current during the telegram phase.

II. Functional Block Diagram and Operating Principle

The IC block diagram (Fig. 2) explains how the complete transponder operates.

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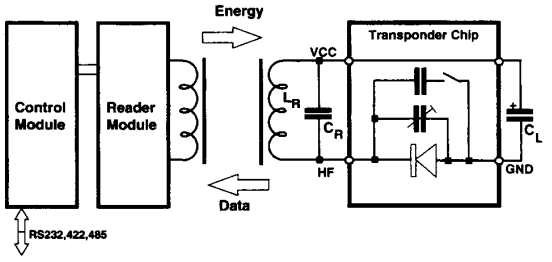

Fig. 1. Transponder system.

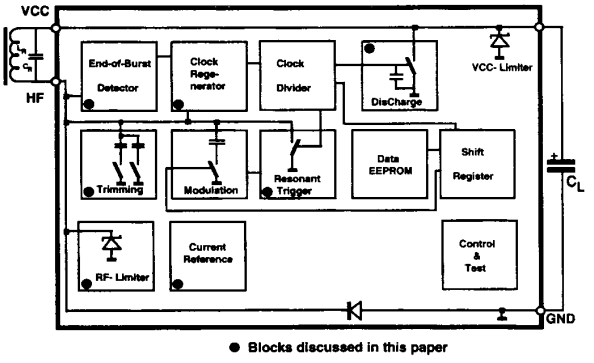

Fig. 2. Transponder block diagram.

A. Energy Transmission and Storage

The carrier frequency is received by the LC tank and the rectifier (n^+ to substrate diode) charges up the supply capacitor. Due to the large variation of the distance to the antenna, the transponder has to operate over more than three orders of magnitude of field strength (Figs. 3(a)–(b)). This means that the induced voltage can reach several hundred volts.

In order to avoid electrical overstress of the circuits, the chip contains two voltage limiter functions: one for the RF voltage, and another one for the supply voltage—with a limiter voltage of about 14 and 6.5 V, respectively. This is especially important over very small distances where strong transformer coupling occurs.

The trimming block ("Trimming") allows optimal tuning of the LC tank with on-chip capacitors so that the maximum possible transmission distance can be achieved.

B. Telegram Generation

The End-of-Burst-Detector generates a start signal for the control logic as soon as the reader stops the RF-charge-up

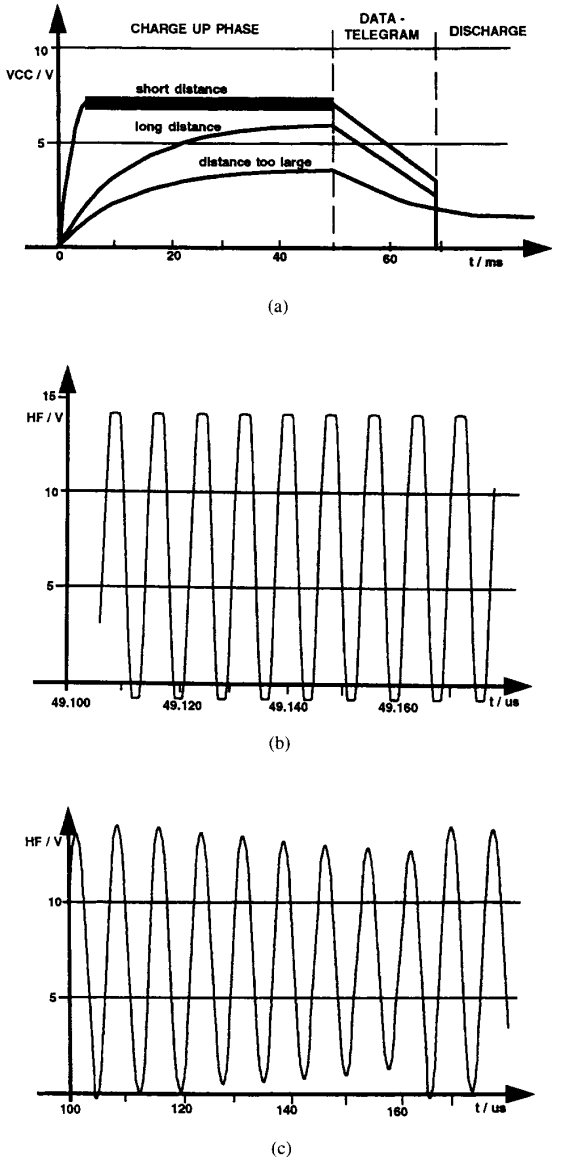

Fig. 3. Waveforms during charge-up and transmission.

burst. This start signal activates all the circuitry required for the telegram generation which has been in power down mode during the charge-up phase.

First, the clock has to be extracted by the "Clock Regenerator." For the telegram transmission, three different functions have to be provided.

- Loading the EEPROM data into a shift register and shifting the data with a specific serial format.
- Keeping the oscillation of the LC tank alive by synchronously triggering the LC tank (like plucking a guitar string, see Fig. 3(c)).
- Transmitting the data back to the reader unit by means of FSK. This is achieved by switching a capacitor in parallel with the LC tank if a "1" is transmitted (block "Modulation").

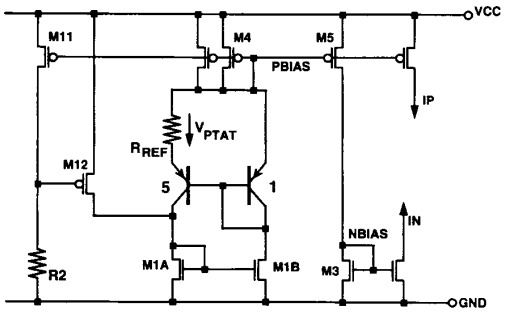

Fig. 4. Current reference.

C. End of Operation

After the telegram has been sent out, the whole circuit is reset and the supply capacitor is discharged. This allows both a well-defined retriggering of the transponder and a better reading selectivity if several transponders are in the field.

III. Transponder IC Building Blocks

In this section, various analog building blocks required for the transponder operations will be described. The main concern for these building blocks is the ability to achieve *lowest possible current consumption.*

A. Current Reference—Bias Generator

A low current bias generator is needed for the various analog functions.

One of the main aspects of the bias generator is that its own current consumption should be as low as possible in order to have an overall low current consumption for the entire chip.

Fig. 4 shows the schematic of the current reference circuit employed for this purpose. A known *PTAT* voltage reference [3] is formed from two lateral bipolar p-n-p transistors (obtained using n-well CMOS technology [4]) and an n-channel current mirror. This *PTAT* voltage appears across a reference resistor. The bipolar transistor ratio of 5 yields a *PTAT* voltage of

$$V_{PTAT} = U_T \times \ln 5 \simeq 42\,\mathrm{mV}. \tag{1}$$

So the current through the reference resistor is about 150 nA at a resistor value of 280 kΩ. The total reference current through $M4$ is then

$$IR = 2 \times IR_{\mathrm{REF}} = 300\,\mathrm{nA}. \tag{2}$$

Another current mirror $M4$ and $M5$ drives the current into $M3$ so that bias voltages for both current sources *(PBIAS)* and current sinks *(NBIAS)* are available. $M11, M12$, and $R2$ are added to secure proper startup of the bias generator.

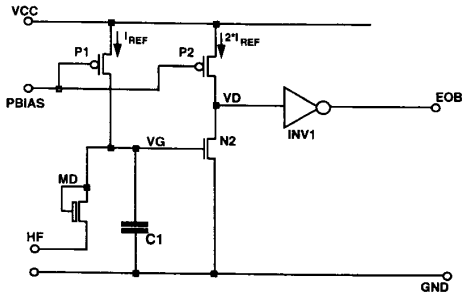

Fig. 5. End-of-burst-detector.

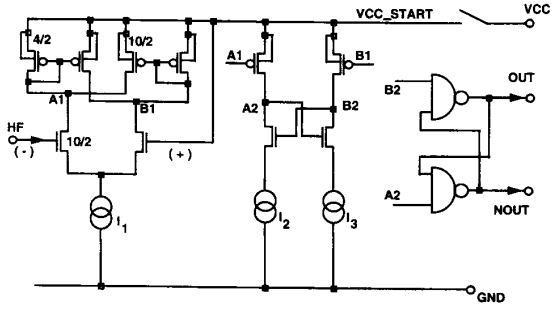

Fig. 6. Clock regenerator.

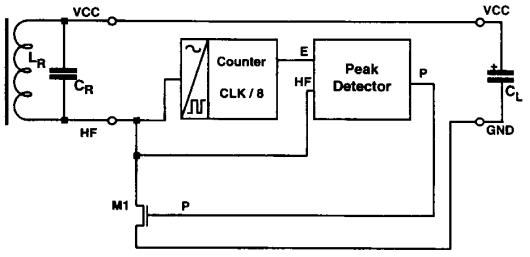

Fig. 7. Transponder oscillator.

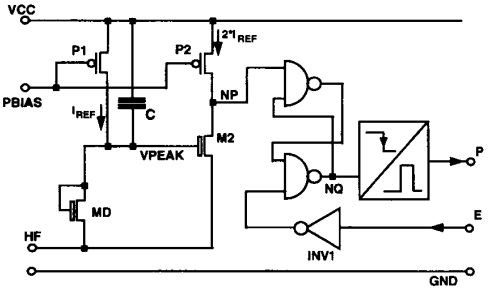

Fig. 8. Peak detector.

B. End-of-Burst-Detector

Capacitor C_1, in Fig. 5, is discharged by signal HF via diode MD, when $HF < 0$ (charge-up). MD is a "high-voltage" (HV) type transistor with poly2-gate and thicker gate oxide. When the burst ends, MD turns off, C_1 is charged by I_{REF}, and $N2$ is turned on if voltage VG has reached the threshold of $N2$. In consequence, the output EOB becomes high and the remaining transponder blocks are activated. An improved version (with hysteresis) can be found in [11].

C. Clock Regenerator

The task of the clock regenerator is to amplify a sinewave of about a few hundred millivolts peak-to-peak to a full swing (rail-to-rail) square wave with short rise and fall times independent of the input signal amplitude. Its own current consumption should be as low as possible. The clock regenerator circuit diagram is shown in Fig. 6. The whole clock regenerator circuit consists of three stages.

For the input stage, an n-channel input differential amplifier with a current source of 1.5 μA has been selected using cross-coupled p-channel loads. The ratio of the p-channel devices is 1 : 2.5 so that positive feedback is achieved [5].

The second stage uses a latch-type differential stage. The two p-channel input transistors operate with the current sources $I2$ and $I3$ as loads. The transistors $M7$ and $M8$ switch the current sources so that current only flows during transition phases.

Finally, a NAND latch is used as the third stage in order to perform additional edge shaping.

The circuit is connected to VCC by means of a switch (PMOS) which is controlled by the start signal EOB, mentioned in Section II-B.

The whole clock regenerator consumes about 2.5 μA @ 5 V at a frequency of 134 kHz and delivers square wave with 20 ns rise and fall time.

D. Transponder Oscillator and Peak Detector Circuit

During the transmission of its telegram, the transponder uses its own LC tank as an oscillator reference [8]. Fig. 7 shows the principle of the oscillator. During oscillation, the LC tank loses energy, mainly through the lossy inductance L_R. In order to maintain the oscillation, some energy is injected into the LC tank by means of recharging C_R; this charging is activated by switch $M1$ and signal P, which is called the pluck pulse. This pulse is generated every eighth period of the HF sine wave so that the refresh optimally supports oscillation at the minimum point of the sinewave and no unwanted loss of energy occurs.

A special circuit has been designed for the detection of the minimum point of the sinewave (Fig. 8) [6]. Current source I_{REF} and capacitor C determine the time for charging up node $VPEAK$. During the positive half of the sinewave HF, the potential at $VPEAK$ ramps up (Fig. 9) and diode MD (HV) is off. When HF decreases and reaches a potential of $VPEAK - VT$, MD turns on and $M2$ (HV) as well (current mirror); a low-pulse occurs at NP and the flip-flop is reset if it was preset by enable signal E previously. The falling edge at NQ is then differentiated and the pluck pulse

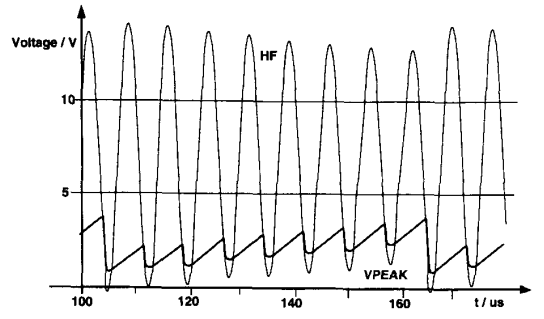

Fig. 9. Voltage in peak detector during transmission (pluck every eighth period).

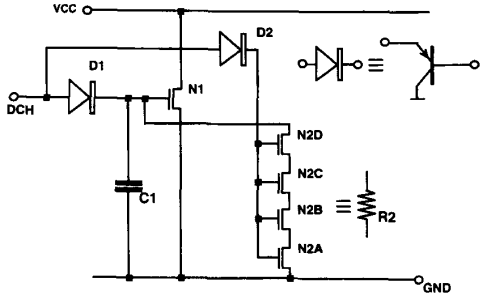

Fig. 10. Discharge circuit.

P is generated, which has a length of about 100 ns. With this method, detuning of the resonant frequency is minimized.

E. Discharge Circuit

After the transmission of a complete telegram, the transponder circuit resets itself completely and discharges the supply capacitor. As already mentioned, this should minimize possible interference if more than one transponder is within the reading range of the reader's antenna.

The discharge circuit (see Fig. 10) consists basically of a large n-channel transistor ($N1$) which is driven from the reset logic. In order to maintain the on-state of the transistor and to secure a complete discharge of the supply capacitor, the gate is controlled via a diode ($D1$). With an additional capacitor $C1$ and a large resistor value formed by the n-channel transistor $N2$, a well-defined time constant can be realized for proper discharge. There is also a maximum time for activation of the discharge circuit to allow repowering of the transponder in continuous burst mode after a few milliseconds. The gate of $N2$ is also activated by another diode ($D2$). Discharge of this gate is not necessary.

F. RF Limiter

In the near distance operation, the voltage across the resonant circuit can reach several hundred volts. Therefore, it is necessary to limit the voltage in order to avoid any damage of the integrated components. Fig. 11 shows the circuit diagram of the so called RF limiter.

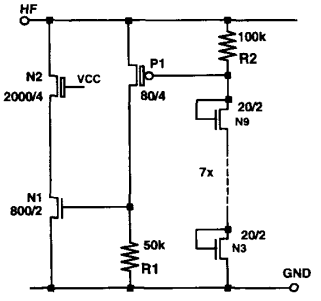

Fig. 11. RF limiter.

The chain of seven n-channel transistors acts as a "zener diode." As soon as the RF voltage exceeds the sum of all thresholds, current starts to flow through resistor $R2$. When the voltage drop across $R2$ reaches the threshold of transistor $P1$ (HV), this transistor will switch on, and in turn activates the n-channel transistor $N1$ which carries most of the current.

Due to the half-wave rectifying principle, the limiter has to clamp at 2 × the supply voltage; therefore, it is necessary to add another transistor $N2$ (HV) in a cascode connection with the gate tied to VCC in order to share the voltage between the two transistors as equally as possible. Otherwise, hot electrons would trigger the lateral n-p-n and cause a severe snap back, leading to unwanted oscillations and parasitic effects of the LC circuit.

The limiter circuit has been designed for a maximum current of 50 mA. However, the limiting factor in continuous operation will be the maximum allowed power dissipation which mainly depends on the package and/or the application. For example, for implanted transponders, the temperature increase of the transponder needs to be limited to a few degrees Celsius.

IV. On-Chip Trimming System

The key to obtaining large reading distances is through the proper tuning of the transponder's LC tank. The selection of external components with tight tolerances is costly because a tight frequency tolerance is needed. Hence, an on-chip trimming circuit/method was chosen by means of a binary weighted capacitor network with 7 b resolution.

Fig. 12 shows one stage of the trim network [7]. The circuit consists of two EEPROM transistors $EE1x$ and $EE2x$ working as nonvolatile switches, and two transistors $M1x$ and $M2x$ for test purposes. The lower transistors $EE1x$ carry the trimming state: if the capacitor has to be activated, the EEPROM transistor is programmed into depletion mode; if the capacitor has to be switched off, $EE1x$ is erased. The upper transistors $EE2x$ are always programmed in depletion mode—they have the task to protect the $EE1x$ from too high voltage at node $D1x$ if $EE1x$ in the off-state.

The on- and off-states of $EE1x$ and $EE2x$ are tested by feeding a certain current I_{IN} via $M1x$ into node $D2x$, and sensing the voltage at node $D2x$ by means of $M2x$. After assembly of L_R, C_R, and C_L, the transponder oscillator

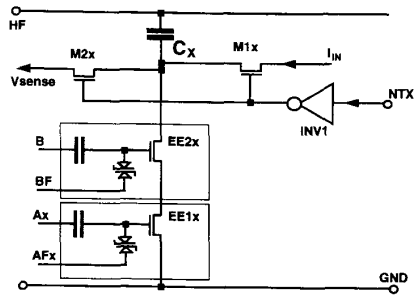

Fig. 12. EEPROM trim capacitor circuit.

is triggered, the resonance frequency is measured, and the seven trimming switches are programmed accordingly until the frequency is within the specified range.

V. Results

The transponder presented in ths paper allows identification data to be read over a distance of up to 2 m, depending on the size of the antenna and the allowable field strength. A key element to achieve this performance is the low-power consumption of the transponder IC. A total current consumption of about 0.5 μA has been achieved in the charge-up mode (current reference and end-of-burst-detection active), while the current in the active mode has been kept under 5 μA.

In addition, the on-chip trimming of the transponder allows optimization of reading performance at low cost. The chip operates within a temperature range of -40 to 125°C and a supply range of 7–3 V.

If more than one transponder enters the electromagnetic field at the same time, the one that is read is the one closest to the reader's antenna. A spacing of about 5 cm is sufficient for transponders with a small ferrite coil of 18 mm length.

A chip photograph is shown in Fig. 13. On the right side, the ten rows of 8 b of EEPROM memory can be seen easily. On the lower left side, the RF limiter is located. On the upper left side, the oscillator circuit, the clock regenerator, and the current reference circuit can be found. The modulation capacitor is split into two parts at the top of the chip. The trimming circuit at the middle left side consists of 32, 16, 8, 4, 2, 1, and 1/2 unit capacitors (from top to bottom), and at the right of it, the very large EEPROM switches and their related capacitors are located. With $W/L = 270/2$, they are probably the world's largest EEPROM transistors.

VI. Conclusion

A novel integrated circuit for a batteryless transponder has been described. Low-power consumption has been achieved by optimizing circuit design and technology. The chip has been fabricated in a 2 μm CMOS process with EEPROM capability (SLM, DLP, n-well). Moreover, this technology not only allows the realization of read-only transponders, but also read/write transponders with a writing distance of half the reading distance [11].

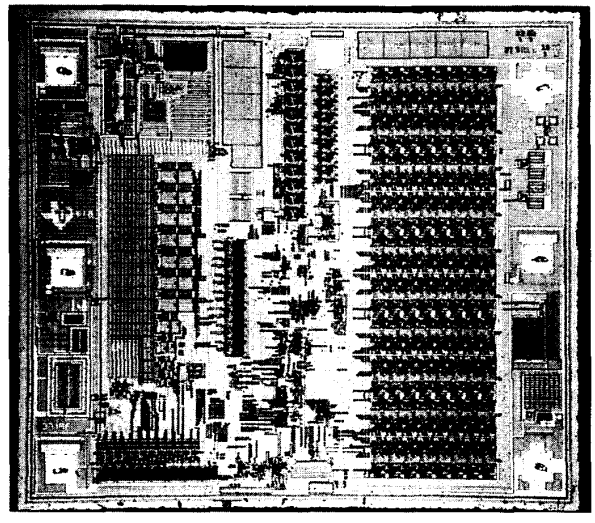

Fig. 13. Transponder chip photograph.

Acknowledgment

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