

# Low Offset and High Slew Rate Buffer amplifier for LCD Application

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## ABSTRACT

The proposed buffer achieves low offset and high slew rate in proposed circuit NMOS folded cascode operation amplifier is used instead of rail to rail operation amplifier, use of only NMOS folded cascode operation amplifier reduces the number of MOS used in circuit and using auto zero negative feedback will provide full swing for positive and negative feedback polarity pixel, and to decrease the offset a current distributed load is used which increases DC gain of operational amplifier and as DC gain increases it reduces offset voltage and increases slew rate with same bias current used in folded and summing stage of operational amplifier. The proposed circuit is simulated and verified in LT-spice and Microwind simulation tool using 350nm CMOS TSMC foundry with 3.3 V supply voltage the offset calculated is around .2mV and slew rate is 14V/ $\mu$ s.

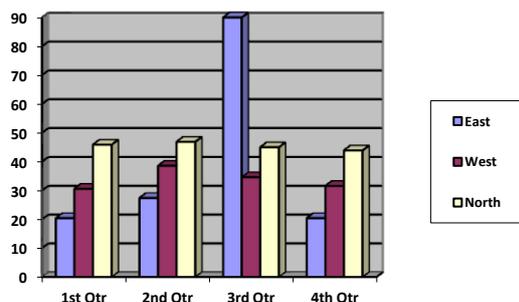
## Keywords

LCA, Buffer Amplifier

## 1. INTRODUCTION

In the recent advancement liquid crystal display becomes one of the most popular display device many computers electronics graduates uses it as a display unit each pixel requires an output buffer for high quality display.

To drive having the resistance and capacitive load the widely used class AB buffer amplifier. A display unit consist of source driver, gate driver, timing controller, voltage transformer, reference voltage generator and Gamma correction voltage levels. The column driver of the LCD is the most important part in LCD architecture for Fast speed high resolution low power dissipation are controlled by column driver. An and LCD column driver generally includes digital to analog converter, data latch, shift registers and output buffers among these output buffers is the most dominant to define the speed, resolution, voltage swing and power consumption as the display pixel are always updated row-by-row, the output buffers must be driven by a step size function so there output voltage should be settled within the horizontal scanning time.

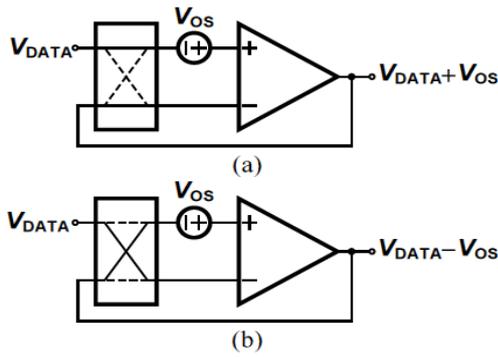


LCD output buffer are commonly realized by two stage operational amplifier in unity feedback configuration since to increase the phase margin use Miller compensation capacitor which involve high area consumption, so to avoid this at output node we use dominant pole to exploit them Miller capacitance, to provide high-speed driving capability we use current comparators at output in order to improve not only high-speed but also decreases power consumption during static and increases slew rate.

Lu et al. [5]–[14] proposed some class-AB output buffers for flat-panel-display application, for which the driving capabilities of the circuit are achieved by adding comparators which sense the rising and/or falling edges of the input waveform to turn on a push/pull transistor to charge/discharge the output load. Yu et al. [15] proposed a class-B output buffer for flat-panel-display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage. Kim et al. [6] proposed a multi-level multi-phase charge-recycling method for low-power AMLCD column drivers. The author proposed this charge-recycling method to reduce the power consumption incurred in driving highly capacitive column lines by storing the charge into the external capacitors and reusing it in the next cycle. Itakura et al. [13-20] proposed an output amplifier in which the phase compensation is achieved by introducing a zero, which is formed by the load capacitance and the phase compensation resistor connected between the output of the amplifier and the capacitive load.

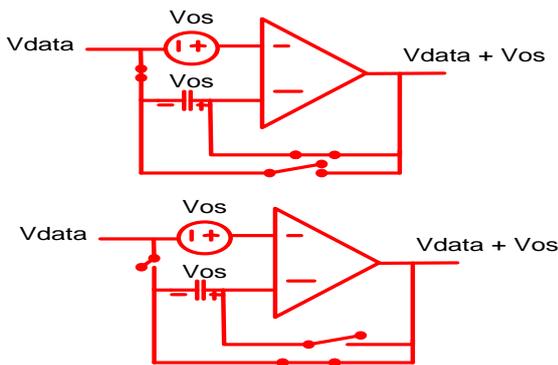
To achieve high resolution for LCD panel DAC resolution should be high and the offset of buffer should be less than resolution of DAC. So, two basic offset cancellation structures with their simple structure are commonly used in LCD source driver, which are chopper and auto-zero [8]–[14]. However, the output buffers in these two structures are still too complicated due to their wide input and output range.

Therefore, we want to improve the offset cancellation structure, and simplify output buffer to become cost-effective. The structure of chopper is shown in Fig. 1. It uses four switches to interchange the input of output buffer so that the offset voltage shown in output is inversed in different two states. If we output positive offset voltage in one frame and negative offset voltage in the next frame, the offset voltage will be averaged to zero. It is important that the output buffer has to change polarity in these two different states. The simple structure of chopper makes it used in some prior researches for offset cancellation [11], [12].



**Fig 1. Chopper output (a) positive offset voltage (b) negative offset voltage**

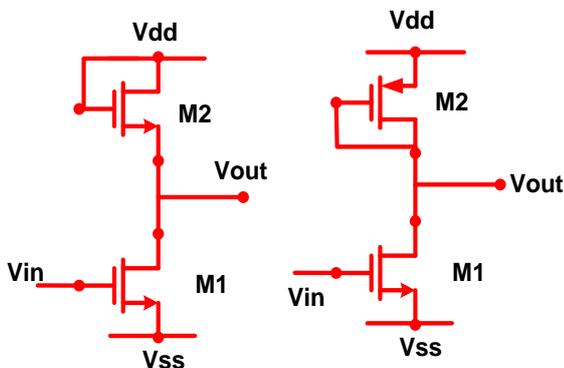
Fig. 2 shows the structure of auto-zero. The basic concept of auto-zero is sampling. It samples the offset voltage and stores in a capacitor in sample state. In output state it cancels the offset voltage due to law of charge conservation. It uses three switches and one capacitor to achieve auto-zero. Usually in LCD source driver uses metal-in-metal (MIM) capacitor as storage capacitor that it won't increase the area of source driver. The simple structure of auto-zero is also used in some prior researches for offset cancellation [8], [13].



**Fig 2. Auto-zero structure (a) sample state (b) output state**

## 2. CURRENT DISTRIBUTED TECHNIQUE FOR GAIN ENHANCEMENT

As diode connected load replaces the conventional resistance as it acquires large area on silicon chip. Fig 3, shows diode connected NMOS and PMOS load. The gain increase if we increase the load resistance, but it increase overdrive and hence the swing of output decreases,



**Fig 3 CS stage with diode connected load, NMOS & PMOS**

$$A_V = -g_{m1} \frac{1}{g_{m2} + g_{mb2}}$$

$$= \frac{g_{m1}}{g_{m2}} \frac{1}{1 + \eta}$$

$$\eta = \frac{g_{mb2}}{g_{m2}}$$

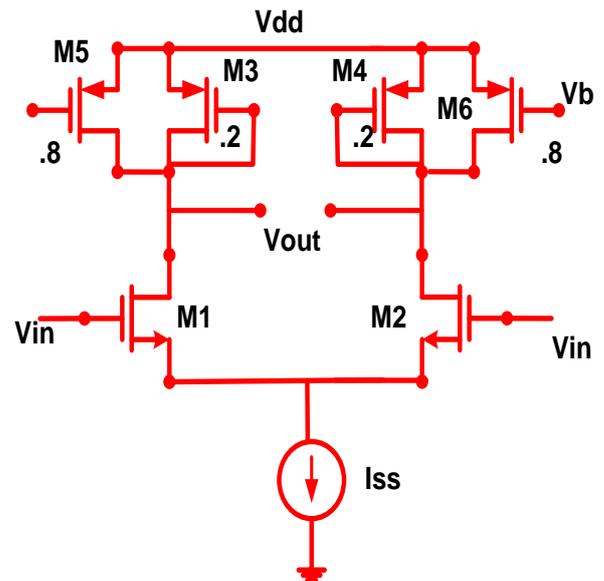
$$A_V = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}$$

if  $\eta$  is neglected the gain is independent of bias current and voltage, means the gain remains constant shows input and output varies linearly, to make it free from body effect we use PMOS as a active load.

As  $I_{D1} = I_{D2}$  so,

$$\mu_n \left(\frac{W}{L}\right)_1 (v_{gs1} - v_{th1})^2 \approx \mu_p \left(\frac{W}{L}\right)_2 (v_{gs2} - v_{th2})^2$$

$$A_V \approx -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cong A_V \approx -\left| \frac{v_{gs1} - v_{th1}}{v_{gs2} - v_{th2}} \right|$$



**Fig 4. Differential amplifier design using current distributed load to increase the gain**

In the circuit the diode-connected loads consume voltage headroom, thus creating a trade-off between the output voltage swings, the voltage gain, and the input CM range. For given bias current and input device dimensions, the circuit's gain and the PMOS overdrive voltage scale together. To achieve a higher gain,  $(W/L)_p$  must decrease, thereby increasing  $[V_{GSP} - V_{THp}]$  and lowering the CM level .

In order to alleviate the above difficulty, part of the bias currents of the input transistors can be provided by PMOS current sources. Illustrated in Fig. 4., the idea is to lower the  $g_m$  of the load devices by reducing their current rather than their aspect ratio. For example, if M5 and M6 carry 80% of the drain current of M1 and M2, the current through M3 and M4 is reduced by a factor of five. For a given  $I_{V_{GSP}} - V_{TH}$

$p_1$ , this translates to a factor of five reduction in the transconductance of M3 and M4 because the aspect ratio of the devices can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current sources. if M5 and M6 carry 80% of the drain current of M1 and M2, the current through M3 and M4 is reduced by a factor of five. For a given  $I_{V_{GSP}} - V_{THP1}$ , this translates to a factor of five reduction in the transconductance of M3 and M4 because the aspect ratio of the devices can be lowered by the same factor. Thus, the differential gain is now approximately five times that of the case with no PMOS current sources.

The auto zero with positive feedback technique and gain enhancement using current distributed load both combined in my proposed circuit to reduce the offset and it also enhance the slew rate.

As digital to analog converter is symmetric with respect to a common  $V_{com}$  voltage which is used of LCD to drive positive and negative pixel as for dot inversion matrix which is generally used in LCD driving mechanism. The symmetric luminance vs applied voltage with respect to  $V_{com}$  is shown in figure. 5 As due to this symmetry we don't need rail-to-rail configuration for buffer.

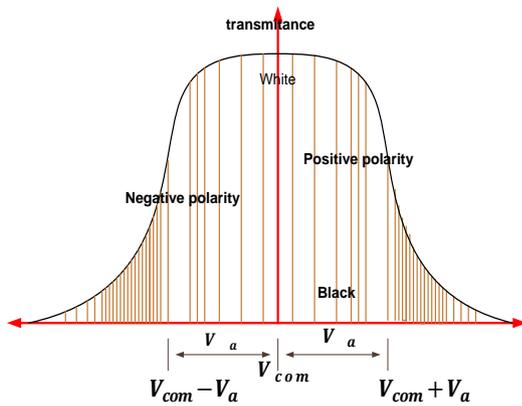


Fig 5 . Luminance vs applied voltage

As the DAC used in LCD is symmetric about the skew common voltage  $V_{com}$ , So here we use

$V_{com}$  voltage as common to drive the buffer for positive polarity and negative polarity buffer, means the buffer will up and down with this  $V_{com}$  reference voltage, and if we use auto zero with negative feedback then we do not need rail-to-rail operation.

The sampling method of auto-zero is better than averaging method of chopper Since conventional auto-zero samples only the offset voltage in sample state, the offset cancellation structure in negative feedback auto zero structure samples more voltage levels, including offset voltage in sample phase and output ideal  $V_{DATA}$  in output phase. Below we describe the detail function of this structure. Because of virtual short property of negative.

Because of virtual short property of negative feedback, we can get the output voltage and stored voltage in capacitor at sample phase in above that

$$V_{OUT} = V_{REF} + V_{OS}$$

$$V_C = V_{OUT} - V_{DATA} = V_{REF} + V_{OS} - V_{DATA}$$

We can see that the stored voltage in sample phase includes reference, offset and data input voltages, which is different from conventional auto-zero. Due to negative feedback and the law of charge conservation, we can get output voltage when it goes to output phase in Fig. above that

$$V_C = V_{REF} + V_{OS} - V_{OUT} = V_{REF} + V_{OS} - V_{DATA}$$

$$V_{OUT} = V_{REF} + V_{OS} - V_{REF} - V_{OS} + V_{DATA} = V_{DATA}$$

In this manner, we can achieve offset cancellation to output ideal  $V_{DATA}$ . We can see from Fig. 5 that the input voltage of output buffer is fixed at reference voltage either in sample or output phase. It means output buffer can output full gray-level voltage range with constant input voltage level. This characteristic is important that we can simplify structure of output buffer to achieve cost-effective offset cancellation structure.

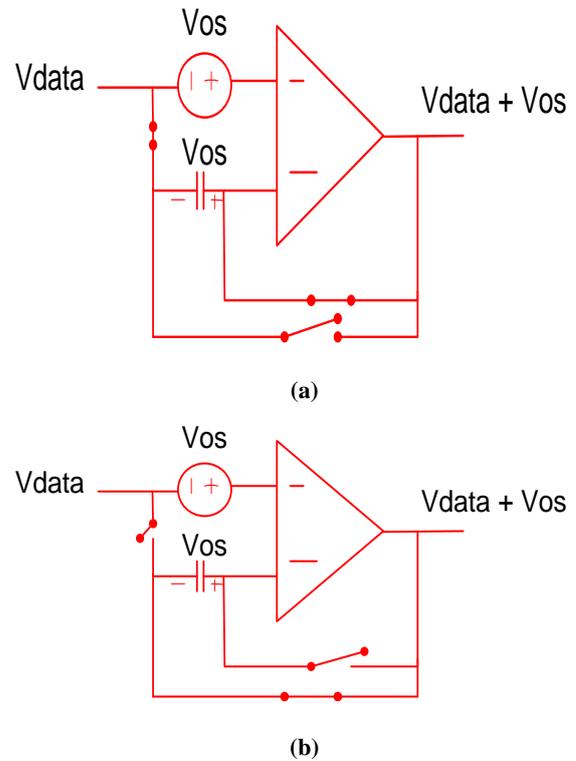


Fig. 6. Positive feedback auto zero offset cancellation structure (a) sample phase (b) output

### 3. PROPOSED BUFFER AMPLIFIER

The proposed buffer configuration contains biasing network (MB1-MB4), NMOS differential amplifier M5 & M6 and M7 for biasing, M8,M17 for folded summing stage and M18,M19 class AB output stage as shown in fig 4.1. Input differential amplifier are designed to draw the same current value  $nI_{B1}/2$ , where  $I_{B1}$  is the quiescent current supplied by the bias network devices MB1-MB4 and  $n$  is the mirror factor of current sources M1 and M4, defined as

$$n = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_{M1}}$$

Assuming an equal aspect ratio for transistors M8,M9,M12,13 and M11-M17, the currents in both branches of the folded-cascode mirror have the same value. Hence, the drain voltages

of M9 and M17 are respectively equal to those of M15 and M16. The currents flowing in M9 and M11 are given by

$$I_{M11} = I_{M9} = n \frac{I_7}{2} + I_{10}$$

Since the gate voltages of M10 and M14 are respectively sizing of the current mirror factors of the folded-cascode input stage, and no additional biasing networks are required to maintain an almost constant output current. Therefore, the output quiescent current of the amplifier class-AB section can get opportunely set by means of an appropriate W/L ratio of M10 & M14, a push-pull O/P stage M18 & M19, operate in class AB mode will turn ON and OFF according to the current distribution at M9 and M12.

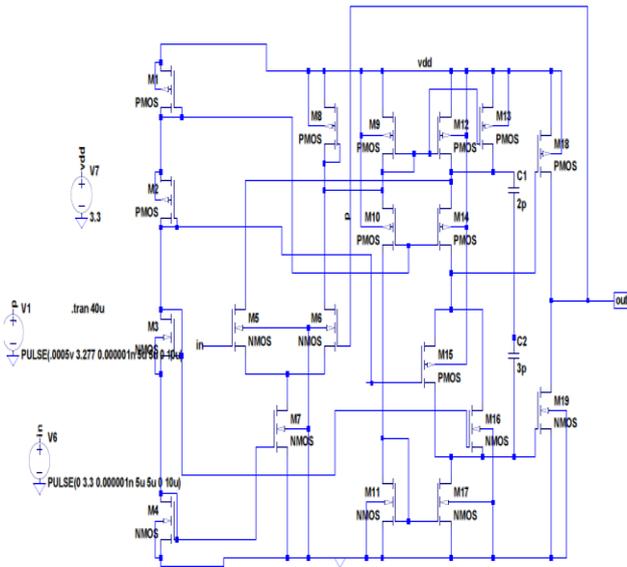


Fig 7. Schematic of proposed buffer

Device dimension of Proposed buffer

| Device                  | Dimension |
|-------------------------|-----------|
| M1, M2, M7              | 9.8/2     |
| M4, M3                  | 4.9/2     |
| M5, M6                  | 19.6/2    |
| M9, M11, M17            | 10/2      |
| M10, M13, M14, M15, M16 | 5/2       |
| M18                     | 3/2       |
| M19                     | 2/5       |

#### 4. SIMULATION RESULT

Simulation and results are obtained using LTSPICE IV & MICROWIND 3 software's. Results illustrate the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 30pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depicts the simulated transient response to a 50-

kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/μs and 14V/μs for the rising and falling edges, respectively, the offset value of buffer found during simulation is in between .15mv - .2mV during multiple simulations.

Simulation of proposed buffer using 50 KHz square wave input signal in LT-spice using CMOS TSMC 350nm foundry is shown in fig 8. Simulation of proposed buffer using 50 KHz square wave input signal in LT-spice using CMOS TSMC 350nm foundry with different capacitive load in between 5p-30p farad is shown in fig 9. Simulation of proposed buffer using 50 KHz triangular wave input signal in LT-spice using CMOS TSMC 350nm foundry is shown in fig 10.

Design of NMOS folded cascode circuit diagram with current distributed active load using 350nm CMOS technology using Microwind is shown in fig 11. Simulation of proposed buffer using 50 KHz square wave input signal in Microwind using CMOS TSMC 350nm foundry is shown in fig 12. Simulation of proposed buffer using 50 KHz triangular wave input signal in Microwind using CMOS TSMC 350nm foundry is shown in fig 13.

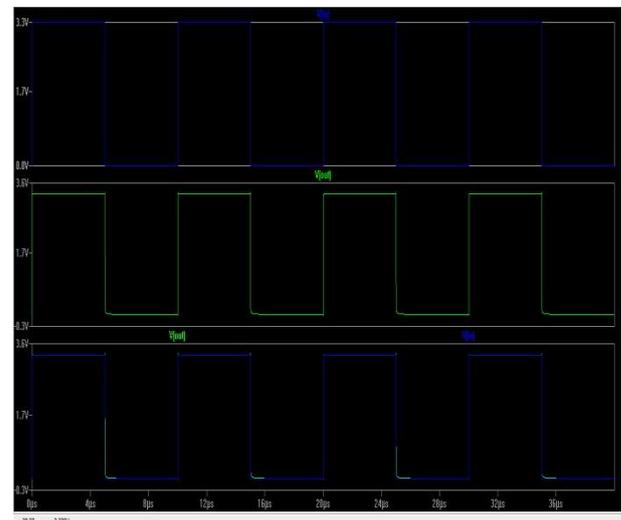


Fig 8. Simulation result of proposed buffer with square wave

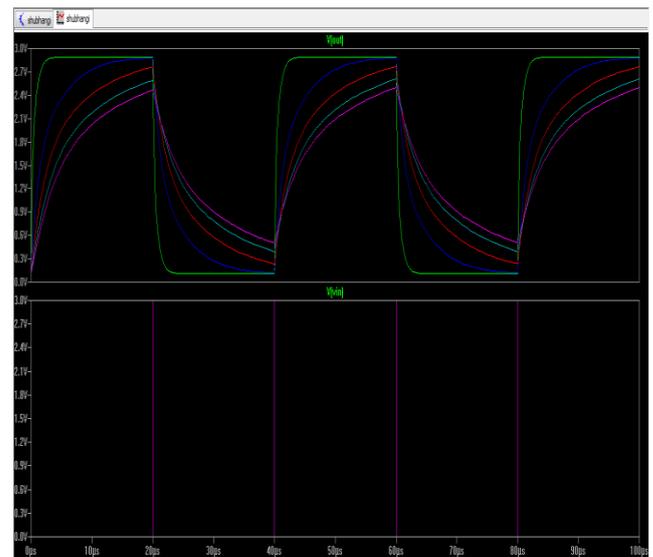


Fig 9. Simulation result of proposed buffer with different capacitive load 5p-30p with square wave

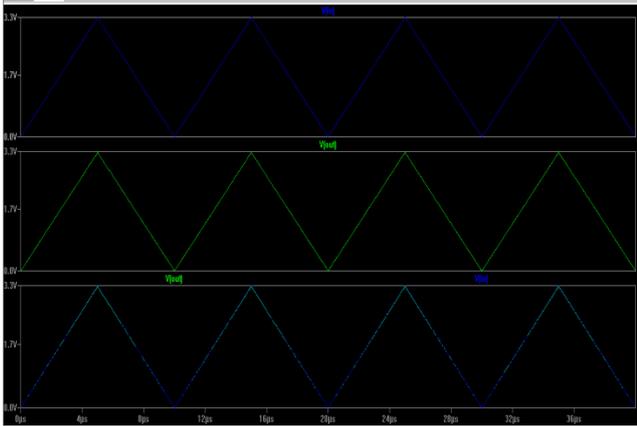


Fig 10. Simulation result of proposed buffer with triangular wave

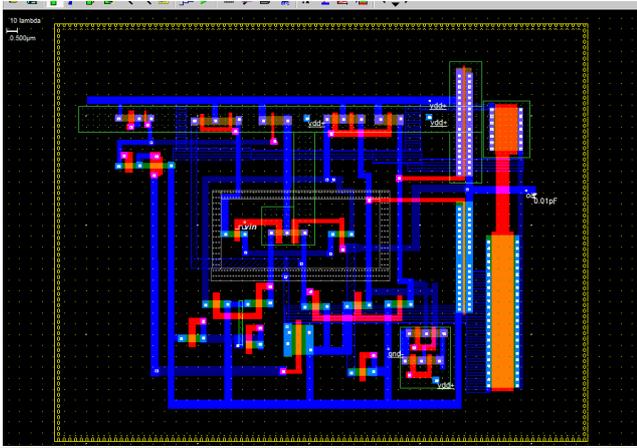


Fig 11. Layout of proposed Buffer amplifier

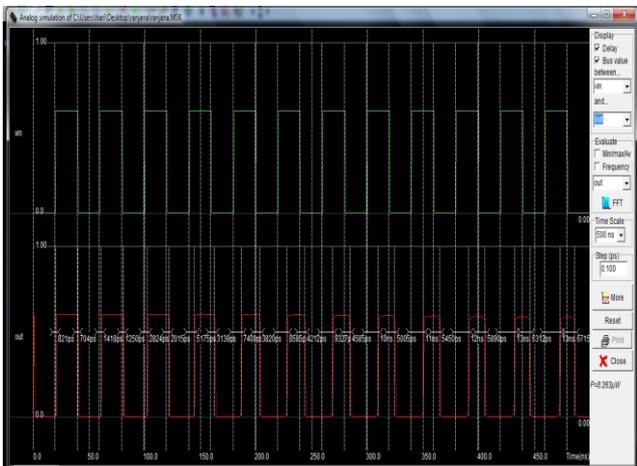


Fig 12. Simulation result of proposed buffer with square wave input

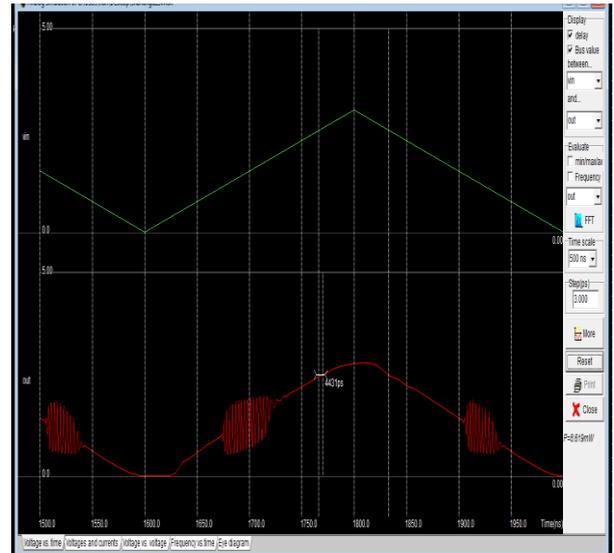


Fig 13. Simulation result of proposed buffer with triangular wave input

Table 2. Comparison table

|                    | [1]     | [2]   | [3]    | [4]       | This work |
|--------------------|---------|-------|--------|-----------|-----------|
| CMOS TECHNOLOGY    | 180nm   | 600nm | 350nm  | 350nm     | 350nm     |
| SUPPLY VOLTAGE (V) | 5v      | 3v    | 5v     | 5v        | 3.3v      |
| IN/OUT RANGE (V)   | 0-5 V   | 0-3 V | 0-5 V  | 0.3-4.7 V | 0-3.3     |
| TRANSISTOR COUNT   | 19      | 36    | 30     | 18        | 19        |
| OFFSET VOLTAGE     | 1.85 mV | NA    | 6.1 mV | NA        | .3 mV     |
| MAXIMUM DIFFERENCE | 40µV    | NA    | NA     | 1.4mV     | 1mV       |
| SLEW RATE (V/µs)   | NA      | NA    | NA     | NA        | 14 V/µs   |

## 5. CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. With the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously. With different capacitive load from 5p to 30p as shown in fig2 & fig 3 with square and triangular wave. A comparison table 2 show the different parameters in comparison with previous results. A simulation in micro-wind tool is shown in Fig 4, fig 5, fig 6 with square and triangular wave input.

## 6. FUTURE SCOPE

Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilises a only 0.2 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas-

\* Since power consumption is low, it has a great future in getting utilized in applications like “ultra low power ADCs”.

\* Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in “image exhibit contrivances, flat panel exhibits etc.

\*Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks. Above are just few examples, but this buffer is having excellent usability in many other areas also.

## 7. REFERENCES

- [1] Ming-Wei Hsu and Chern-Lin Chen “A Cost-Effective Offset Cancellation Structure for LCD Source Driver” 978-1-4799-3432-4/14/\$31.00 ©2014 IEEE.
- [2] C.-W. Lu, “A rail-to-rail class-AB amplifier with an offset cancellation for LCD drivers,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 525-537, Feb. 2009.
- [3] G.-T Hong and C.-H. Shen, “A low offset high voltage swing rail-to-rail buffer amplifier with for LCD driver,” in *Proc. IEEE Conf. on Electron Devices and Solid-State Circuits*, 2007, pp. 814-846.
- [4] C.-H. Tsai, J.-H. Wang, H.-Y. Zheng, C.-T. Chang, and C.-Y. Wang, “A new compact low-offset push-pull output buffer with current positive feedback for a 10-bit LCD source driver,” *IET Journal of Circuits, Devices & Systems*, vol. 4, no. 6, pp. 539-547, Nov. 2010.
- [5] Chih-Wen Lu, “High-Speed Driving and Compact High-Speed Low-power Rail-to-Rail Class-B Buffer Amplifier for Small- and Large-size LCD Applications,” accepted by *IEEE Journal of Solid-State Circuit*.
- [6] Ming-Chan Weng and Jiin-Chuan Wu, “A Compact Low- Power Rail-to-Rail Class-B Buffer for LCD Column Driver,” *IEICE Trans. Electron.*, Vol. E85-C, No. 8 August, pp. 1659- 1663, 2002.
- [7] Pang-Cheng Yu and Jiin-Chuan Wu, “A Class-B Output Buffer for Flat-Panel-Display Column Driver,” *IEEE Journal of Solid-State Circuits*, Vol. 34, No.1, Jan. pp. 116-119, 1999.
- [8] D. J. R. Cristaldi, S. Pennisi, and F. Pulvirenti, *Liquid Crystal Display Drivers: Techniques and Circuits*. New York: Springer, Mar. 2009.
- [9] S. Di Fazio, S. Pennisi, F. Pulvirenti, and T. Signorelli, “670-nA CMOS OTA for AMLCD column driver,” *J. Circuits, Syst., Comput.*, vol. 18, no. 2, pp. 339–350, Apr. 2009.
- [10] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, “A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries,” *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.
- [11] T. Itakura, “A high slew-rate operational amplifier for an LCD driver IC,” *IEICE Trans. Fundamentals*, vol. E78-A, no. 2, pp. 191–195, Feb. 1995.
- [12] T. Itakura and H. Minamizaki, “10- .A quiescent current opamp design for LCD driver ICs,” *IEICE Trans. Fundamentals*, vol. E81-A, no. 2, Feb. 1998.
- [13] C.-W. Lu and K. Hsu, “A high-speed low-power rail-to-rail column driver for AMLCD application,” *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1313–1320, Aug. 2004.
- [14] Y. S. Son, J. H. Kim, H. H. Cho, J. P. Hong, J. H. Na, D. S. Kim, D. K. Han, J. C. Hong, Y. J. Jeon, and G. H. Cho, “A column driver with low-power area-efficient push-pull buffer amplifiers for active-matrix LCDs,” *ISSCC Dig. Tech. Papers*, pp. 142–143, Feb. 2007.
- [15] R. Ito, T. Itakura, and H. Minamizaki, “A class-AB amplifier for LCD driver,” in *IEEE Symp. on VLSI Circuits*, June 2007, pp. 148–149.
- [16] P.-C. Yu and J.-C. Wu, “A class-B output buffer for flat-panel-display column driver,” *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 116–119, Jan. 1999.
- [17] C.-W. Lu and C. L. Lee, “A low-power high-speed class-AB buffer amplifier for flat-panel-display application,” *IEEE Trans. Very Large- Scale Integr. (VLSI) Syst.*, vol. 10, no. 4, pp. 163–168, Apr. 2002.
- [18] M.-C. Weng and J.-C. Wu, “A compact low-power rail-to-rail class-B buffer for LCD column driver,” *IEICE Trans. Electron.*, vol. E85-C, no. 8, pp. 1659–1663, Aug. 2002.
- [19] T. Itakura and H. Minamizaki, “A two-gain-stage amplifier without an on-chip miller capacitor in an LCD driver IC,” *IEICE Trans. Fundamentals*, vol. E85-A, no. 8, pp. 1913–1920, Aug. 2002.
- [20] T. Itakura, H. Minamizaki, T. Satio, and T. Kuroda, “A 402-output TFT-LCD driver IC with power control based on the number of colors selected,” *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 503–510, Mar. 2003.
- [21] C.-W. Lu, “High-speed driving scheme and compact high-speed low power rail-to-rail class-B buffer amplifier for LCD applications,” *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1938–1947, Nov. 2004.
- [22] C.-W. Lu and P. H. Xiao, “A high-speed low-power rail-to-rail buffer amplifier for LCD application,” in *Proc. CCECE ’06*, Dec. 2006, pp. 709–712.
- [23] J.-H. Wang, J.-C. Qiu, H.-Y. Zheng, C.-H. Tsai, C.-Y. Wang, C.-C. Lee, and C.-T. Chang, “A compact low-power high slew-rate rail-to rail class-AB buffer amplifier for LCD driver ICs,” in *Proc. EDSS ’07*, Dec. 2007, pp. 397–400.
- [24] D. Marano, G. Palumbo, and S. Pennisi, “Improved low-power high speed buffer amplifier with slew-rate enhancement for LCD applications,” *J. Circuits, Syst., Comput.*, to be published.
- [25] R. Mita, G. Palumbo, and S. Pennisi, “Low-voltage high-drive CMOS current feedback opamp,” *IEEE Trans. Circuits Syst. II*, vol. 52, pp. 317–321, June 2005.

- [26] M. Annese, S. Bertaiola, G. Croce, A. Milani, R. Roggero, P. Galbiati, and C. Costiero, "0.18 .. BCD-High Voltage Gate (HVG) process to address advanced display drivers roadmap," Proc. Power Semiconductor Devices and ICs, pp. 363–366, 2005.
- [27] Chih-Wen Lu and Kuo Jen Hsu, "A High-Speed Low-Power Rail-to-Rail Column Driver for AMLCD Application" IEEE Journal of Solid-State Circuits, vol. 39, pp. 1313-1320, Aug., 2004.
- [28] Chih-Wen Lu, "High-Speed Driving and Compact High-Speed Low-power Rail-to-Rail Class-B Buffer Amplifier for Small- and Large-size LCD Applications," accepted by IEEE Journal of Solid-State Circuit.
- [29] Ming-Chan Weng and Jiin-Chuan Wu, "A Compact Low- Power Rail-to-Rail Class-B Buffer for LCD Column Driver," IEICE Trans. Electron., Vol. E85-C, No. 8 August, pp. 1659- 1663, 2002.
- [30] Pang-Cheng Yu and Jiin-Chuan Wu, "A Class-B Output Buffer for Flat-Panel-Display Column Driver," IEEE Journal of Solid-State Circuits, Vol. 34, No.1, Jan. pp. 116-119, 1999.
- [31] Tetsuro Itaku, Hironori Minamizaki, Tetsuya Satio, and Tadashi Kuroda, "A 402-Output TFT-LCD Driver IC With Power Control Based on the Number of Colors Selected," IEEE Journal of Solid-State Circuits, Vol. 38, No.3, March, pp. 503-510, 2003.
- [32] TFT-LCD source drivers NT39360, NT3982, and NT3994. Novatek. [Online]. Available: <http://www.novatek.com.tw/>.